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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2432
Number of Logic Elements/Cells	24320
Total RAM Bits	311296
Number of I/O	508
Number of Gates	1537000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k600cf672i8aa">https://www.e-xfl.com/product-detail/intel/ep20k600cf672i8aa</a>

**Table 7. APEX 20KC Device Features (Part 2 of 2)**

Feature	APEX 20KC Devices
I/O standard support	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI and PCI-X 3.3-V AGP CTT GTL+ LVCMOS LVTTTL True-LVDS™ and LVPECL data pins (in EP20K400C and larger devices) LVDS and LVPECL clock pins (in all devices) LVDS and LVPECL data pins up to 156 Mbps (in EP20K200C devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	CAM Dual-port RAM FIFO RAM ROM

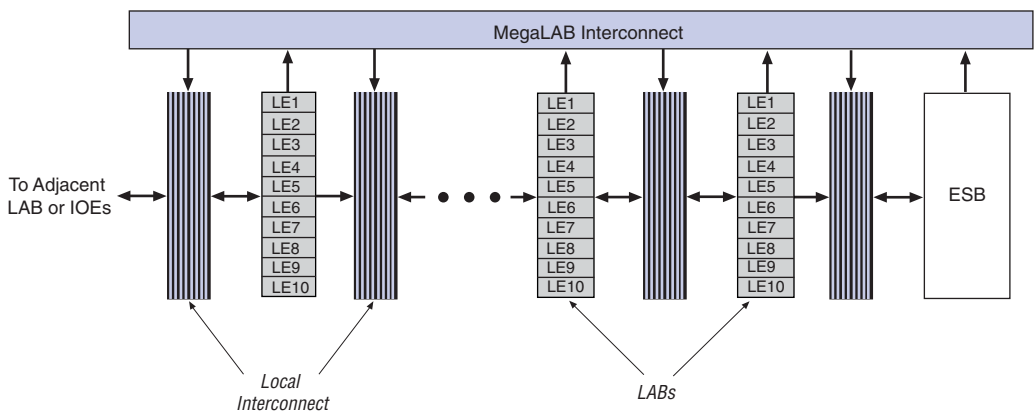
All APEX 20KC devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault-coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20KC devices can be configured on the board for the specific functionality required.

APEX 20KC devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC16, EPC8, EPC4, EPC2, and EPC1 configuration devices and one-time programmable (OTP) EPC1 configuration devices, which configure APEX 20KC devices via a serial data stream. Moreover, APEX 20KC devices contain an optimized interface that permits microprocessors to configure APEX 20KC devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20KC devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

## MegaLAB Structure

APEX 20KC devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. In EP20K1000C devices, MegaLAB structures contain 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

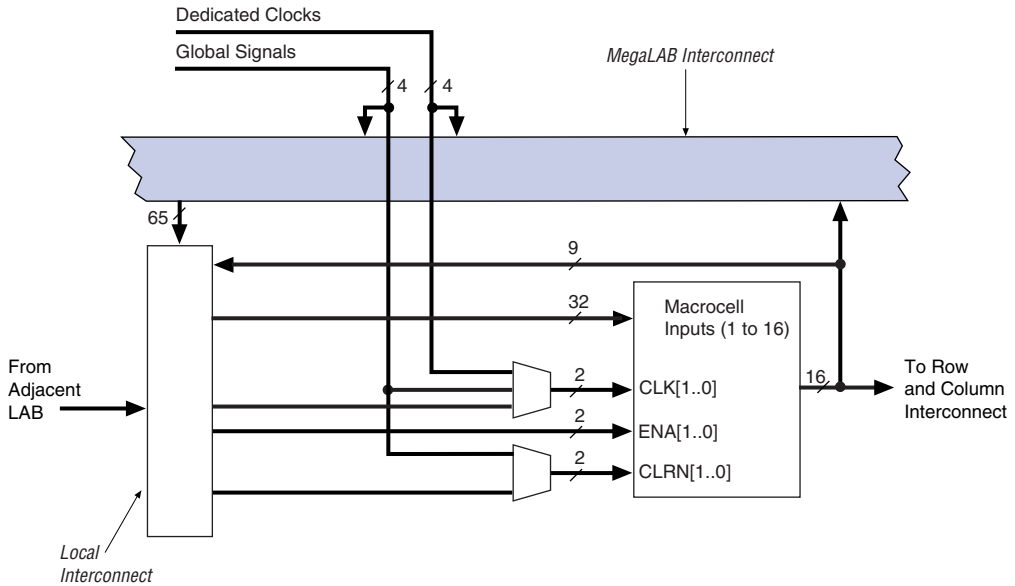
**Figure 2. MegaLAB Structure**



## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20KC LAB.

APEX 20KC devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas, minimizing the use of the MegaLAB and FastTrack interconnect and providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

**Figure 13. Product-Term Logic in ESB**

### Macrocells

APEX 20KC macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform De Morgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. [Figure 14](#) shows the APEX 20KC macrocell.

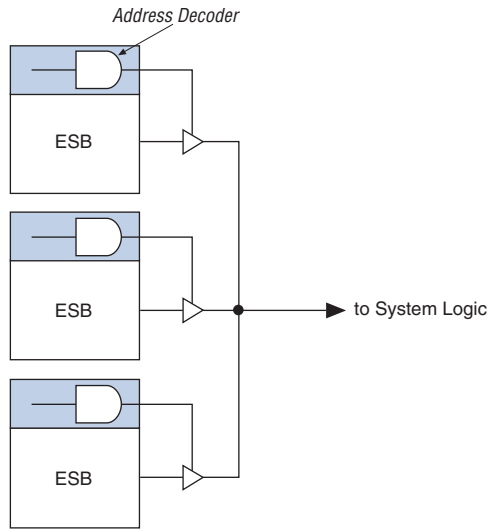
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the FastTrack or MegaLAB interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the FastTrack and MegaLAB interconnects. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes:  $128 \times 16$ ,  $256 \times 8$ ,  $512 \times 4$ ,  $1,024 \times 2$ , or  $2,048 \times 1$ . By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two  $128 \times 16$  RAM blocks can be combined to form a  $128 \times 32$  RAM block, and two  $512 \times 4$  RAM blocks can be combined to form a  $512 \times 8$  RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See [Figure 18](#).

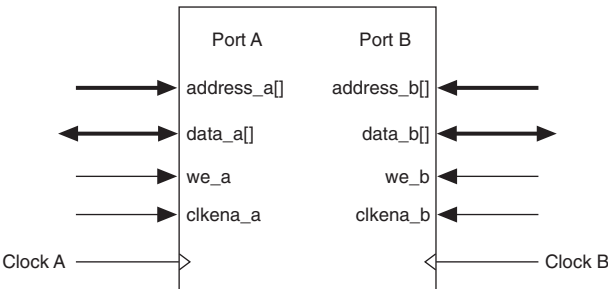
Figure 18. Deep Memory Block Implemented with Multiple ESBs



The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two ESBs are used to support two simultaneous reads or writes.

The ESB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in [Figure 19](#).

Figure 19. APEX 20KC ESB Implementing Dual-Port RAM



**Notes to Figure 25:**

- (1) This programmable delay has four settings: off and three levels of delay.
- (2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. **Figure 26** shows how a row IOE connects to the interconnect.

**Figure 26. Row IOE Connection to the Interconnect**

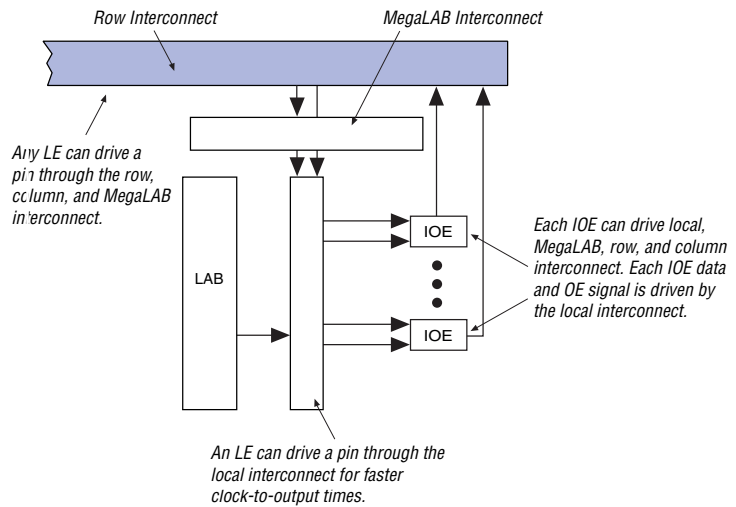
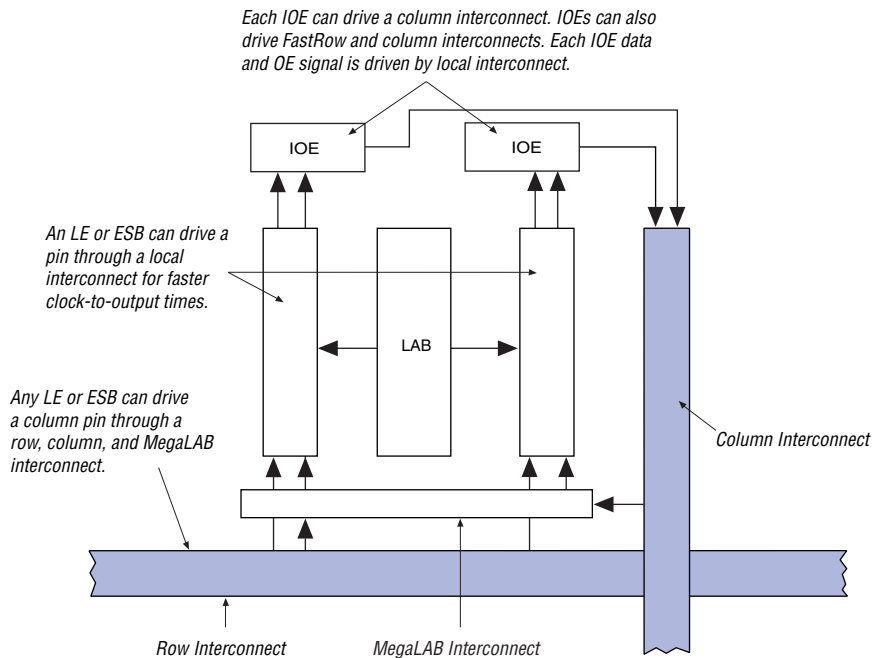


Figure 27 shows how a column IOE connects to the interconnect.

**Figure 27. Column IOE Connection to the Interconnect**



## Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.



## Advanced I/O Standard Support

APEX 20KC IOEs support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.



For more information on I/O standards supported by APEX 20KC devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KC device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL at up to 156 Mbps per channel with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate  $V_{REF}$  level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K400C and larger APEX 20KC devices support the LVDS interface for data pins (EP20K200C devices support LVDS clock pins, but not data pins). EP20K400C and EP20K600C devices support LVDS for data pins at up to 840 Mbps per channel. EP20K1000C devices support LVDS on 16 channels at up to 750 Mbps.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used for the LVDS I/O standard, they support all of the other I/O standards. [Figure 28](#) shows the arrangement of the APEX 20KC I/O banks.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20KC devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20KC devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc). Finally, APEX 20KC devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20KC devices support the JTAG instructions shown in [Table 13](#).

**Table 13. APEX 20KC JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20KC device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

**Figure 30. APEX 20KC JTAG Waveforms**

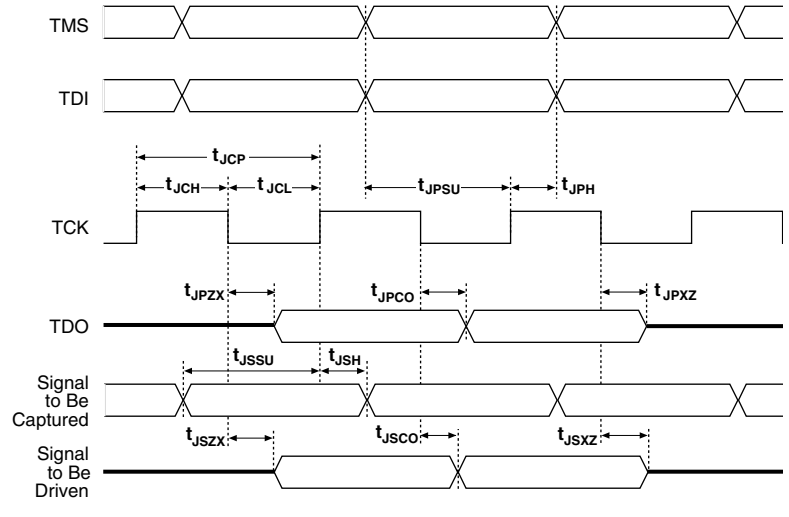


Table 16 shows the JTAG timing parameters and values for APEX 20KC devices.

**Table 16. APEX 20KC JTAG Timing Parameters & Values**

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		35	ns
$t_{JSZX}$	Update register high impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- [Application Note 39 \(IEEE Std. 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#)

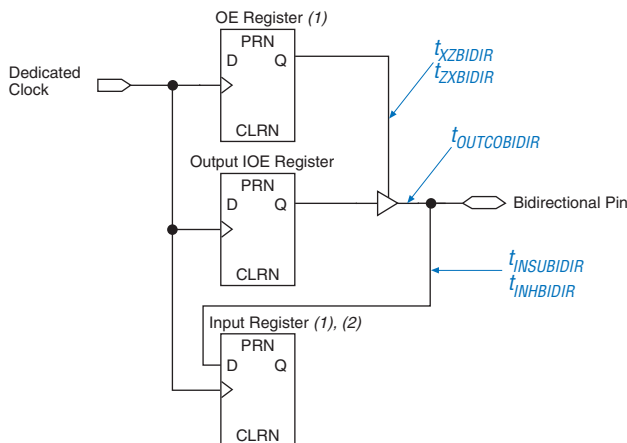
**Table 26. 3.3-V PCI-X Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{CCIO}$	Output supply voltage		3.0	3.3	3.6	V
$V_{IH}$	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
$V_{IL}$	Low-level input voltage		-0.5		$0.35 \times V_{CCIO}$	V
$V_{IPU}$	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
$I_{IL}$	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	-10.0		10.0	$\mu A$
$V_{OH}$	High-level output voltage	$I_{OUT} = -500 \mu A$	$0.9 \times V_{CCIO}$			V
$V_{OL}$	Low-level output voltage	$I_{OUT} = 1,500 \mu A$			$0.1 \times V_{CCIO}$	V
$L_{pin}$	Pin Inductance				15.0	nH

**Table 27. 3.3-V LVDS I/O Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{CCIO}$	I/O supply voltage		3.135	3.3	3.465	V
$V_{OD}$	Differential output voltage	$R_L = 100 \Omega$	250		650	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between high and low	$R_L = 100 \Omega$			50	mV
$V_{OS}$	Output offset voltage	$R_L = 100 \Omega$	1.125	1.25	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ between high and low	$R_L = 100 \Omega$			50	mV
$V_{TH}$	Differential input threshold	$V_{CM} = 1.2 V$	-100		100	mV
$V_{IN}$	Receiver input voltage range		0.0		2.4	V
$R_L$	Receiver differential input resistor (external to APEX devices)		90	100	110	$\Omega$

**Figure 35. Synchronous Bidirectional Pin External Timing**



**Notes to Figure 35:**

- (1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin. Use the “Output Enable Routing = Single-Pin” option in the Quartus II software to set the output enable register.
- (2) Use the “Decrease Input Delay to Internal Cells = OFF” option in the Quartus II software to set the LAB-adjacent input register. This maintains a zero hold time for LAB-adjacent registers while giving a fast, position-independent setup time. Set “Decrease Input Delay to Internal Cells = ON” and move the input register farther away from the bidirectional pin for a faster setup time with zero hold time. The exact position where zero hold occurs with the minimum setup time varies with device density and speed grade.

Tables 36 to 38 describes the  $f_{MAX}$  timing parameters shown in Figure 32. Table 39 describes the functional timing parameters.

**Table 36. APEX 20KC  $t_{MAX}$  LE Timing Parameters**

Symbol	Parameter
$t_{SU}$	LE register setup time before clock
$t_H$	LE register hold time before clock
$t_{CO}$	LE register clock-to-output delay
$t_{LUT}$	LUT delay for data-in to data-out

**Table 39. APEX 20KC Minimum Pulse Width Timing Parameters**

Symbol	Parameter
$t_{CH}$	Minimum clock high time from clock pin
$t_{CL}$	Minimum clock low time from clock pin
$t_{CLRP}$	LE clear pulse width
$t_{PREP}$	LE preset pulse width
$t_{ESBCH}$	Clock high time
$t_{ESBCL}$	Clock low time
$t_{ESBWP}$	Write pulse width
$t_{ESBRP}$	Read pulse width

Tables 40 and 41 describe APEX 20KC external timing parameters. The timing values for these pin-to-pin delays are reported for all pins using the 3.3-V LVTTTL I/O standard.

**Table 40. APEX 20KC External Timing Parameters** *Note (1)*

Symbol	Clock Parameter	Conditions
$t_{INSU}$	Setup time with global clock at IOE register	
$t_{INH}$	Hold time with global clock at IOE register	
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE output register	(2)
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
$t_{INHPLL}$	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	(2)

Tables 44 through 67 show the  $f_{MAX}$  and external timing parameters for EPC20K200C, EP20K400C, EP20K600C, and EP20K1000C devices.

**Table 44. EP20K200C  $f_{MAX}$  LE Timing Microparameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.01		0.01		0.01		ns
$t_H$	0.10		0.10		0.10		ns
$t_{CO}$		0.27		0.30		0.32	ns
$t_{LUT}$		0.65		0.78		0.92	ns

**Table 45. EP20K200C  $f_{MAX}$  ESB Timing Microparameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.30		1.51		1.69	ns
$t_{ESBSRC}$		2.35		2.49		2.72	ns
$t_{ESBAWC}$		2.92		3.46		3.86	ns
$t_{ESBSWC}$		3.05		3.44		3.85	ns
$t_{ESBWASU}$	0.45		0.50		0.54		ns
$t_{ESBWAH}$	0.44		0.50		0.55		ns
$t_{ESBWDSU}$	0.57		0.63		0.68		ns
$t_{ESBWDH}$	0.44		0.50		0.55		ns
$t_{ESBRASU}$	1.25		1.43		1.56		ns
$t_{ESBRAH}$	0.00		0.03		0.11		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	2.01		2.27		2.45		ns
$t_{ESBWADDRSU}$	-0.20		-0.24		-0.28		ns
$t_{ESBRADDRSU}$	0.02		0.00		-0.02		ns
$t_{ESBDATAC01}$		1.09		1.28		1.43	ns
$t_{ESBDATAC02}$		2.10		2.52		2.82	ns
$t_{ESBDD}$		2.50		2.97		3.32	ns
$t_{PD}$		1.48		1.78		2.00	ns
$t_{PTERMSU}$	0.58		0.72		0.81		ns
$t_{PTERMCO}$		1.10		1.29		1.45	ns

**Table 49. EP20K200C External Bidirectional Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	1.38		1.78		1.99		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	3.79	2.00	4.31	2.00	4.70	ns
$t_{\text{XZBIDIR}}$		6.12		6.51		7.89	ns
$t_{\text{ZXBIDIR}}$		6.12		6.51		7.89	ns
$t_{\text{INSUBIDIRPLL}}$	2.82		3.47		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.36	0.50	2.62	-	-	ns
$t_{\text{XZBIDIRPLL}}$		4.69		4.82		-	ns
$t_{\text{ZXBIDIRPLL}}$		4.69		4.82		-	ns

**Table 50. EP20K400C  $t_{\text{MAX}}$  LE Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.01		0.01		0.01		ns
$t_{\text{H}}$	0.10		0.10		0.10		ns
$t_{\text{CO}}$		0.27		0.30		0.32	ns
$t_{\text{LUT}}$		0.65		0.78		0.92	ns



**Table 53. EP20K400C Minimum Pulse Width Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.33		1.66		2.00		ns
$t_{CL}$	1.33		1.66		2.00		ns
$t_{CLRP}$	0.20		0.20		0.20		ns
$t_{PREP}$	0.20		0.20		0.20		ns
$t_{ESBCH}$	1.33		1.66		2.00		ns
$t_{ESBCL}$	1.33		1.66		2.00		ns
$t_{ESBWP}$	1.05		1.28		1.44		ns
$t_{ESBRP}$	0.87		1.06		1.19		ns

**Table 54. EP20K400C External Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	1.37		1.52		1.64		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.25	2.00	4.61	2.00	5.03	ns
$t_{INSUPLL}$	0.80		0.91		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.27	0.50	2.55	-	-	ns

**Table 59. EP20K600C Minimum Pulse Width Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.33		1.66		2.00		ns
$t_{CL}$	1.33		1.66		2.00		ns
$t_{CLRP}$	0.20		0.20		0.20		ns
$t_{PREP}$	0.20		0.20		0.20		ns
$t_{ESBCH}$	1.33		1.66		2.00		ns
$t_{ESBCL}$	1.33		1.66		2.00		ns
$t_{ESBWP}$	1.05		1.28		1.44		ns
$t_{ESBRP}$	0.87		1.06		1.19		ns

**Table 60. EP20K600C External Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	1.28		1.40		1.45		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.29	2.00	4.77	2.00	5.11	ns
$t_{INSUPLL}$	0.80		0.91		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.37	0.50	2.63	-	-	ns

**Table 61. EP20K600C External Bidirectional Timing Parameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.03		2.57		2.97		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	4.29	2.00	4.77	2.00	5.11	ns
$t_{\text{XZBIDIR}}$		8.31		9.14		9.76	ns
$t_{\text{ZXBIDIR}}$		8.31		9.14		9.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.99		4.77		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.37	0.50	2.63	-	-	ns
$t_{\text{XZBIDIRPLL}}$		6.35		6.94		-	ns
$t_{\text{ZXBIDIRPLL}}$		6.35		6.94		-	ns

**Table 62. EP20K1000C  $t_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.01		0.01		0.01		ns
$t_{\text{H}}$	0.10		0.10		0.10		ns
$t_{\text{CO}}$		0.27		0.30		0.32	ns
$t_{\text{LUT}}$		0.66		0.79		0.92	ns

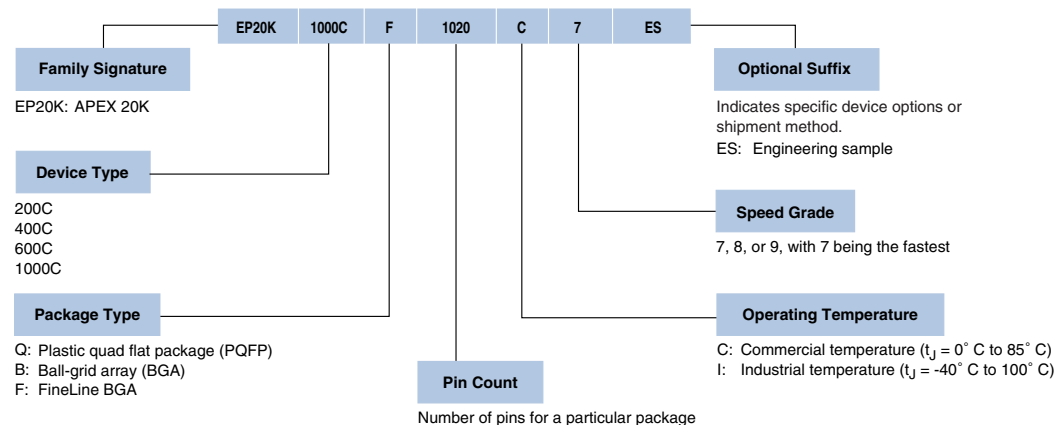
**Table 63. EP20K1000C  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.48		1.57		1.65	ns
$t_{ESBSRC}$		2.36		2.50		2.73	ns
$t_{ESBAWC}$		2.93		3.46		3.86	ns
$t_{ESBSWC}$		3.08		3.43		3.83	ns
$t_{ESBWASU}$	0.51		0.50		0.52		ns
$t_{ESBWAH}$	0.38		0.51		0.57		ns
$t_{ESBWDSU}$	0.62		0.62		0.66		ns
$t_{ESBWDH}$	0.38		0.51		0.57		ns
$t_{ESBRASU}$	1.40		1.47		1.53		ns
$t_{ESBRAH}$	0.00		0.07		0.18		ns
$t_{ESBWESU}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	1.92		2.19		2.35		ns
$t_{ESBWADDRSU}$	-0.20		-0.28		-0.32		ns
$t_{ESBRADDRSU}$	0.00		-0.03		-0.05		ns
$t_{ESBDATAO1}$		1.12		1.30		1.46	ns
$t_{ESBDATAO2}$		2.11		2.53		2.84	ns
$t_{ESBDD}$		2.56		2.96		3.30	ns
$t_{PD}$		1.49		1.79		2.02	ns
$t_{PTERMSU}$	0.61		0.69		0.77		ns
$t_{PTERMCO}$		1.13		1.32		1.48	ns

**Table 64. EP20K1000C  $t_{MAX}$  Routing Delays**

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.15		0.17		0.19	ns
$t_{F5-20}$		1.13		1.31		1.50	ns
$t_{F20+}$		2.30		2.71		3.19	ns

**Figure 39. APEX 20KC Device Packaging Ordering Information**



## Revision History

The information contained in the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2 supersedes information published in previous versions.

### Version 2.2

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.2:

- Updated [Tables 1](#).
- Updated notes in [Tables 20](#).

### Version 2.1

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 2.1:

- Removed figure on AC Test Conditions.
- Updated conditions in [Tables 40](#) and [41](#).
- Added [Tables 42](#) and [43](#).
- Updated  $V_{OD}$  in [Table 27](#).
- Added [Figures 36](#) through [38](#).
- Updated [Tables 44](#) through [49](#).
- Updated [Tables 62](#) through [67](#).
- Removed notes in [Tables 44](#) through [67](#).
- Various textual changes throughout the document.