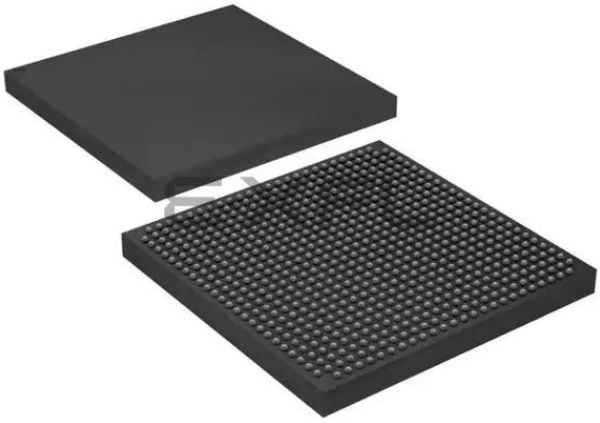

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2432 |
| Number of Logic Elements/Cells | 24320 |
| Total RAM Bits | 311296 |
| Number of I/O | 508 |
| Number of Gates | 1537000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k600cf672i8n |

After an APEX 20KC device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20KC devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

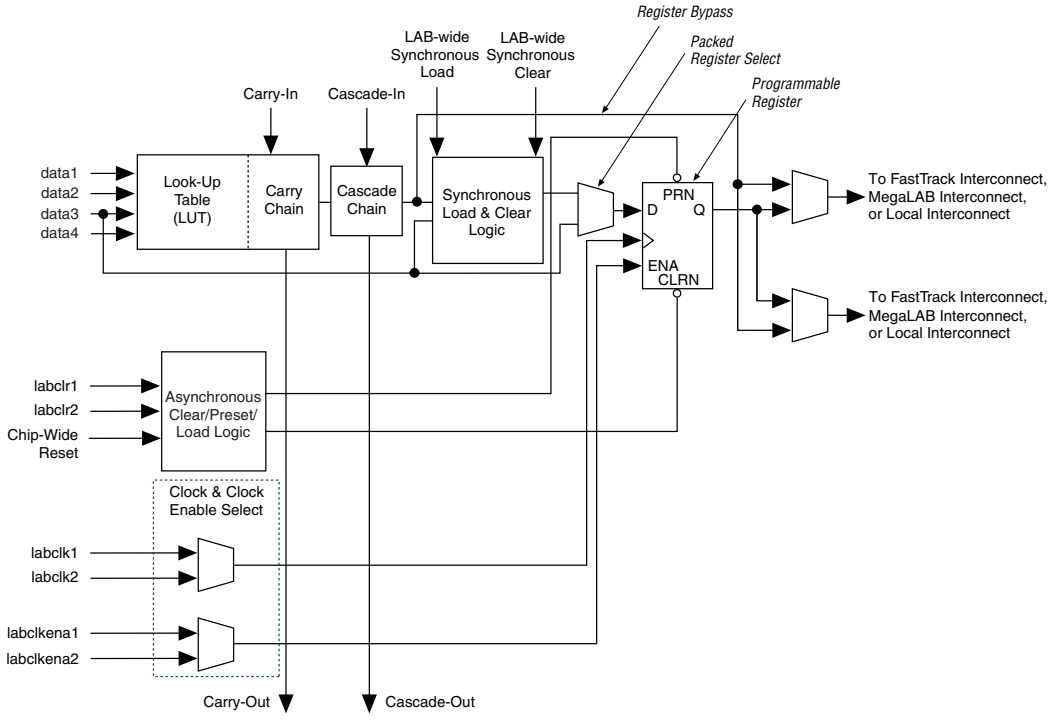
The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20KC devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20KC architecture.

## Functional Description

APEX 20KC devices incorporate LUT-based logic, product-term-based logic, and memory into one device on an all-copper technology process. Signal interconnections within APEX 20KC devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KC devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

*Figure 5. APEX 20KC Logic Element*




Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

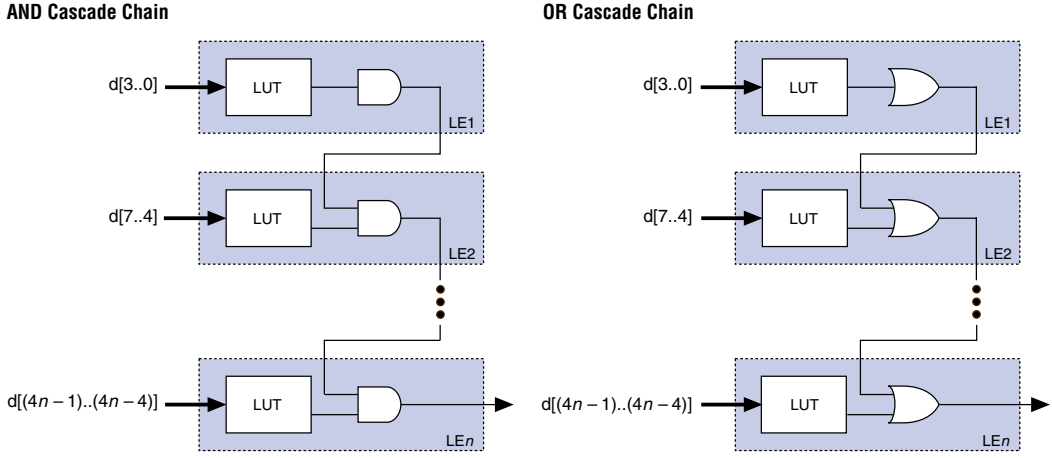
Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

### *Cascade Chain*

With the cascade chain, the APEX 20KC architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

***Figure 7. APEX 20KC Cascade Chain***



### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

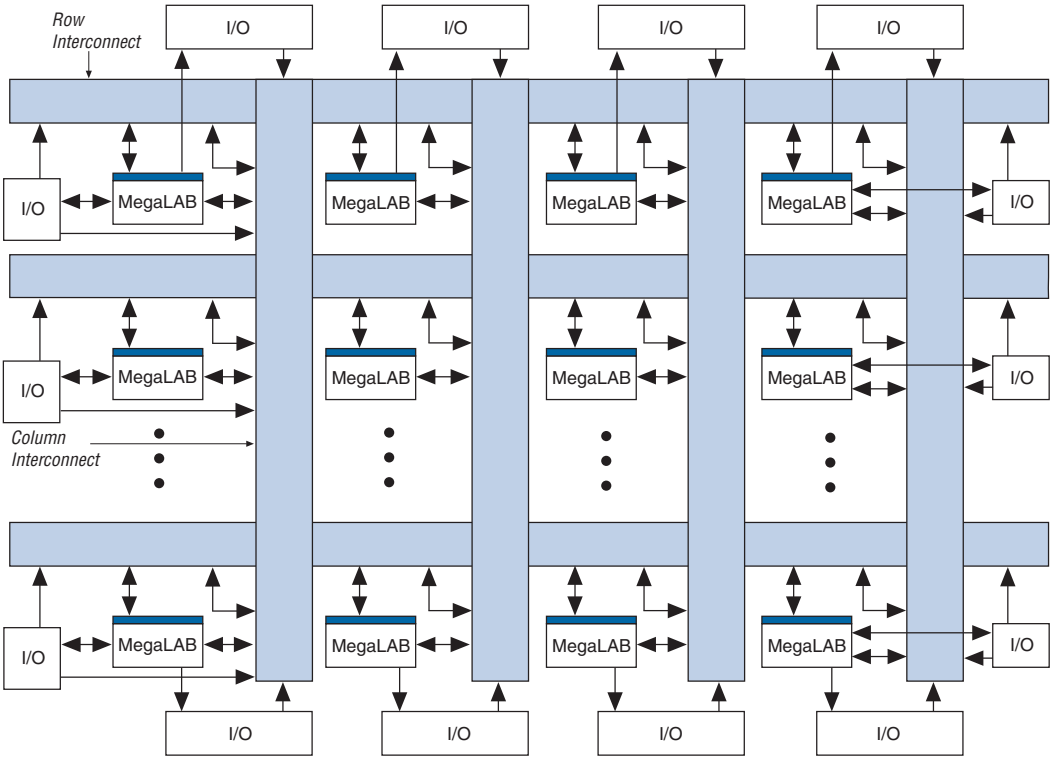
The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

*Figure 9. APEX 20KC Interconnect Structure*



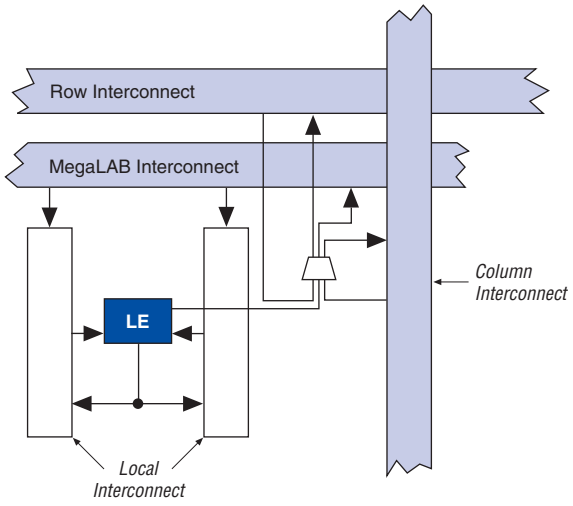

A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

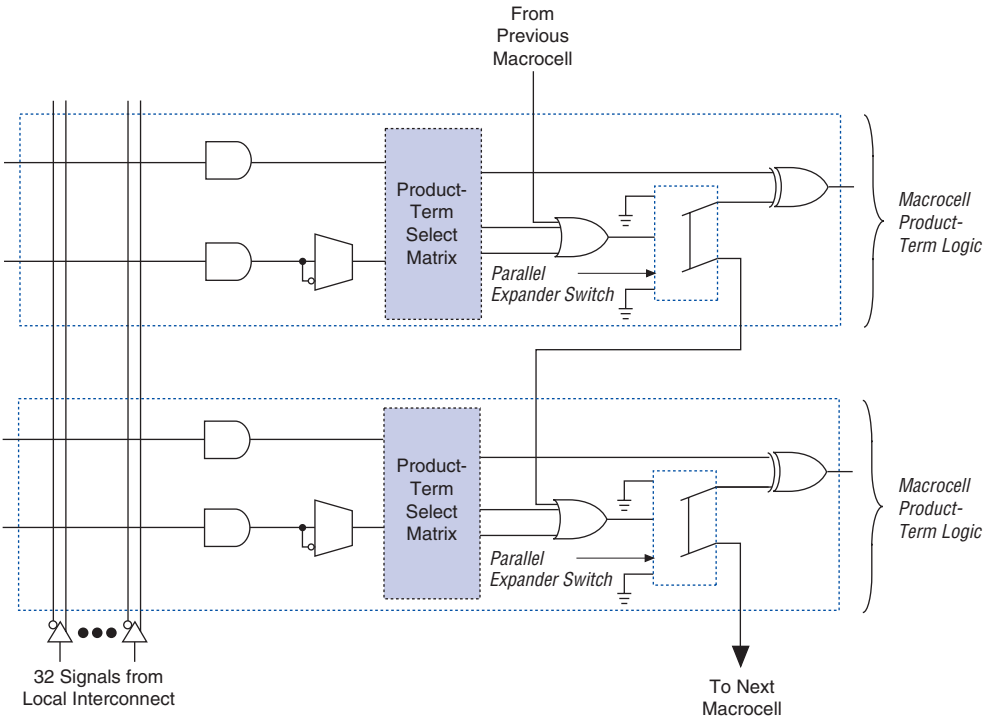
Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

*Figure 11. Driving the FastTrack Interconnect*




APEX 20KC devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. The FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K400C and larger devices, the FastRow interconnect drives the two MegaLAB structures in the top left corner, the two MegaLAB structures in the two right corner, the two MegaLAB structures in the bottom left corner, and the two MegaLAB structures in the bottom right corner. On EP20K200C and smaller devices, FastRow interconnect drives the two MegaLAB structures on the top and the two MegaLAB structures on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLAB structures except the end local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

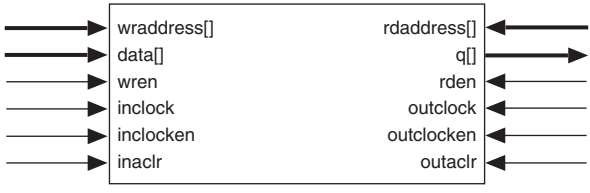
*Figure 16. APEX 20KC Parallel Expanders*




## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

*Figure 17. ESB Block Diagram*



ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the FastTrack or MegaLAB interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the FastTrack and MegaLAB interconnects. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

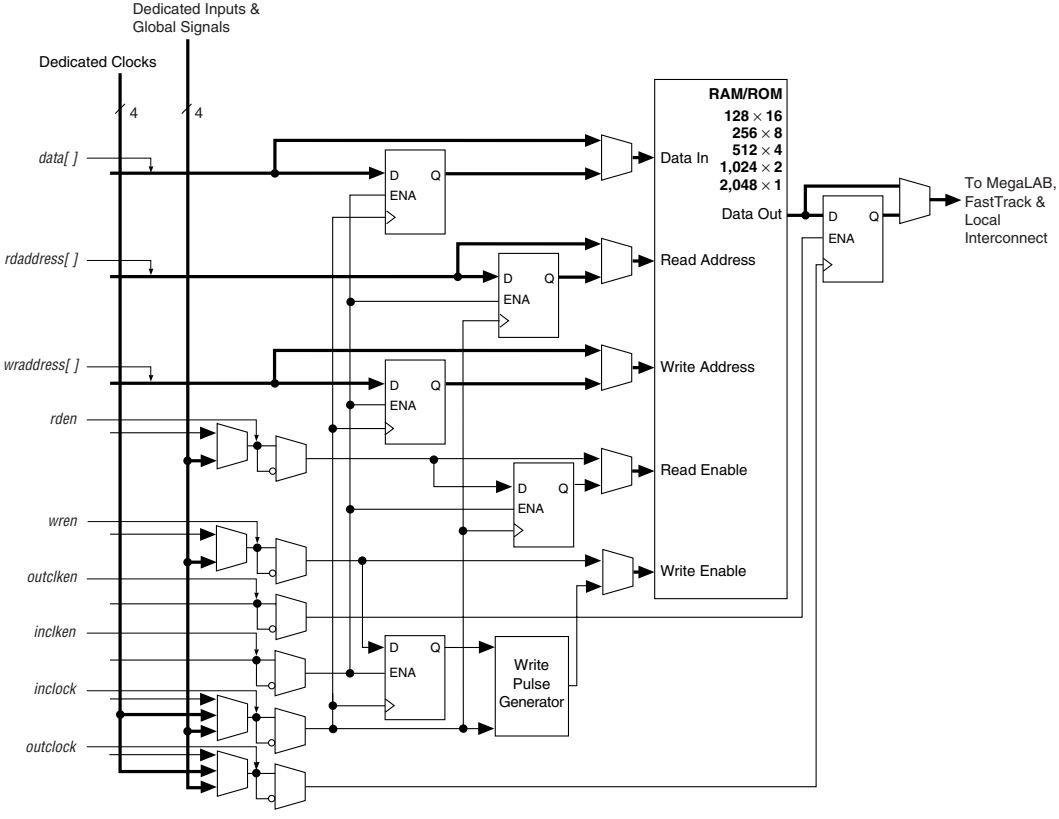
When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

***Figure 21. ESB in Input/Output Clock Mode*** *Note (1)*



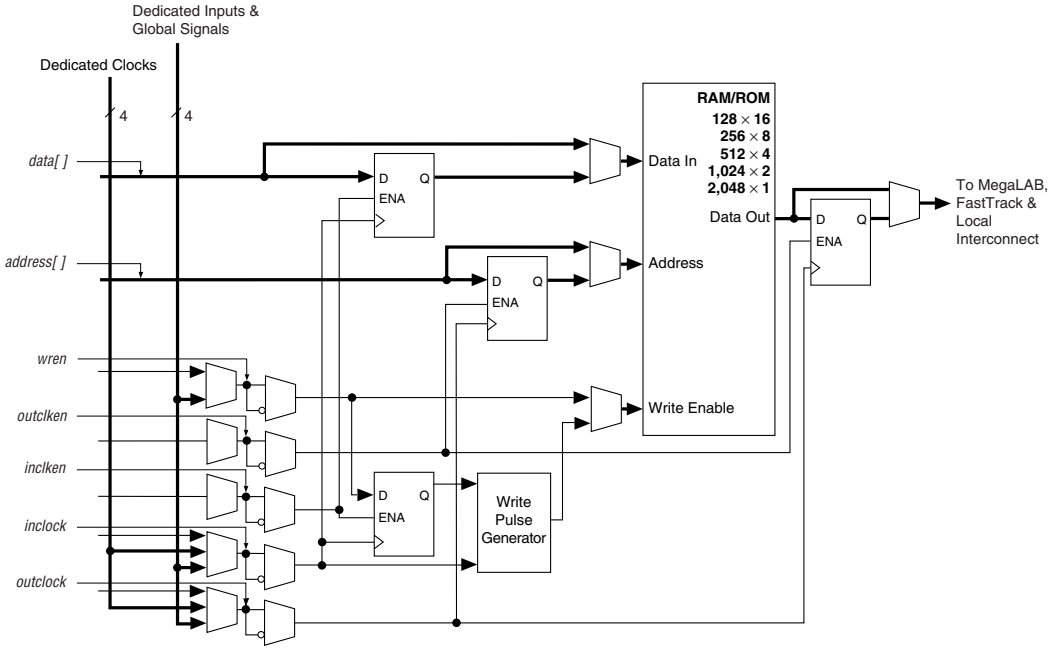

*Note to Figure 21:*

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

## Single-Port Mode

The APEX 20KC ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

*Figure 22. ESB in Single-Port Mode* *Note (1)*




*Note to Figure 22:*

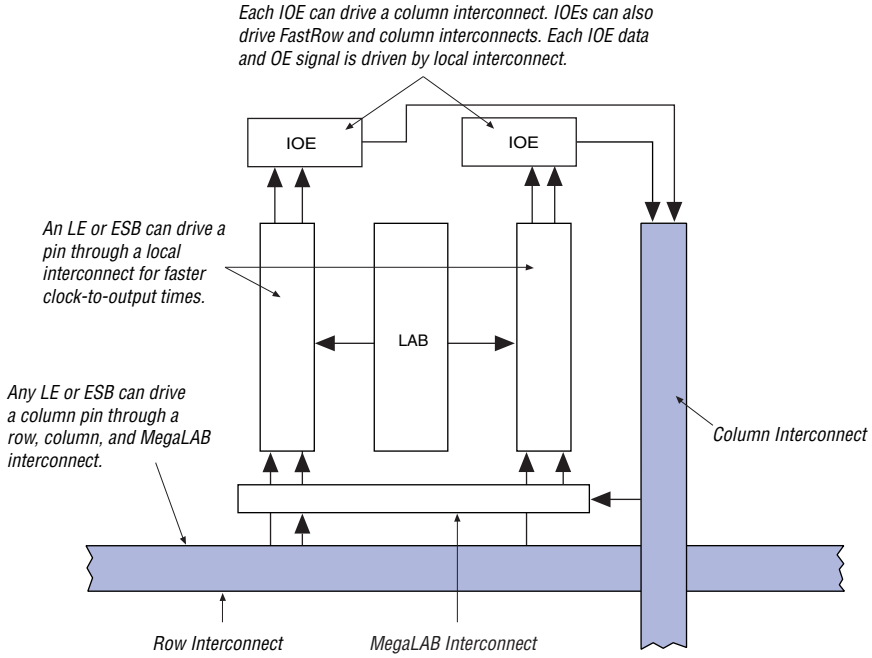
(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

## Content-Addressable Memory

In APEX 20KC devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

Figure 27 shows how a column IOE connects to the interconnect.

*Figure 27. Column IOE Connection to the Interconnect*




## Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Open-drain output pins on APEX 20KC devices (with a series resistor and a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

## ClockLock & ClockBoost Features

APEX 20KC devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20KC devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20KC device's high-speed clock to provide significant improvements in system performance and bandwidth. APEX 20KC devices in -7 and -8 speed grades have PLLs and support the ClockLock and ClockBoost features.

The ClockLock and ClockBoost features in APEX 20KC devices are enabled through the Quartus II software. External devices are not required to use these features.

### APEX 20KC ClockLock Feature

APEX 20KC devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200C devices have two PLLs; the EP20K400C and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KC PLLs.

#### *External PLL Feedback*

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KC device and another high-speed device, such as SDRAM.

*Figure 30. APEX 20KC JTAG Waveforms*

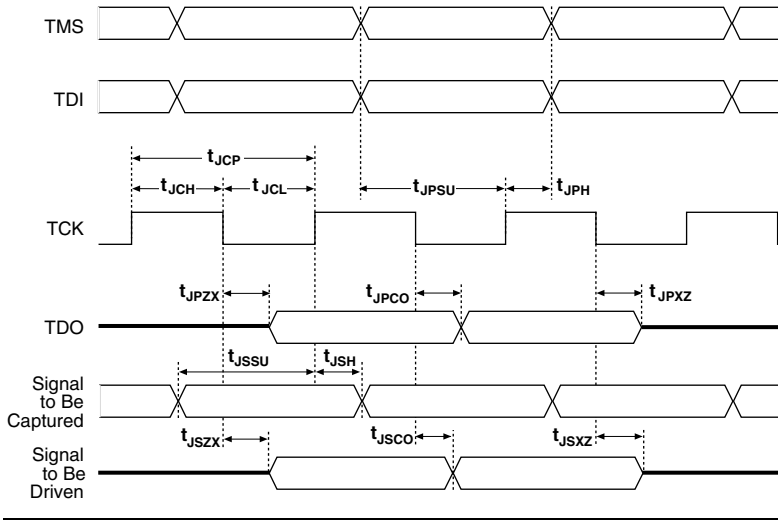



Table 16 shows the JTAG timing parameters and values for APEX 20KC devices.

*Table 16. APEX 20KC JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*

- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20KC device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20KC devices are made under conditions equivalent to those defined in the "Timing Model" section on page 65. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

## Operating Conditions

Tables 17 through 20 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KC devices.

*Table 17. APEX 20KC Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 2.5 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Table 22. LVCMOS I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Power supply voltage range | | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.8 | V |
| $I_I$ | Input pin leakage current | $V_{IN}$ = 0 V or 3.3 V | –10 | 10 | µA |
| $V_{OH}$ | High-level output voltage | $V_{CCIO}$ = 3.0 V<br>$I_{OH}$ = –0.1 mA *(1)* | $V_{CCIO}$ – 0.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CCIO}$ = 3.0 V<br>$I_{OL}$ = 0.1 mA *(2)* | | 0.2 | V |

*Table 23. 2.5-V I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.625 | V |
| $V_{IH}$ | High-level input voltage | | 1.7 | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.8 | V |
| $I_I$ | Input pin leakage current | $V_{IN}$ = 0 V or 3.3 V | –10 | 10 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –0.1 mA *(1)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA *(1)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA *(1)* | 1.7 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 0.1 mA *(2)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA *(2)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA *(2)* | | 0.7 | V |

*Table 28. GTL+ I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Termination voltage | | 1.35 | 1.5 | 1.65 | V |
| $V_{REF}$ | Reference voltage | | 0.88 | 1.0 | 1.12 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF}$ – 0.1 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 36 mA *(2)* | | | 0.65 | V |

*Table 29. SSTL-2 Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.15 | 1.25 | 1.35 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.18 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.18 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –7.6 mA *(1)* | $V_{TT}$ + 0.57 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 7.6 mA *(2)* | | | $V_{TT}$ – 0.57 | V |

*Table 46. EP20K200C $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.15 | | 0.17 | | 0.20 | ns |
| $t_{F5-20}$ | | 0.81 | | 0.94 | | 1.12 | ns |
| $t_{F20+}$ | | 0.98 | | 1.13 | | 1.35 | ns |

*Table 47. EP20K200C Minimum Pulse Width Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBCL}$ | 1.33 | | 1.66 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.05 | | 1.28 | | 1.44 | | ns |
| $t_{ESBRP}$ | 0.87 | | 1.06 | | 1.19 | | ns |

*Table 48. EP20K200C External Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.23 | | 1.26 | | 1.33 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 3.79 | 2.00 | 4.31 | 2.00 | 4.70 | ns |
| $t_{INSUPLL}$ | 0.81 | | 0.92 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.36 | 0.50 | 2.62 | - | - | ns |

*Table 51. EP20K400C $f_{MAX}$ ESB Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.30 | | 1.51 | | 1.69 | ns |
| $t_{ESBSRC}$ | | 2.35 | | 2.49 | | 2.72 | ns |
| $t_{ESBAWC}$ | | 2.92 | | 3.46 | | 3.86 | ns |
| $t_{ESBSWC}$ | | 3.05 | | 3.44 | | 3.85 | ns |
| $t_{ESBWASU}$ | 0.45 | | 0.50 | | 0.54 | | ns |
| $t_{ESBWAH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.57 | | 0.63 | | 0.68 | | ns |
| $t_{ESBWDH}$ | 0.44 | | 0.50 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.25 | | 1.43 | | 1.56 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.03 | | 0.11 | | ns |
| $t_{ESBWESU}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 2.01 | | 2.27 | | 2.45 | | ns |
| $t_{ESBWADDRSU}$ | –0.20 | | –0.24 | | –0.28 | | ns |
| $t_{ESBRADDRSU}$ | 0.02 | | 0.00 | | –0.02 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.28 | | 1.43 | ns |
| $t_{ESBDATACO2}$ | | 2.10 | | 2.52 | | 2.82 | ns |
| $t_{ESBDD}$ | | 2.50 | | 2.97 | | 3.32 | ns |
| $t_{PD}$ | | 1.48 | | 1.78 | | 2.00 | ns |
| $t_{PTERMSU}$ | 0.58 | | 0.72 | | 0.81 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.29 | | 1.45 | ns |

*Table 52. EP20K400C $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.15 | | 0.17 | | 0.19 | ns |
| $t_{F5-20}$ | | 0.94 | | 1.06 | | 1.25 | ns |
| $t_{F20+}$ | | 1.73 | | 1.96 | | 2.30 | ns |

*Table 63. EP20K1000C $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.48 | | 1.57 | | 1.65 | ns |
| $t_{ESBSRC}$ | | 2.36 | | 2.50 | | 2.73 | ns |
| $t_{ESBAWC}$ | | 2.93 | | 3.46 | | 3.86 | ns |
| $t_{ESBSWC}$ | | 3.08 | | 3.43 | | 3.83 | ns |
| $t_{ESBWASU}$ | 0.51 | | 0.50 | | 0.52 | | ns |
| $t_{ESBWAH}$ | 0.38 | | 0.51 | | 0.57 | | ns |
| $t_{ESBWDSU}$ | 0.62 | | 0.62 | | 0.66 | | ns |
| $t_{ESBWDH}$ | 0.38 | | 0.51 | | 0.57 | | ns |
| $t_{ESBRASU}$ | 1.40 | | 1.47 | | 1.53 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.07 | | 0.18 | | ns |
| $t_{ESBWESU}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 1.92 | | 2.19 | | 2.35 | | ns |
| $t_{ESBWADDRSU}$ | –0.20 | | –0.28 | | –0.32 | | ns |
| $t_{ESBRADDRSU}$ | 0.00 | | –0.03 | | –0.05 | | ns |
| $t_{ESBDATACO1}$ | | 1.12 | | 1.30 | | 1.46 | ns |
| $t_{ESBDATACO2}$ | | 2.11 | | 2.53 | | 2.84 | ns |
| $t_{ESBDD}$ | | 2.56 | | 2.96 | | 3.30 | ns |
| $t_{PD}$ | | 1.49 | | 1.79 | | 2.02 | ns |
| $t_{PTERMSU}$ | 0.61 | | 0.69 | | 0.77 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.32 | | 1.48 | ns |

*Table 64. EP20K1000C $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.15 | | 0.17 | | 0.19 | ns |
| $t_{F5-20}$ | | 1.13 | | 1.31 | | 1.50 | ns |
| $t_{F20+}$ | | 2.30 | | 2.71 | | 3.19 | ns |

*Table 67. EP20K1000C External Bidirectional Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.86 | | 2.54 | | 3.15 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.63 | 2.00 | 5.26 | 2.00 | 5.69 | ns |
| $t_{XZBIDIR}$ | | 8.98 | | 9.89 | | 10.67 | ns |
| $t_{ZXBIDIR}$ | | 8.98 | | 9.89 | | 10.67 | ns |
| $t_{INSUBIDIRPLL}$ | 4.17 | | 5.27 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.32 | 0.50 | 2.55 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 6.67 | | 7.18 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 6.67 | | 7.18 | | - | ns |

Tables 68 and 69 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

*Table 68. Selectable I/O Standard Input Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.00 | | 0.00 | ns |
| 1.8 V | | 0.04 | | 0.11 | | 0.14 | ns |
| PCI | | 0.00 | | 0.04 | | 0.03 | ns |
| GTL+ | | –0.30 | | 0.25 | | 0.23 | ns |
| SSTL-3 Class I | | –0.19 | | –0.13 | | –0.13 | ns |
| SSTL-3 Class II | | –0.19 | | –0.13 | | –0.13 | ns |
| SSTL-2 Class I | | –0.19 | | –0.13 | | –0.13 | ns |
| SSTL-2 Class II | | –0.19 | | –0.13 | | –0.13 | ns |
| LVDS | | –0.19 | | –0.17 | | –0.16 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| AGP | | 0.00 | | 0.00 | | 0.00 | ns |