Infineon Technologies - SAF-XC161CS-32F20F BB-A Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	99
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc161cs-32f20f-bb-a

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Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P2		IO	Port 2 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 2 is selectable (standard or special). The following Port 2 pins also serve for alternate functions:
P2.8	49	I/O I	CC8IO CAPCOM1: CC8 Capture Inp./Compare Output, EX0IN Fast External Interrupt 0 Input (default pin)
P2.9	50	I/O I	CC9IO CAPCOM1: CC9 Capture Inp./Compare Output, EX1IN Fast External Interrupt 1 Input (default pin)
P2.10	51	I/O I	CC10IO CAPCOM1: CC10 Capture Inp./Compare Outp., EX2IN Fast External Interrupt 2 Input (default pin)
P2.11	52	I/O I	CC11IO CAPCOM1: CC11 Capture Inp./Compare Outp., EX3IN Fast External Interrupt 3 Input (default pin)
P2.12	53	I/O I	CC12IO CAPCOM1: CC12 Capture Inp./Compare Outp., EX4IN Fast External Interrupt 4 Input (default pin)
P2.13	54	I/O I	CC13IO CAPCOM1: CC13 Capture Inp./Compare Outp., EX5IN Fast External Interrupt 5 Input (default pin)
P2.14	55	I/O I	CC14IO CAPCOM1: CC14 Capture Inp./Compare Outp., EX6IN Fast External Interrupt 6 Input (default pin)
P2.15	56	I/O I I	CC15IO CAPCOM1: CC15 Capture Inp./Compare Outp., EX7IN Fast External Interrupt 7 Input (default pin), T7IN CAPCOM2: Timer T7 Count Input
$\overline{\text{TRST}}$	57	I	$\overline{\text{T}}$est-System Reset Input. For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{RSTIN}}$ activates the XC164CM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
PORT0 P0L.0 - P0L.7, P0H.0, P0H.1, P0H.2 - P0H.7	 95 - 102, 105, 106, 111 - 116	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. Each pin can be programmed for input (output driver in high-impedance state) or output. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0 *Note: At the end of an external reset ($\overline{EA}$ = 0) PORT0 also may input configuration values.*
PORT1 P1L.0 - P1L.6 P1L.7 P1H.0 P1H.1 P1H.2 P1H.3 P1H.4 P1H.5 P1H.6 P1H.7	 117 - 123 124 127 128 129 130 131 132 133 134	IO O I/O I/O I I/O I/O I/O I I/O I/O I/O I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions: (A0-6) Address output only CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp. CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp., EX0IN Fast External Interrupt 0 Input (alternate pin B) MRST1 SSC1 Master-Receive/Slave-Transmit In/Outp. MTSR1 SSC1 Master-Transmit/Slave-Receive Out/Inp. SCLK1 SSC1 Master Clock Output/Slave Clock Input, EX0IN Fast External Interrupt 0 Input (alternate pin A) CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp. CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp. CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp. CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	137 138	O I	XTAL2: Output of the main oscillator amplifier circuit XTAL1: Input to the main oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
XTAL3 XTAL4	140 141	I O	XTAL3: Input to the auxiliary (32-kHz) oscillator amplifier XTAL4: Output of the auxiliary (32-kHz) oscillator amplifier circuit To clock the device from an external source, drive XTAL3, while leaving XTAL4 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL3 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
$\overline{\text{RSTIN}}$	142	I	Reset Input with Schmitt-Trigger characteristics. A low-level at this pin while the oscillator is running resets the XC161. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle.* *External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
$\overline{\text{BRK OUT}}$	143	O	Debug System: Break Out
$\overline{\text{BRKIN}}$	144	I	Debug System: Break In
NC	1, 2, 107 - 110	–	No connection. It is recommended not to connect these pins to the PCB.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
V_{AREF}	41	–	Reference voltage for the A/D converter.
V_{AGND}	42	–	Reference ground for the A/D converter.
V_{DDI}	48, 78, 135	–	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the **Operating Conditions**.
V_{DDP}	6, 20, 28, 58, 88, 103, 125	–	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the **Operating Conditions**.
V_{SSI}	47, 79, 136, 139	–	**Digital Ground** Connect decoupling capacitors to adjacent V_{DD}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.
V_{SSP}	5, 19, 27, 35, 36, 37, 38, 89, 104, 126	–	

1) The CAN interface lines are assigned to ports P4, P7, and P9 under software control.

3 Functional Description

The architecture of the XC161 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC161.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC161.

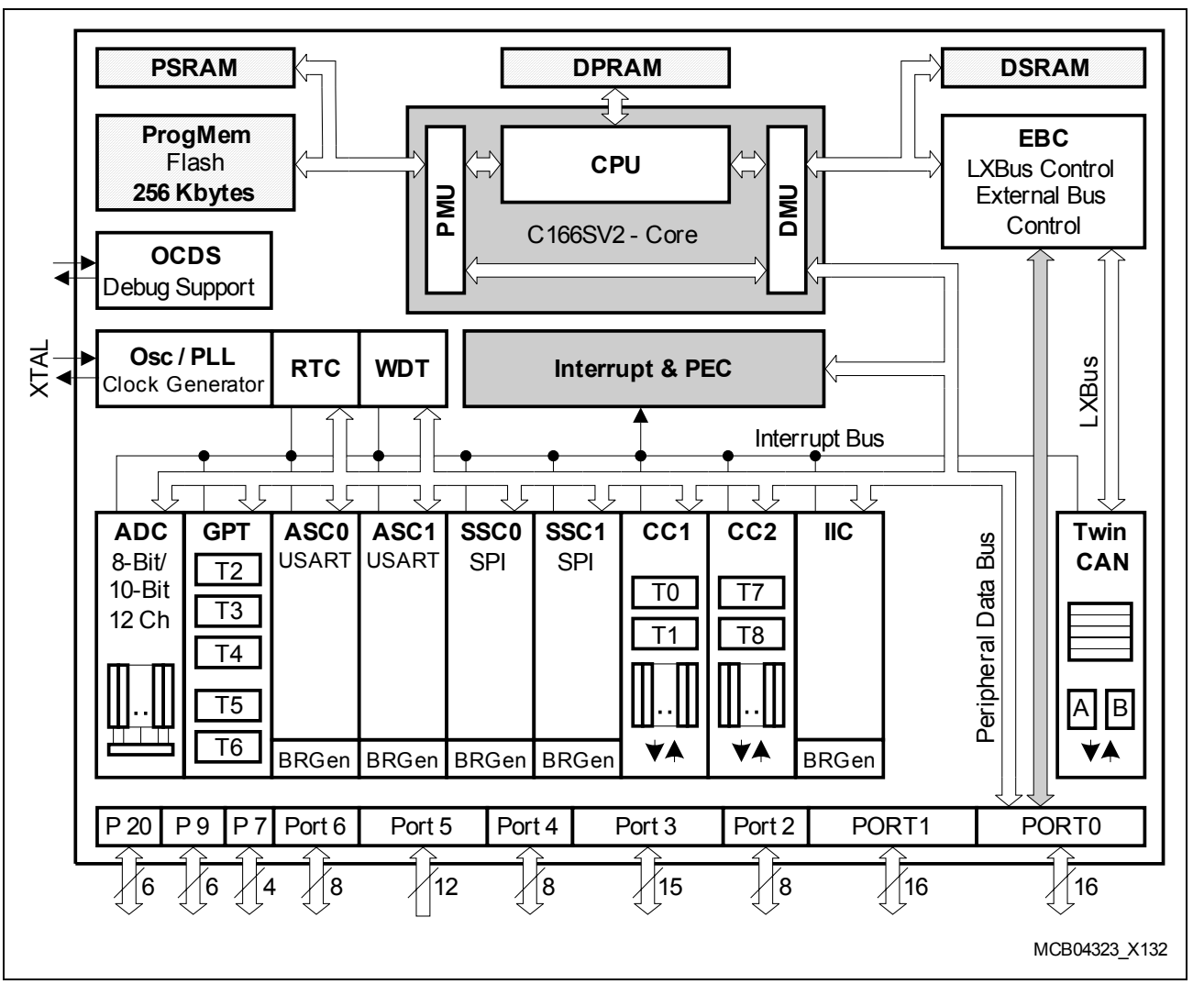

Figure 3 Block Diagram

4) The Emulation PSRAM (EPSRAM) realizes a 2nd access path to the PSRAM with a different timing.

5) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes[1)], which are as follows:

- 16 … 24-bit Addresses, 16-bit Data, Demultiplexed
- 16 … 24-bit Addresses, 16-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output. The high order address (segment) lines use Port 4. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines are assigned to Port 4.

Up to 5 external $\overline{\text{CS}}$ signals (4 windows plus default) can be generated in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Access to very slow memories or modules with varying access times is supported via a particular ‘Ready’ function. The active level of the control input signal is selectable.

A $\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ protocol is available for bus arbitration and allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software. After enabling, pins P6.7 … P6.5 ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{\text{HLDA}}$ pin is an output. In Slave Mode pin $\overline{\text{HLDA}}$ is switched to input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

The EBC also controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.

3.6 Capture/Compare Units (CAPCOM1/2)

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for each capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function.
All registers of each module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Table 6 Compare Modes (CAPCOM1/2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; can be used with any compare mode

3.7 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

3.12 TwinCAN Module

The integrated TwinCAN module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip TwinCAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Two Full-CAN nodes share the TwinCAN module's resources to optimize the CAN bus traffic handling and to minimize the CPU load. The module provides up to 32 message objects, which can be assigned to one of the CAN nodes and can be combined to FIFO-structures. Each object provides separate masks for acceptance filtering.

The flexible combination of Full-CAN functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the number of message objects permit precise and comfortable CAN bus traffic handling.

Gateway functionality allows automatic data exchange between two separate CAN bus systems, which reduces CPU load and improves the real time behavior of the entire system.

The bit timing for both CAN nodes is derived from the master clock and is programmable up to a data rate of 1 Mbit/s. Each CAN node uses two pins of Port 4, Port 7, or Port 9 to interface to an external bus transceiver. The interface pins are assigned via software.

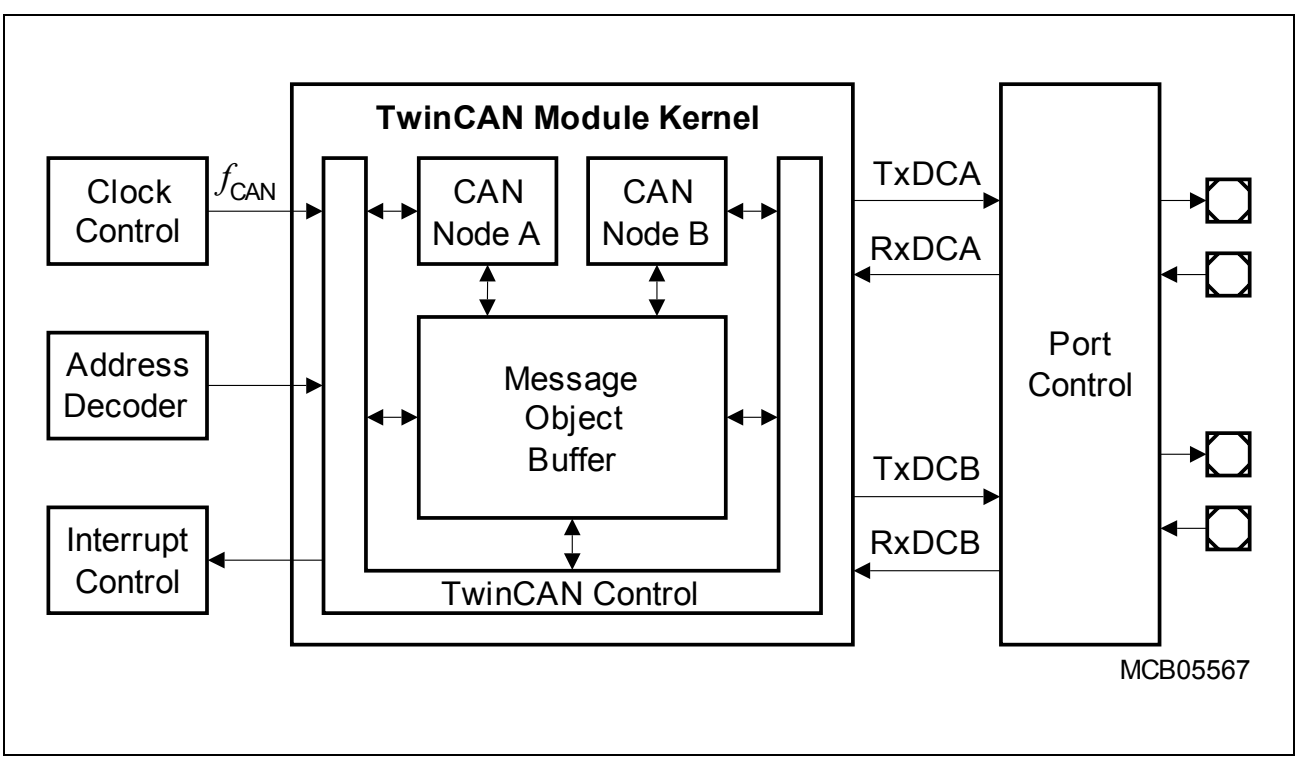

Figure 9 TwinCAN Module Block Diagram

Table 7 Summary of the XC161's Parallel Ports

Port	Control	Alternate Functions
PORT0	Pad drivers	Address/Data lines or data lines[1)]
PORT1	Pad drivers	Address lines[2)]
		Capture inputs or compare outputs, Serial interface lines
Port 2	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs, Timer control signal, Fast external interrupt inputs
Port 3	Pad drivers, Open drain, Input threshold	Timer control signals, serial interface lines, Optional bus control signal $\overline{BHE}$/$\overline{WRH}$, System clock output CLKOUT (or FOUT)
Port 4	Pad drivers, Open drain, Input threshold	Segment address lines[3)]
		CAN interface lines[4)]
Port 5	–	Analog input channels to the A/D converter, Timer control signals
Port 6	Open drain, Input threshold	Capture inputs or compare outputs, Bus arbitration signals $\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$, Optional chip select signals
Port 7	Open drain, Input threshold	Capture inputs or compare outputs, CAN interface lines[4)]
Port 9	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs
		CAN interface lines[4)], IIC bus interface lines[4)]
Port 20	Pad drivers, Open drain	Bus control signals $\overline{RD}$, $\overline{WR}$/$\overline{WRL}$, READY, ALE, External access enable pin $\overline{EA}$, Reset indication output $\overline{RSTOUT}$

1) For multiplexed bus cycles.

2) For demultiplexed bus cycles.

3) For more than 64 Kbytes of external resources.

4) Can be assigned by software.

3.18 Instruction Set Summary

Table 8 lists the instructions of the XC161 in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

4.2 DC Parameters

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1, XTAL3)	V_{IL}	SR	-0.5	$0.2 \times V_{DDP}$ - 0.1	V	–
Input low voltage for XTAL1, XTAL3[2)3)]	V_{ILC}	SR	-0.5	$0.3 \times V_{DDI}$	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	$0.45 \times V_{DDP}$	V	[4)]
Input high voltage TTL (all except XTAL1, XTAL3)	V_{IH}	SR	$0.2 \times V_{DDP}$ + 0.9	V_{DDP} + 0.5	V	–
Input high voltage XTAL1, XTAL3[2)3)]	V_{IHC}	SR	$0.7 \times V_{DDI}$	V_{DDI} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	$0.8 \times V_{DDP}$ - 0.2	V_{DDP} + 0.5	V	[4)]
Input Hysteresis (Special Threshold)	HYS		$0.04 \times V_{DDP}$	–	V	V_{DDP} in [V], Series resistance = 0 Ω[4)]
Output low voltage	V_{OL}	CC	–	1.0	V	$I_{OL} \le I_{OLmax}$[5)]
			–	0.45	V	$I_{OL} \le I_{OLnom}$[5)6)]
Output high voltage[7)]	V_{OH}	CC	V_{DDP} - 1.0	–	V	$I_{OH} \ge I_{OHmax}$[5)]
			V_{DDP} - 0.45	–	V	$I_{OH} \ge I_{OHnom}$[5)6)]
Input leakage current (Port 5)[8)]	I_{OZ1}	CC	–	±300	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 125$ °C
				±200	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 85$ °C[15)]
Input leakage current (all other[9)])[8)]	I_{OZ2}	CC	–	±500	nA	$0.45\ V < V_{IN} < V_{DDP}$
Configuration pull-up current[10)]	I_{CPUH}[11)]		–	-10	µA	$V_{IN} = V_{IHmin}$
	I_{CPUL}[12)]		-100	–	µA	$V_{IN} = V_{ILmax}$

3) The pad supply voltage pins (V_{DDP}) mainly provide the current consumed by the pin output drivers. This output driver current is not covered by parameter I_{DDP}. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.
4) The total supply current in Sleep and Power down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator or auxiliary oscillator (if active).
5) This parameter is determined mainly by the transistor leakage currents. This current heavily depends on the junction temperature (see **Figure 12**). The junction temperature T_J is the same as the ambient temperature T_A if no current flows through the port output drivers. Otherwise, the resulting temperature difference must be taken into account.
6) All inputs (including JTAG pins and pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.
7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 11**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = PLLODIV+1) to generate the master clock signal f_{MC}. Therefore, the number of VCO cycles can be represented as K × **N**, where **N** is the number of consecutive f_{MC} cycles (TCM).

For a period of **N** × TCM the accumulated PLL jitter is defined by the deviation D_N:

D_N [ns] = ±(1.5 + 6.32 × **N** / f_{MC}); f_{MC} in [MHz], **N** = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: D_3 = ±(1.5 + 6.32 × **3** / 20) = 2.448 ns.

This formula is applicable for K × **N** < 95. For longer periods the K × **N** = 95 value can be used. This steady value can be approximated by: D_{Nmax} [ns] = ±(1.5 + 600 / (K × f_{MC})).

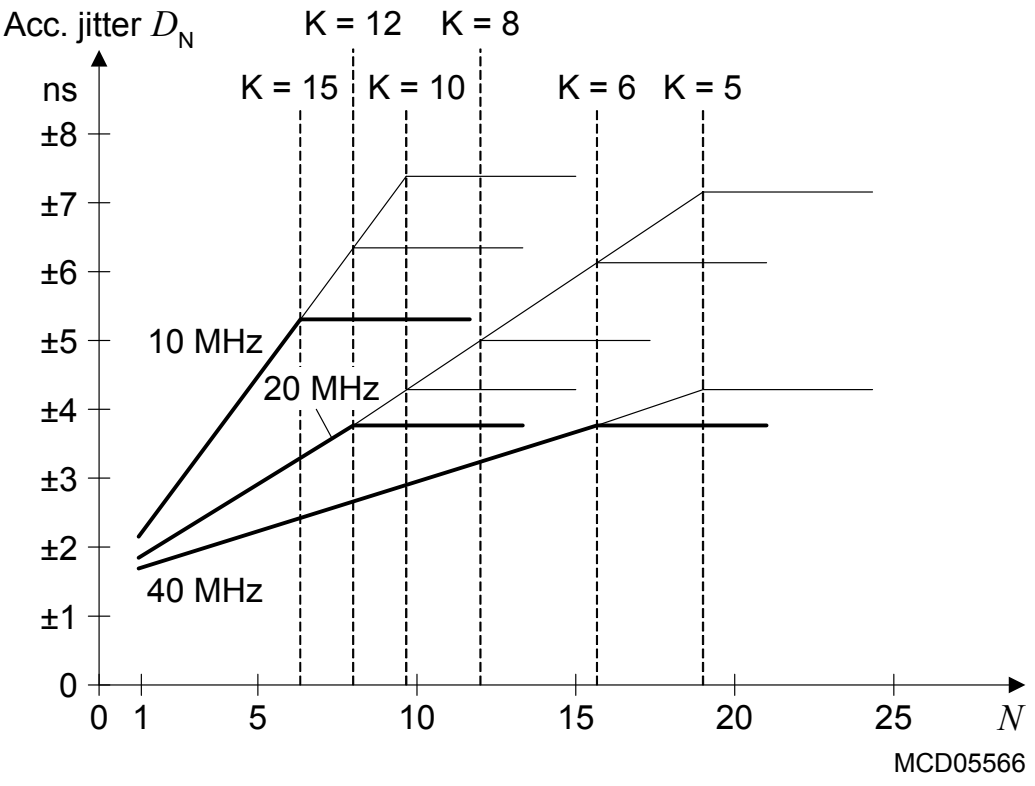

Figure 15 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 22 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			Min.	Max.	
Output valid delay for: RD, WR(L/H)	tc_{10}	CC	1	15	ns
Output valid delay for: BHE, ALE	tc_{11}	CC	-1	8	ns
Output valid delay for: A23 … A16, A15 … A0 (on PORT1)	tc_{12}	CC	3	18	ns
Output valid delay for: A15 … A0 (on PORT0)	tc_{13}	CC	3	18	ns
Output valid delay for: CS	tc_{14}	CC	3	16	ns
Output valid delay for: D15 … D0 (write data, MUX-mode)	tc_{15}	CC	3	19	ns
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	tc_{16}	CC	2	16	ns
Output hold time for: RD, WR(L/H)	tc_{20}	CC	-3	4	ns
Output hold time for: BHE, ALE	tc_{21}	CC	0	11	ns
Output hold time for: A23 … A16, A15 … A0 (on PORT0)	tc_{23}	CC	1	13	ns
Output hold time for: CS	tc_{24}	CC	-2	4	ns
Output hold time for: D15 … D0 (write data)	tc_{25}	CC	1	13	ns
Input setup time for: READY, D15 … D0 (read data)	tc_{30}	SR	29	–	ns
Input hold time READY, D15 … D0 (read data)[1)]	tc_{31}	SR	-5	–	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can be removed after the rising edge of RD.

Note: The shaded parameters have been verified by characterization. They are not subject to production test.

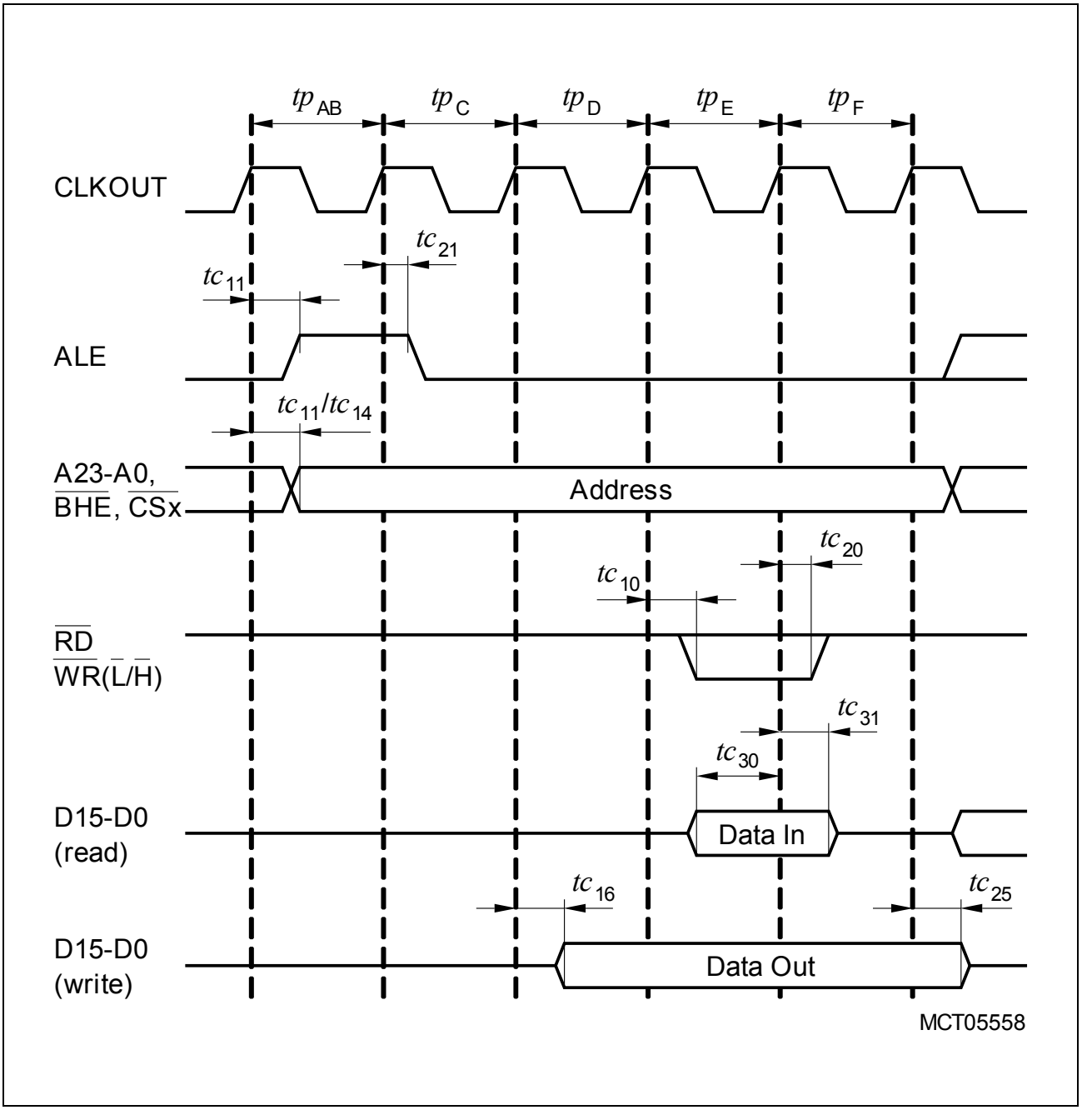

Figure 21 Demultiplexed Bus Cycle

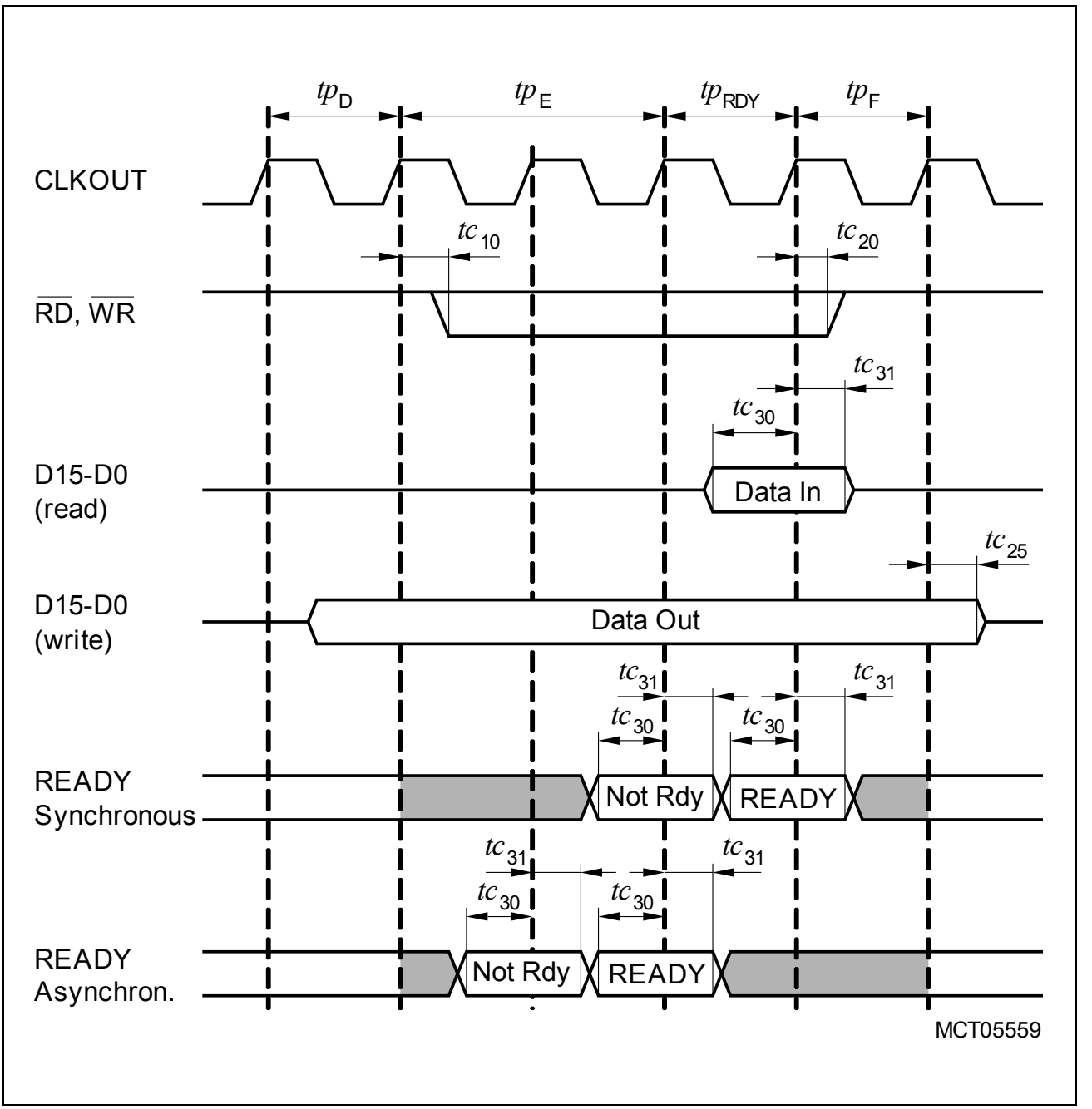

Figure 22 READY Timing

Note: If the READY input is sampled inactive at the indicated sampling point (“Not Rdy”) a READY-controlled waitstate is inserted (tp_{RDY}), sampling the READY input active at the indicated sampling point (“Ready”) terminates the currently running bus cycle.
Note the different sampling points for synchronous and asynchronous READY.
This example uses one mandatory waitstate (see tp_E) before the READY input is evaluated.

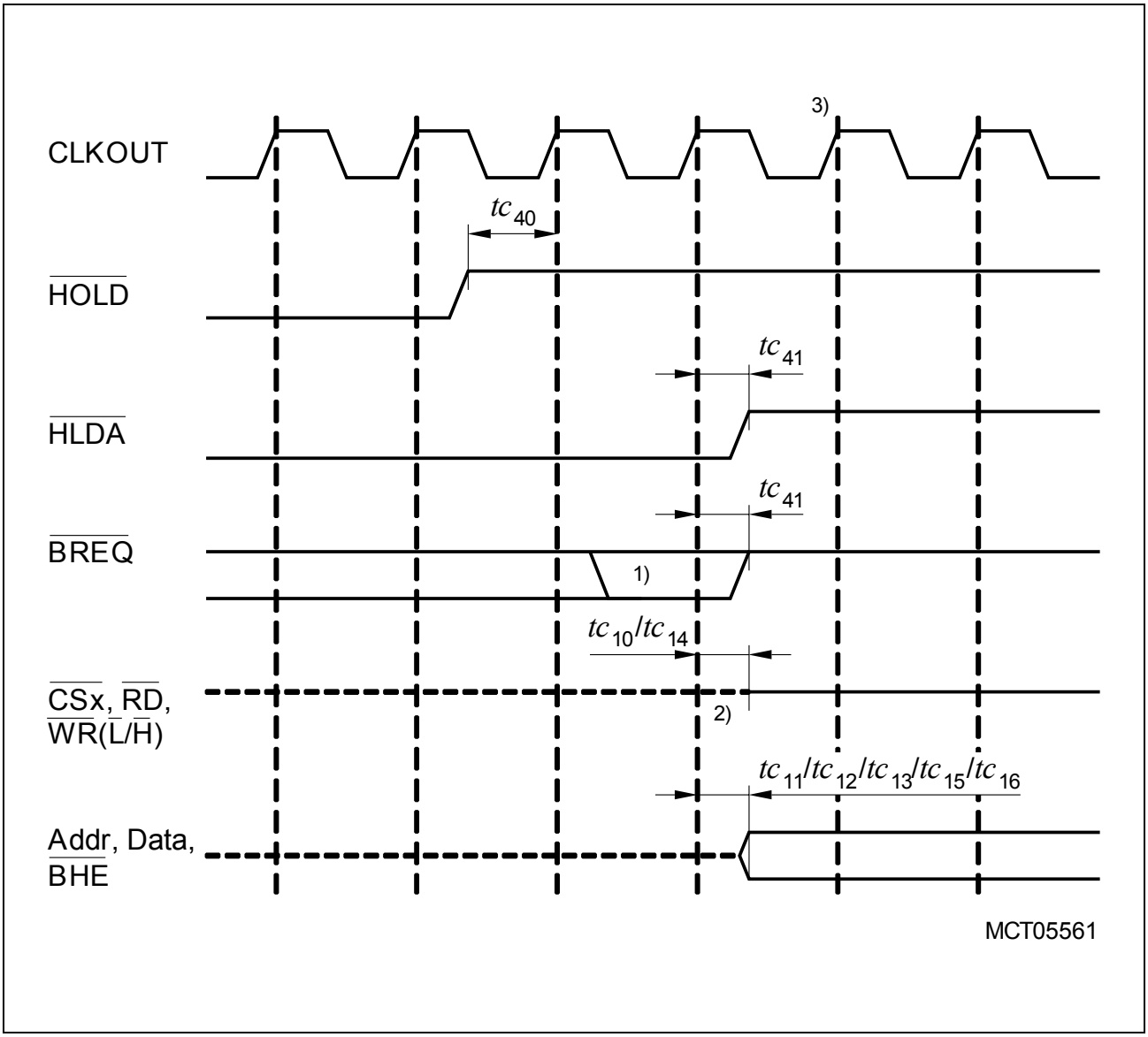

Figure 24 External Bus Arbitration, Regaining the Bus

Notes

1. *This is the last chance for BREQ to trigger the indicated regain-sequence. Even if BREQ is activated earlier, the regain-sequence is initiated by HOLD going high. Please note that HOLD may also be deactivated without the XC161 requesting the bus.*
2. *The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).*
3. *The next XC161 driven bus cycle may start here.*