Infineon Technologies - SAK-XC161CS-32F20F BB-A Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	99
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc161cs-32f20f-bb-a

XC161
Revision History: V1.2, 2006-08

Previous Version(s):
V1.1, 2005-06
V1.0, 2004-11

Page	Subjects (major changes since last revision)
12	Description of the $\overline{\text{TRST}}$ signal modified.
17	Footnote added about pins XTAL1/XTAL3 belonging to V_{DDI} power domain.
21	Emulation Program SRAM (EPSRAM) introduced in the memory map.
50	Instructions Set Summary improved.
57	Footnote added about amplitude at XTAL1 pin.
82	Green package added.
82	Thermal Resistance: R_{THA} replaced by $R_{\Theta JC}$ and $R_{\Theta JL}$ because R_{THA} strongly depends on the external system (PCB, environment). P_{DISS} removed, because no static parameter, but derived from thermal resistance.

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
mcdocu.comments@infineon.com

1 Summary of Features

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 × 16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with 73 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 4 Kbytes On-Chip Data SRAM (DSRAM)
  - 6 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 256 Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - 12-Channel A/D Converter with Programmable Resolution (10-bit or 8-bit) and Conversion Time (down to 2.55 µs or 2.15 µs)
  - Two 16-Channel General Purpose Capture/Compare Units (32 Input/Output Pins)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip TwinCAN Interface (Rev. 2.0B active) with 32 Message Objects (Full CAN/Basic CAN) on Two CAN Nodes, and Gateway Functionality
  - IIC Bus Interface (10-bit addressing, 400 kbit/s) with 3 Channels (multiplexed)
  - On-Chip Real Time Clock, Driven by Dedicated Oscillator
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.0	59	I	T0IN	CAPCOM1 Timer T0 Count Input,
		O	TxD1	ASC1 Clock/Data Output (Async./Sync),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin B)
P3.1	60	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A)
P3.2	61	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	62	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	63	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	64	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	65	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	66	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	67	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	68	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	69	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	70	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin A)
P3.12	75	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	76	I/O	SCLK0	SSC0 Master Clock Output/Slave Clock Input.,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	77	O	CLKOUT	Master Clock Output,
		O	FOUT	Programmable Frequency Output
TCK	71	I	Debug System: JTAG Clock Input	
TDI	72	I	Debug System: JTAG Data In	
TDO	73	O	Debug System: JTAG Data Out	
TMS	74	I	Debug System: JTAG Test Mode Selection	

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P20		IO	Port 20 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output. The input threshold of Port 20 is selectable (standard or special). The following Port 20 pins also serve for alternate functions:	
P20.0	90	O	$\overline{RD}$	External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	91	O	$\overline{WR}$/$\overline{WRL}$	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus.
P20.2	92	I	READY	READY Input. When the READY function is enabled, memory cycle time waitstates can be forced via this pin during an external access.
P20.4	93	O	ALE	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	94	I	$\overline{EA}$	External Access Enable pin. **A low-level** at this pin during and after Reset forces the XC161 to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high-level** forces the XC161 to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
P20.12	3	O	$\overline{RSTOUT}$	Internal Reset Indication Output. **Is activated** asynchronously with an external hardware reset. It may also be activated (selectable) synchronously with an internal software or watchdog reset. **Is deactivated** upon the execution of the EINIT instruction, optionally at the end of reset, or at any time (before EINIT) via user software.
			Note: Port 20 pins may input configuration values (see $\overline{EA}$).	

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
V_{AREF}	41	–	Reference voltage for the A/D converter.
V_{AGND}	42	–	Reference ground for the A/D converter.
V_{DDI}	48, 78, 135	–	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the **Operating Conditions**.
V_{DDP}	6, 20, 28, 58, 88, 103, 125	–	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the **Operating Conditions**.
V_{SSI}	47, 79, 136, 139	–	**Digital Ground** Connect decoupling capacitors to adjacent V_{DD}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.
V_{SSP}	5, 19, 27, 35, 36, 37, 38, 89, 104, 126	–	

1) The CAN interface lines are assigned to ports P4, P7, and P9 under software control.

3.1 Memory Subsystem and Organization

The memory space of the XC161 is configured in a Von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bitaddressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources, including peripherals on the LXBus (such as TwinCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

256 Kbytes of on-chip Flash memory store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors, one 32-Kbyte sector, and three 64-Kbyte sectors. Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
Programming typically takes 2 ms per 128-byte block (5 ms max.), erasing a sector typically takes 200 ms (500 ms max.).

6 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

4 Kbytes of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, and general purpose register banks. A register

1) Each two 8-Kbyte sectors are combined for write-protection purposes.

The XC161 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions: • Hardware Reset • Software Reset • Watchdog Timer Overflow	–	 RESET RESET RESET	 xx’0000$_H$ xx’0000$_H$ xx’0000$_H$	 00$_H$ 00$_H$ 00$_H$	 III III III
Class A Hardware Traps: • Non-Maskable Interrupt • Stack Overflow • Stack Underflow • Software Break	 NMI STKOF STKUF SOFTBRK	 NMITRAP STOTRAP STUTRAP SBRKTRAP	 xx’0008$_H$ xx’0010$_H$ xx’0018$_H$ xx’0020$_H$	 02$_H$ 04$_H$ 06$_H$ 08$_H$	 II II II II
Class B Hardware Traps: • Undefined Opcode • PMI Access Error • Protected Instruction Fault • Illegal Word Operand Access	 UNDOPC PACER PRTFLT ILLOPA	 BTRAP BTRAP BTRAP BTRAP	 xx’0028$_H$ xx’0028$_H$ xx’0028$_H$ xx’0028$_H$	 0A$_H$ 0A$_H$ 0A$_H$ 0A$_H$	 I I I I
Reserved	–	–	[2C$_H$ - 3C$_H$]	[0B$_H$ - 0F$_H$]	–
Software Traps • TRAP Instruction	–	–	Any [xx’0000$_H$ - xx’01FC$_H$] in steps of 4$_H$	Any [00$_H$ - 7F$_H$]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.

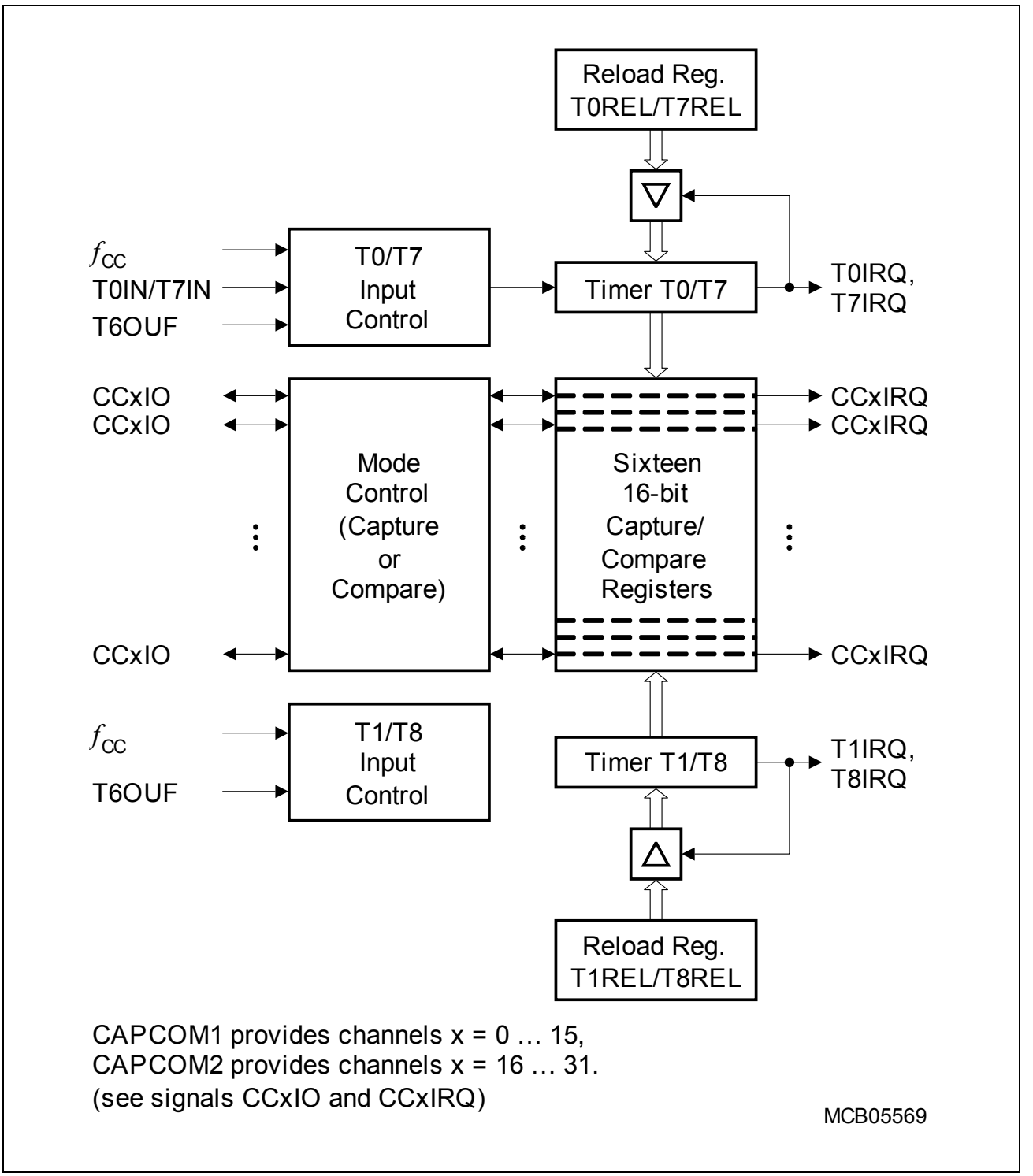

Figure 5 CAPCOM1/2 Unit Block Diagram

3.7 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

3.17 Power Management

The XC161 provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the XC161 into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC161's CPU clock frequency which drastically reduces the consumed power.
  External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3). Each peripheral can separately be disabled/enabled.

The on-chip RTC supports intermittent operation of the XC161 by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Configuration pull-down current[13]	I_{CPDL}[11]		–	10	µA	$V_{IN} = V_{ILmax}$
	I_{CPDH}[12]		120	–	µA	$V_{IN} = V_{IHmin}$
Level inactive hold current[14]	I_{LHI}[11]		–	-10	µA	$V_{OUT} = 0.5 \times V_{DDP}$
Level active hold current[14]	I_{LHA}[12]		-100	–	µA	V_{OUT} = 0.45 V
XTAL1, XTAL3 input current	I_{IL}	CC	–	±20	µA	$0 V < V_{IN} < V_{DDI}$
Pin capacitance[15] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of $0.4 \times V_{DDI}$ is sufficient.

3) If XTAL3 is driven by a crystal, reaching an amplitude (peak to peak) of $0.25 \times V_{DDI}$ is sufficient.

4) This parameter is tested for P2, P3, P4, P6, P7, P9.

5) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

6) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

7) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

8) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

9) The driver of P3.15 is designed for faster switching, because this pin can deliver the reference clock for the bus interface (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 µA.

10) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0.
The pull-ups on $\overline{RD}$ and $\overline{WR}$ ($\overline{WRL}$/$\overline{WRH}$) are also active during bus hold.

11) The maximum current may be drawn while the respective signal line remains inactive.

12) The minimum current must be drawn to drive the respective signal line active.

13) This specification is valid during Reset for configuration on ALE.
The pull-down on ALE is also active during bus hold.

14) This specification is valid during Reset for pins P6.4-0, which can act as $\overline{CS}$ outputs.
The pull-ups on $\overline{CS}$ outputs are also active during bus hold.
The pull-up on pin $\overline{HLDA}$ is active when arbitration is enabled and the EBC operates in slave mode.

15) Not subject to production test - verified by design/characterization.

3) The pad supply voltage pins (V_{DDP}) mainly provide the current consumed by the pin output drivers. This output driver current is not covered by parameter I_{DDP}. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.
4) The total supply current in Sleep and Power down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator or auxiliary oscillator (if active).
5) This parameter is determined mainly by the transistor leakage currents. This current heavily depends on the junction temperature (see **Figure 12**). The junction temperature T_J is the same as the ambient temperature T_A if no current flows through the port output drivers. Otherwise, the resulting temperature difference must be taken into account.
6) All inputs (including JTAG pins and pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.
7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 11**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

Sample time and conversion time of the XC161's A/D Converter are programmable. In compatibility mode, the above timing can be calculated using **Table 15**.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 15 A/D Converter Computation Table[1)]

ADCON.15|14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13|12 (ADSTC)	Sample Time t_S
00	f_{SYS} / 4	00	$t_{BC} \times 8$
01	f_{SYS} / 2	01	$t_{BC} \times 16$
10	f_{SYS} / 16	10	$t_{BC} \times 32$
11	f_{SYS} / 8	11	$t_{BC} \times 64$

1) These selections are available in compatibility mode. An improved mechanism to control the ADC input clock can be selected.

Converter Timing Example:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), ADCTC = '01', ADSTC = '00'
Basic clock f_{BC} = f_{SYS} / 2 = 20 MHz, i.e. t_{BC} = 50 ns
Sample time t_S = $t_{BC} \times 8$ = 400 ns
Conversion 10-bit:
With post-calibr. t_{C10P} = $52 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2600 + 400 + 150) ns = 3.15 µs
Post-calibr. off t_{C10} = $40 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2000 + 400 + 150) ns = 2.55 µs
Conversion 8-bit:
With post-calibr. t_{C8P} = $44 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2200 + 400 + 150) ns = 2.75 µs
Post-calibr. off t_{C8} = $32 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (1600 + 400 + 150) ns = 2.15 µs

4.4 AC Parameters

4.4.1 Definition of Internal Timing

The internal operation of the XC161 is controlled by the internal master clock f_{MC}.

The master clock signal f_{MC} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{MC}. This influence must be regarded when calculating the timings for the XC161.

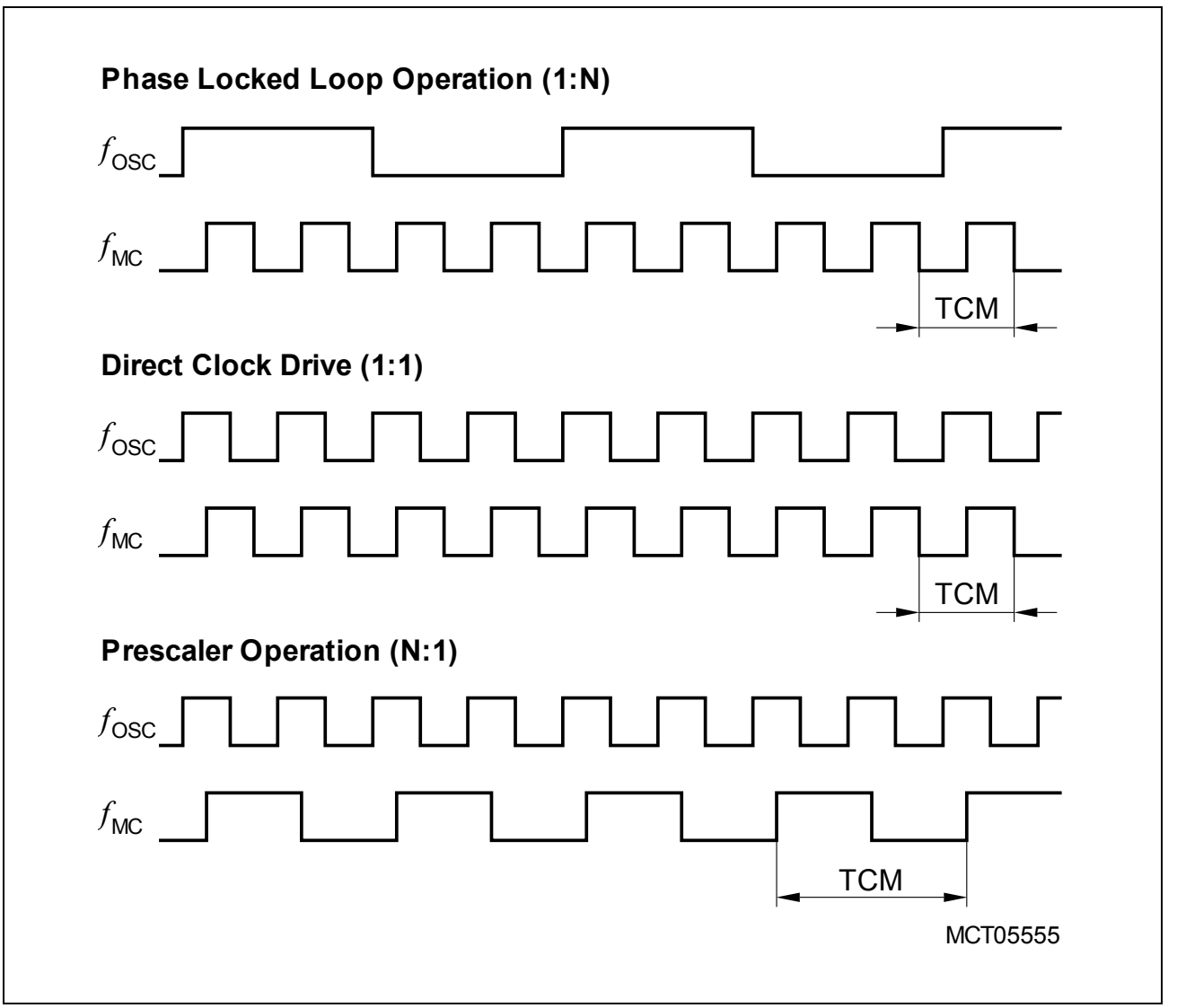

Figure 14 Generation Mechanisms for the Master Clock

*Note: The example for PLL operation shown in **Figure 14** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The used mechanism to generate the master clock is selected by register PLLCON.

generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = PLLODIV+1) to generate the master clock signal f_{MC}. Therefore, the number of VCO cycles can be represented as K × **N**, where **N** is the number of consecutive f_{MC} cycles (TCM).

For a period of **N** × TCM the accumulated PLL jitter is defined by the deviation D_N:

D_N [ns] = ±(1.5 + 6.32 × **N** / f_{MC}); f_{MC} in [MHz], **N** = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: D_3 = ±(1.5 + 6.32 × **3** / 20) = 2.448 ns.

This formula is applicable for K × **N** < 95. For longer periods the K × **N** = 95 value can be used. This steady value can be approximated by: D_{Nmax} [ns] = ±(1.5 + 600 / (K × f_{MC})).

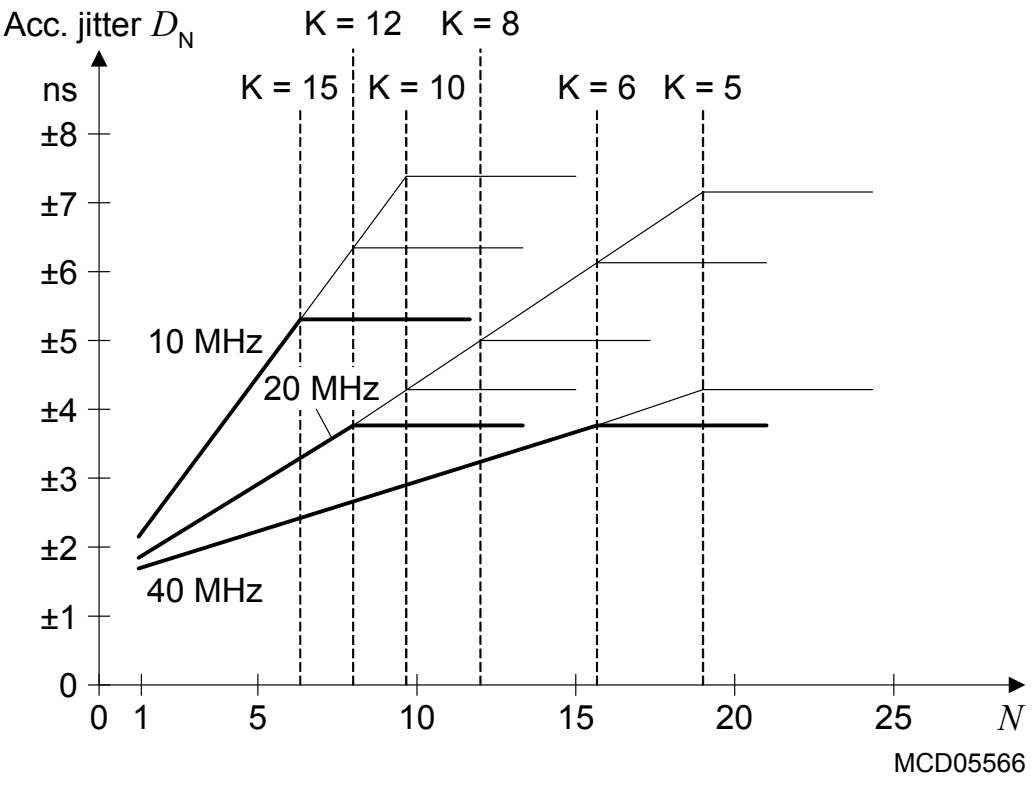

Figure 15 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 16 VCO Bands for PLL Operation[1)]

PLLCON.PLLVB	VCO Frequency Range	Base Frequency Range
00	100 … 150 MHz	20 … 80 MHz
01	150 … 200 MHz	40 … 130 MHz
10	200 … 250 MHz	60 … 180 MHz
11	Reserved	

1) Not subject to production test - verified by design/characterization.

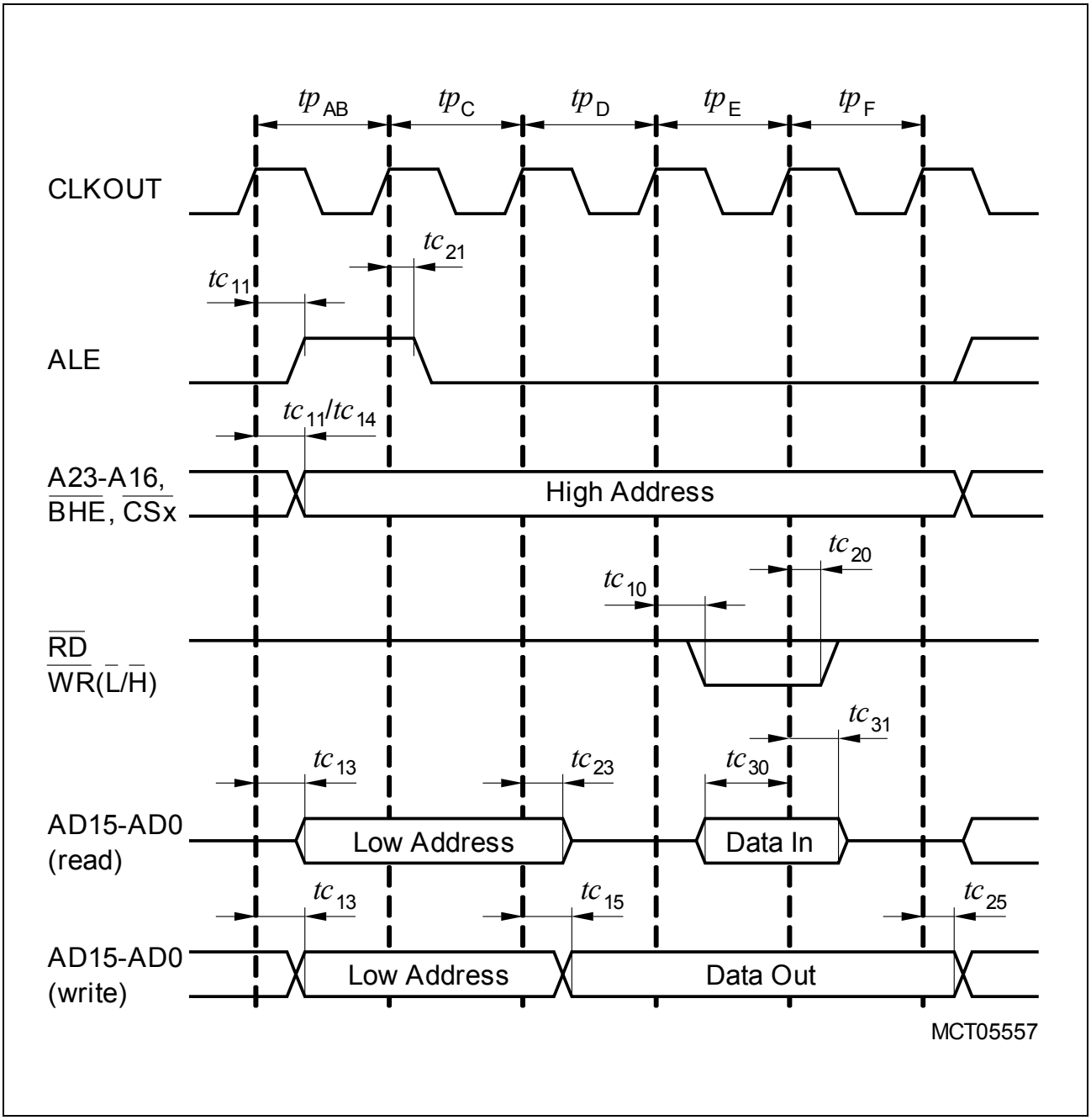

Figure 20 Multiplexed Bus Cycle

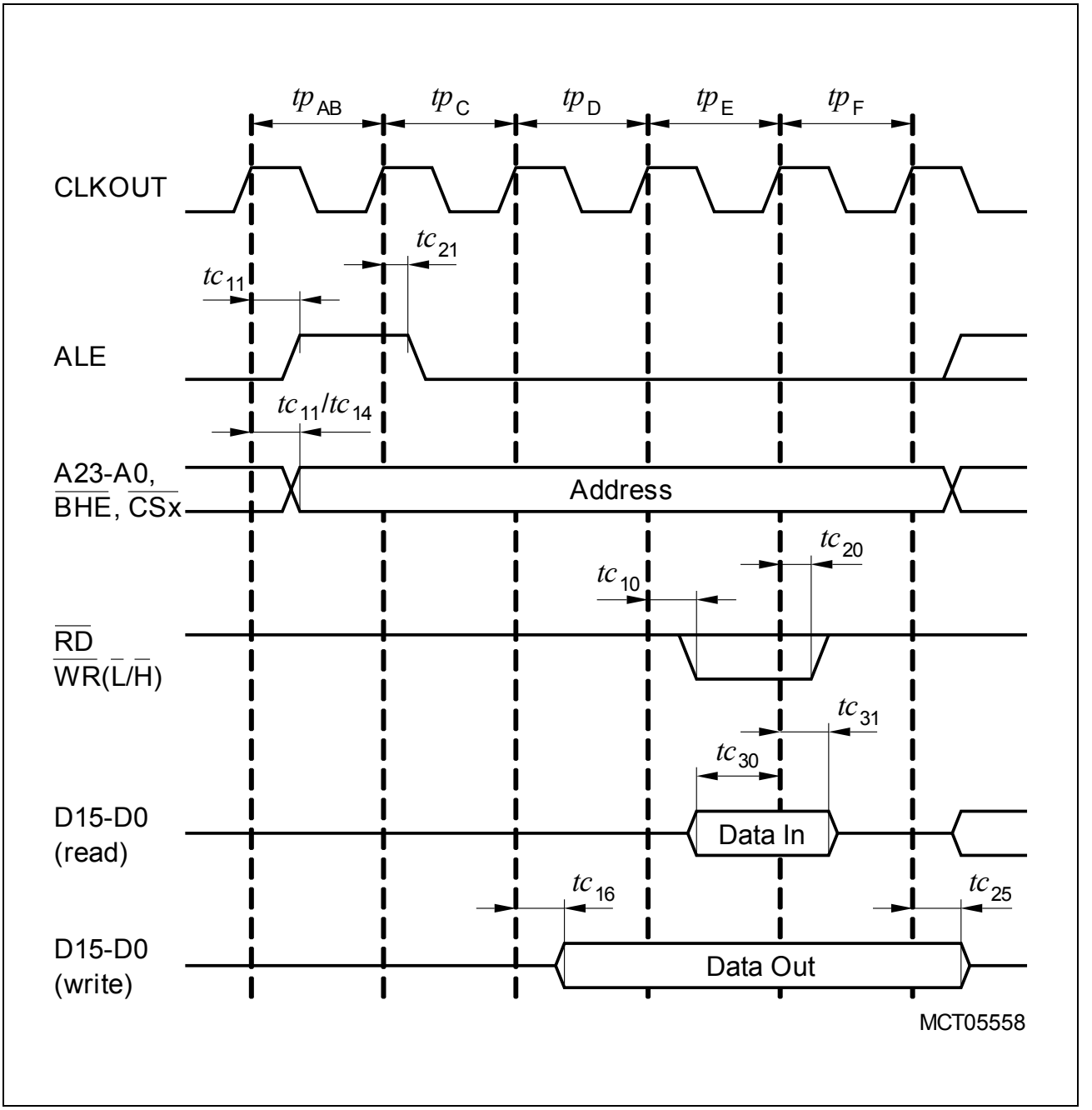

Figure 21 Demultiplexed Bus Cycle

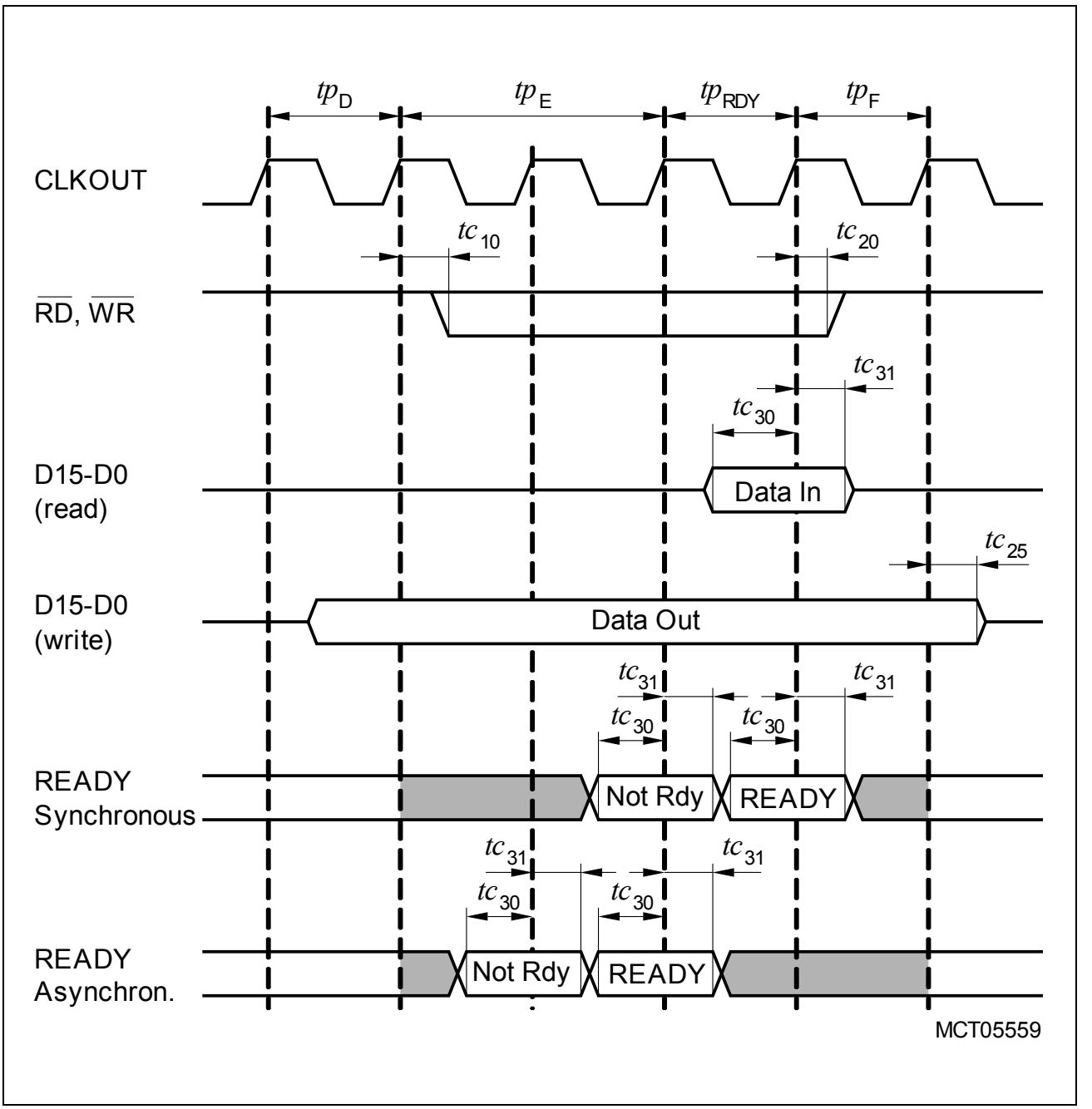

Figure 22 READY Timing

Note: If the READY input is sampled inactive at the indicated sampling point (“Not Rdy”) a READY-controlled waitstate is inserted (tp_{RDY}), sampling the READY input active at the indicated sampling point (“Ready”) terminates the currently running bus cycle.
Note the different sampling points for synchronous and asynchronous READY.
This example uses one mandatory waitstate (see tp_E) before the READY input is evaluated.

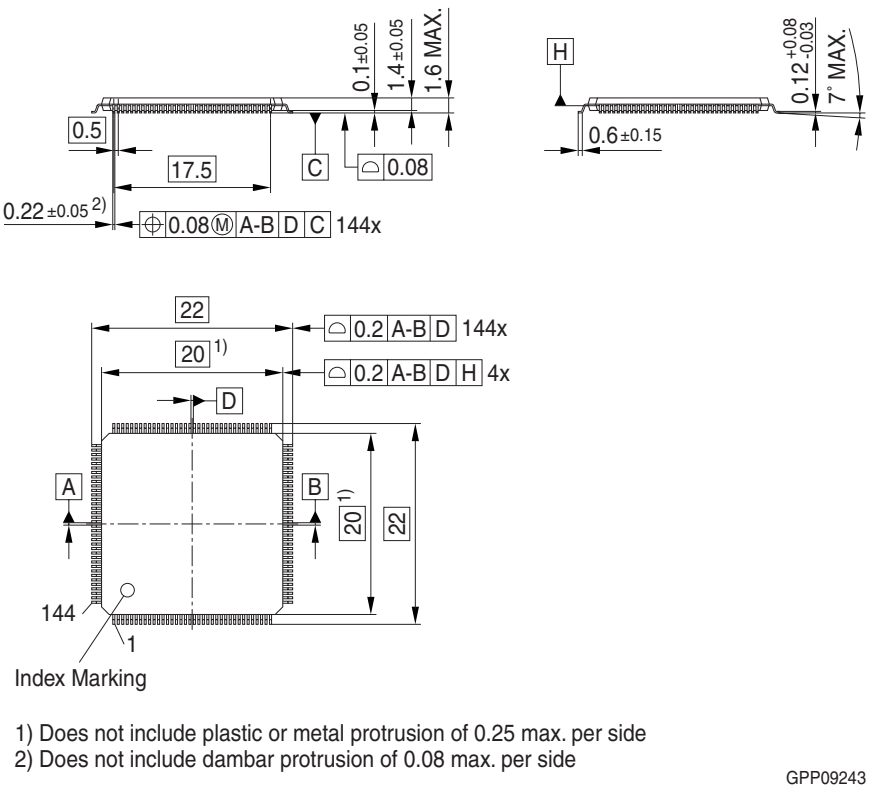

Figure 26 P-TQFP-144-19 (Plastic - Thin Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mm