Infineon Technologies - XC161CS32F40FBBAKXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	99
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc161cs32f40fbbakxuma1

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1 Summary of Features

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 × 16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with 73 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 4 Kbytes On-Chip Data SRAM (DSRAM)
  - 6 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 256 Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - 12-Channel A/D Converter with Programmable Resolution (10-bit or 8-bit) and Conversion Time (down to 2.55 µs or 2.15 µs)
  - Two 16-Channel General Purpose Capture/Compare Units (32 Input/Output Pins)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip TwinCAN Interface (Rev. 2.0B active) with 32 Message Objects (Full CAN/Basic CAN) on Two CAN Nodes, and Gateway Functionality
  - IIC Bus Interface (10-bit addressing, 400 kbit/s) with 3 Channels (multiplexed)
  - On-Chip Real Time Clock, Driven by Dedicated Oscillator
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog

2.2 Pin Configuration and Definition

The pins of the XC161 are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) and C*) mark pins to be used as alternate external interrupt inputs, C*) marks pins that can have CAN interface lines assigned to them.

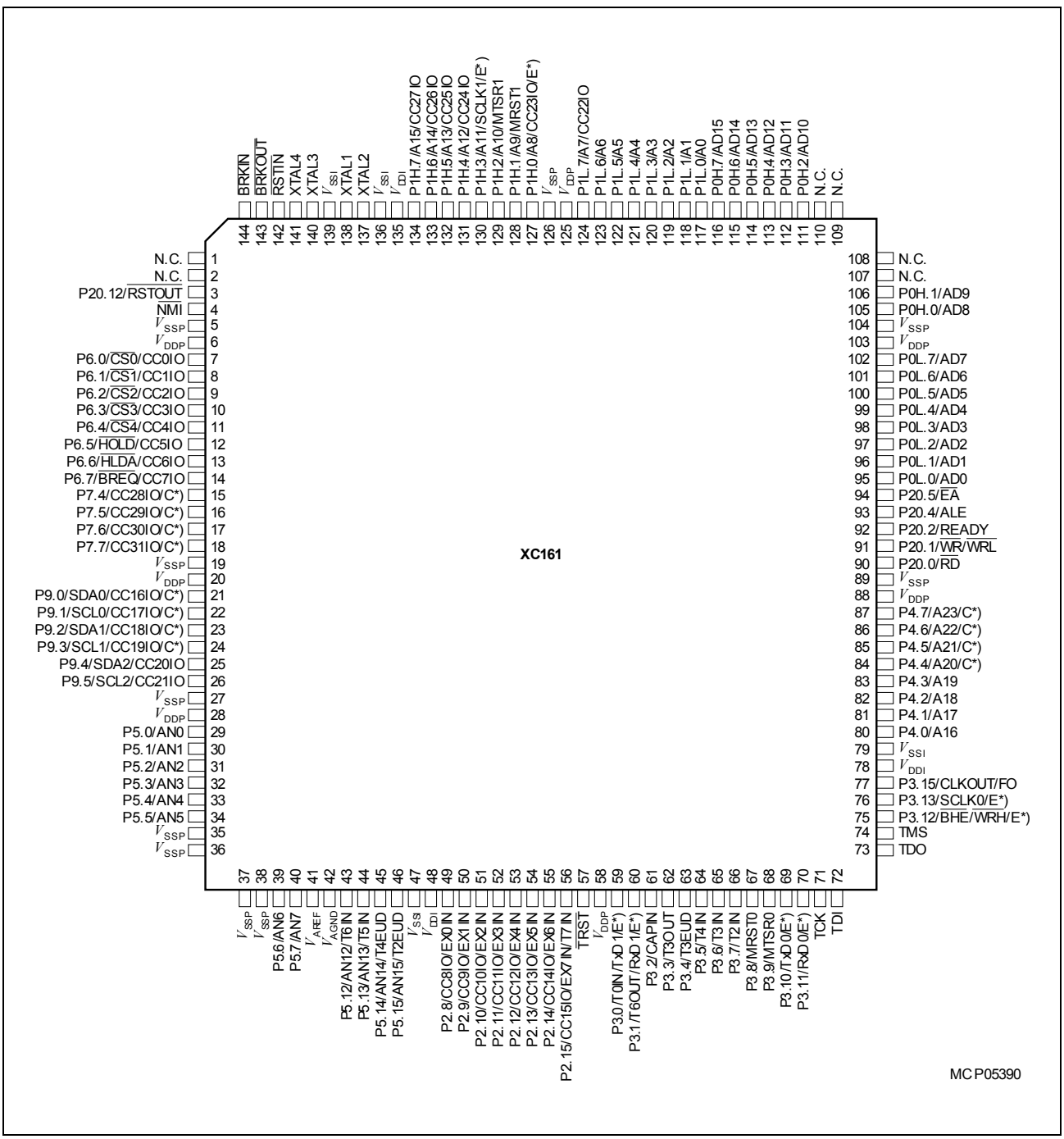

Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function		
P9		IO	Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions:[1)]		
P9.0	21	I/O I I/O	CC16IO CAN2_RxD SDA0	CAPCOM2: CC16 Capture Inp./Compare Outp., CAN Node 2 Receive Data Input, IIC Bus Data Line 0	
P9.1	22	I/O O I/O	CC17IO CAN2_TxD SCL0	CAPCOM2: CC17 Capture Inp./Compare Outp., CAN Node 2 Transmit Data Output, IIC Bus Clock Line 0	
P9.2	23	I/O I I/O	CC18IO CAN1_RxD SDA1	CAPCOM2: CC18 Capture Inp./Compare Outp., CAN Node 1 Receive Data Input, IIC Bus Data Line 1	
P9.3	24	I/O O I/O	CC19IO CAN1_TxD SCL1	CAPCOM2: CC19 Capture Inp./Compare Outp., CAN Node 1 Transmit Data Output, IIC Bus Clock Line 1	
P9.4	25	I/O I/O	CC20IO SDA2	CAPCOM2: CC20 Capture Inp./Compare Outp., IIC Bus Data Line 2	
P9.5	26	I/O I/O	CC21IO SCL2	CAPCOM2: CC21 Capture Inp./Compare Outp., IIC Bus Clock Line 2	
P5		I	Port 5 is a 12-bit input-only port. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:		
P5.0	29	I	AN0		
P5.1	30	I	AN1		
P5.2	31	I	AN2		
P5.3	32	I	AN3		
P5.4	33	I	AN4		
P5.5	34	I	AN5		
P5.6	39	I	AN6		
P5.7	40	I	AN7		
P5.12	43	I	AN12,	T6IN	GPT2 Timer T6 Count/Gate Input
P5.13	44	I	AN13,	T5IN	GPT2 Timer T5 Count/Gate Input
P5.14	45	I	AN14,	T4EUD	GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	46	I	AN15,	T2EUD	GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
PORT0 P0L.0 - P0L.7, P0H.0, P0H.1, P0H.2 - P0H.7	 95 - 102, 105, 106, 111 - 116	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. Each pin can be programmed for input (output driver in high-impedance state) or output. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0 *Note: At the end of an external reset ($\overline{EA}$ = 0) PORT0 also may input configuration values.*
PORT1 P1L.0 - P1L.6 P1L.7 P1H.0 P1H.1 P1H.2 P1H.3 P1H.4 P1H.5 P1H.6 P1H.7	 117 - 123 124 127 128 129 130 131 132 133 134	IO O I/O I/O I I/O I/O I/O I I/O I/O I/O I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions: (A0-6) Address output only CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp. CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp., EX0IN Fast External Interrupt 0 Input (alternate pin B) MRST1 SSC1 Master-Receive/Slave-Transmit In/Outp. MTSR1 SSC1 Master-Transmit/Slave-Receive Out/Inp. SCLK1 SSC1 Master Clock Output/Slave Clock Input, EX0IN Fast External Interrupt 0 Input (alternate pin A) CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp. CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp. CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp. CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.

3 Functional Description

The architecture of the XC161 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC161.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC161.

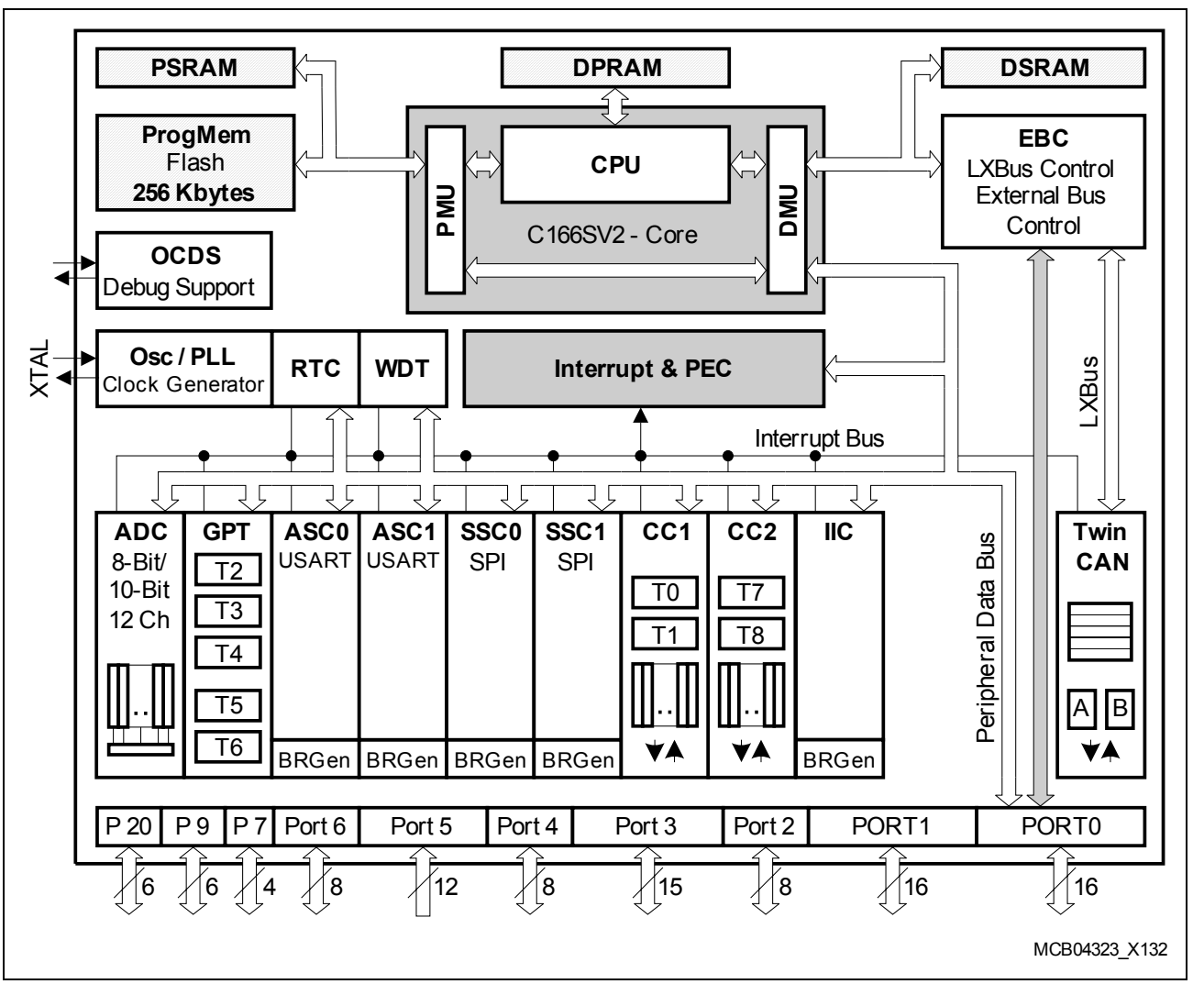

Figure 3 Block Diagram

Table 4 XC161 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
CAN0	CAN_0IC	xx'0150$_H$	54$_H$ / 84$_D$
CAN1	CAN_1IC	xx'0154$_H$	55$_H$ / 85$_D$
CAN2	CAN_2IC	xx'0158$_H$	56$_H$ / 86$_D$
CAN3	CAN_3IC	xx'015C$_H$	57$_H$ / 87$_D$
CAN4	CAN_4IC	xx'0164$_H$	59$_H$ / 89$_D$
CAN5	CAN_5IC	xx'0168$_H$	5A$_H$ / 90$_D$
CAN6	CAN_6IC	xx'016C$_H$	5B$_H$ / 91$_D$
CAN7	CAN_7IC	xx'0170$_H$	5C$_H$ / 92$_D$
RTC	RTC_IC	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	–	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	–	xx'0134$_H$	4D$_H$ / 77$_D$
Unassigned node	–	xx'0138$_H$	4E$_H$ / 78$_D$
Unassigned node	–	xx'013C$_H$	4F$_H$ / 79$_D$
Unassigned node	–	xx'0140$_H$	50$_H$ / 80$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

The XC161 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions: • Hardware Reset • Software Reset • Watchdog Timer Overflow	–	 RESET RESET RESET	 xx’0000$_H$ xx’0000$_H$ xx’0000$_H$	 00$_H$ 00$_H$ 00$_H$	 III III III
Class A Hardware Traps: • Non-Maskable Interrupt • Stack Overflow • Stack Underflow • Software Break	 NMI STKOF STKUF SOFTBRK	 NMITRAP STOTRAP STUTRAP SBRKTRAP	 xx’0008$_H$ xx’0010$_H$ xx’0018$_H$ xx’0020$_H$	 02$_H$ 04$_H$ 06$_H$ 08$_H$	 II II II II
Class B Hardware Traps: • Undefined Opcode • PMI Access Error • Protected Instruction Fault • Illegal Word Operand Access	 UNDOPC PACER PRTFLT ILLOPA	 BTRAP BTRAP BTRAP BTRAP	 xx’0028$_H$ xx’0028$_H$ xx’0028$_H$ xx’0028$_H$	 0A$_H$ 0A$_H$ 0A$_H$ 0A$_H$	 I I I I
Reserved	–	–	[2C$_H$ - 3C$_H$]	[0B$_H$ - 0F$_H$]	–
Software Traps • TRAP Instruction	–	–	Any [xx’0000$_H$ - xx’01FC$_H$] in steps of 4$_H$	Any [00$_H$ - 7F$_H$]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

3.12 TwinCAN Module

The integrated TwinCAN module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip TwinCAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Two Full-CAN nodes share the TwinCAN module's resources to optimize the CAN bus traffic handling and to minimize the CPU load. The module provides up to 32 message objects, which can be assigned to one of the CAN nodes and can be combined to FIFO-structures. Each object provides separate masks for acceptance filtering.

The flexible combination of Full-CAN functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the number of message objects permit precise and comfortable CAN bus traffic handling.

Gateway functionality allows automatic data exchange between two separate CAN bus systems, which reduces CPU load and improves the real time behavior of the entire system.

The bit timing for both CAN nodes is derived from the master clock and is programmable up to a data rate of 1 Mbit/s. Each CAN node uses two pins of Port 4, Port 7, or Port 9 to interface to an external bus transceiver. The interface pins are assigned via software.

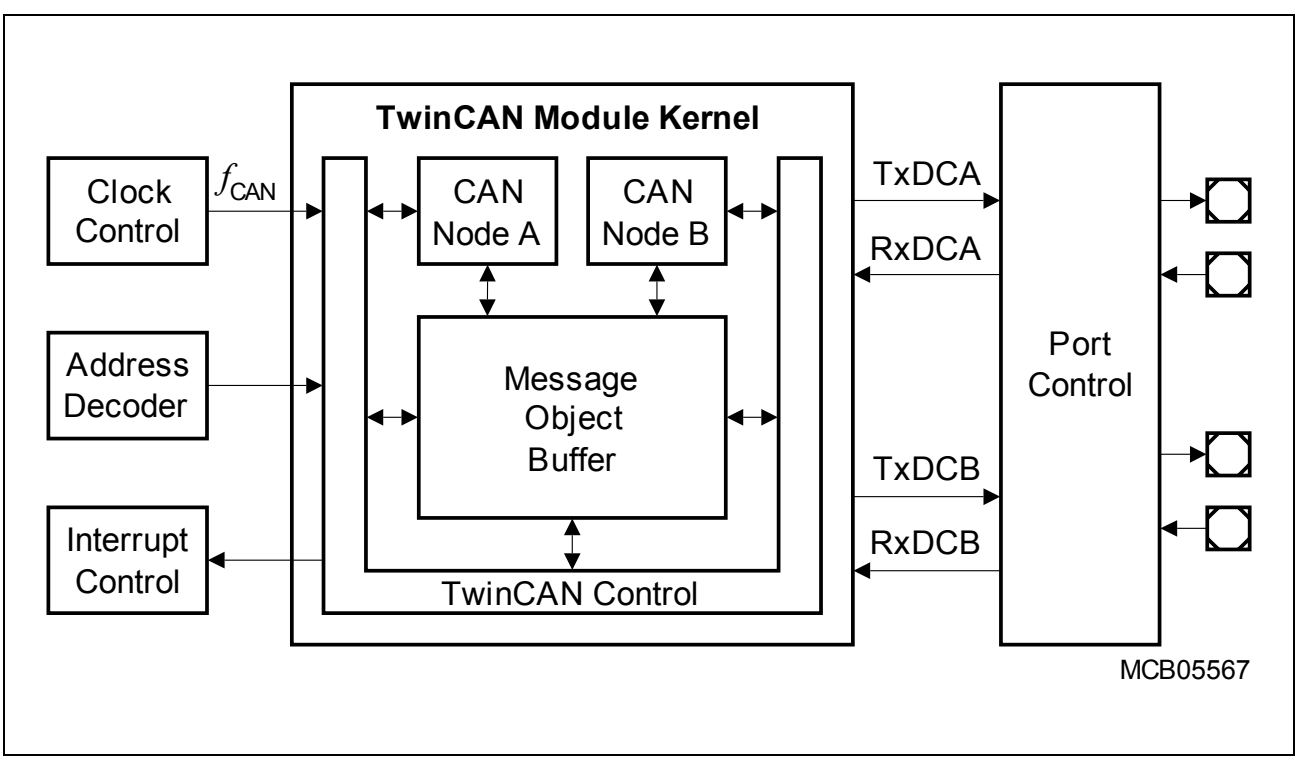

Figure 9 TwinCAN Module Block Diagram

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Configuration pull-down current[13]	I_{CPDL}[11]		–	10	µA	$V_{IN} = V_{ILmax}$
	I_{CPDH}[12]		120	–	µA	$V_{IN} = V_{IHmin}$
Level inactive hold current[14]	I_{LHI}[11]		–	-10	µA	$V_{OUT} = 0.5 \times V_{DDP}$
Level active hold current[14]	I_{LHA}[12]		-100	–	µA	V_{OUT} = 0.45 V
XTAL1, XTAL3 input current	I_{IL}	CC	–	±20	µA	$0 V < V_{IN} < V_{DDI}$
Pin capacitance[15] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of $0.4 \times V_{DDI}$ is sufficient.

3) If XTAL3 is driven by a crystal, reaching an amplitude (peak to peak) of $0.25 \times V_{DDI}$ is sufficient.

4) This parameter is tested for P2, P3, P4, P6, P7, P9.

5) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

6) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

7) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

8) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

9) The driver of P3.15 is designed for faster switching, because this pin can deliver the reference clock for the bus interface (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 µA.

10) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0.
The pull-ups on $\overline{RD}$ and $\overline{WR}$ ($\overline{WRL}$/$\overline{WRH}$) are also active during bus hold.

11) The maximum current may be drawn while the respective signal line remains inactive.

12) The minimum current must be drawn to drive the respective signal line active.

13) This specification is valid during Reset for configuration on ALE.
The pull-down on ALE is also active during bus hold.

14) This specification is valid during Reset for pins P6.4-0, which can act as $\overline{CS}$ outputs.
The pull-ups on $\overline{CS}$ outputs are also active during bus hold.
The pull-up on pin $\overline{HLDA}$ is active when arbitration is enabled and the EBC operates in slave mode.

15) Not subject to production test - verified by design/characterization.

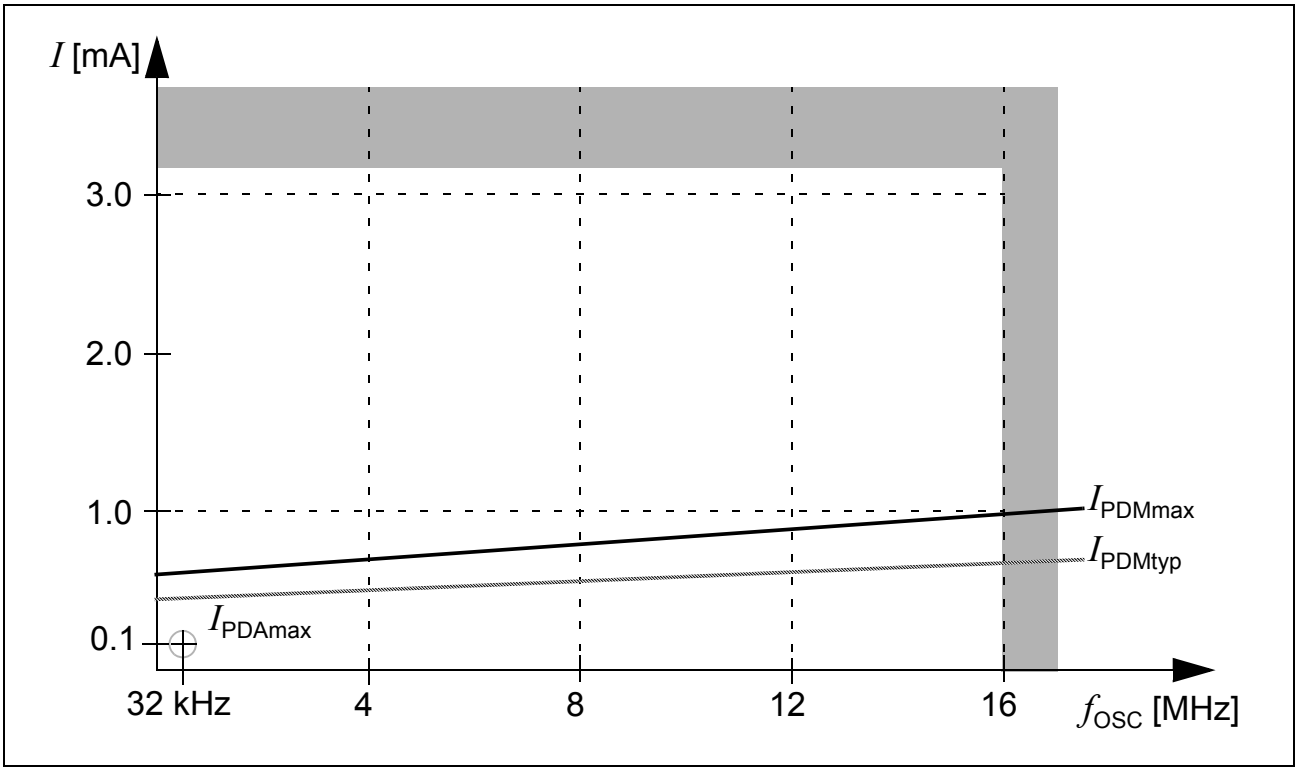

Figure 11 **Sleep and Power Down Supply Current due to RTC and Oscillator Running, as a Function of Oscillator Frequency**

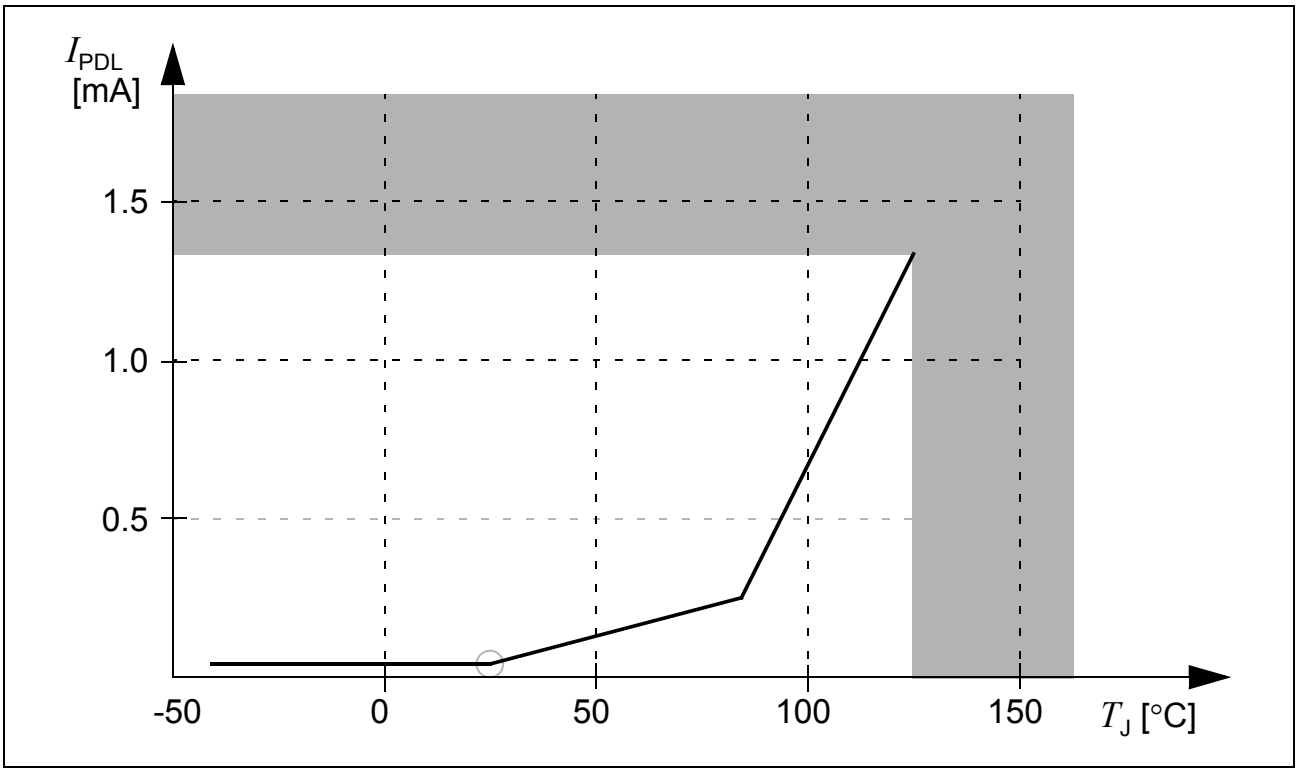

Figure 12 **Sleep and Power Down Leakage Supply Current as a Function of Temperature**

Sample time and conversion time of the XC161's A/D Converter are programmable. In compatibility mode, the above timing can be calculated using **Table 15**.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 15 A/D Converter Computation Table[1)]

ADCON.15|14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13|12 (ADSTC)	Sample Time t_S
00	f_{SYS} / 4	00	$t_{BC} \times 8$
01	f_{SYS} / 2	01	$t_{BC} \times 16$
10	f_{SYS} / 16	10	$t_{BC} \times 32$
11	f_{SYS} / 8	11	$t_{BC} \times 64$

1) These selections are available in compatibility mode. An improved mechanism to control the ADC input clock can be selected.

Converter Timing Example:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), ADCTC = '01', ADSTC = '00'
Basic clock f_{BC} = f_{SYS} / 2 = 20 MHz, i.e. t_{BC} = 50 ns
Sample time t_S = $t_{BC} \times 8$ = 400 ns
Conversion 10-bit:
With post-calibr. t_{C10P} = $52 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2600 + 400 + 150) ns = 3.15 µs
Post-calibr. off t_{C10} = $40 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2000 + 400 + 150) ns = 2.55 µs
Conversion 8-bit:
With post-calibr. t_{C8P} = $44 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2200 + 400 + 150) ns = 2.75 µs
Post-calibr. off t_{C8} = $32 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (1600 + 400 + 150) ns = 2.15 µs

4.4 AC Parameters

4.4.1 Definition of Internal Timing

The internal operation of the XC161 is controlled by the internal master clock f_{MC}.

The master clock signal f_{MC} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{MC}. This influence must be regarded when calculating the timings for the XC161.

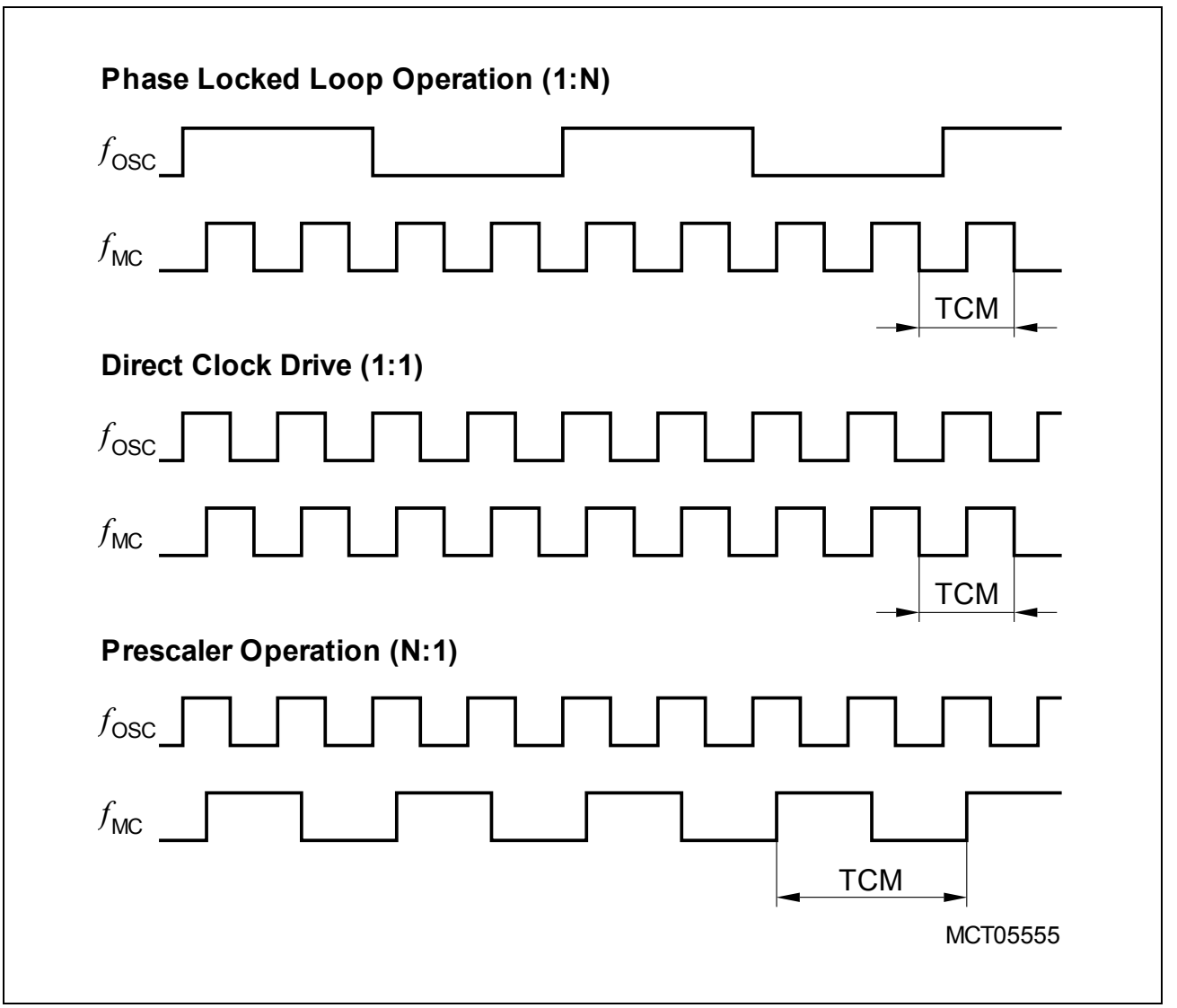

Figure 14 Generation Mechanisms for the Master Clock

*Note: The example for PLL operation shown in **Figure 14** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The used mechanism to generate the master clock is selected by register PLLCON.

4.4.2 On-chip Flash Operation

The XC161's Flash module delivers data within a fixed access time (see **Table 17**).

Accesses to the Flash module are controlled by the PMI and take 1+WS clock cycles, where WS is the number of Flash access waitstates selected via bitfield WSFLASH in register IMBCTRL. The resulting duration of the access phase must cover the access time t_{ACC} of the Flash array. Therefore, the required Flash waitstates depend on the available speed grade as well as on the actual system frequency.

Note: The Flash access waitstates only affect non-sequential accesses. Due to prefetching mechanisms, the performance for sequential accesses (depending on the software structure) is only partially influenced by waitstates.
In typical applications, eliminating one waitstate increases the average performance by 5% … 15 %.

Table 17 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
Flash module access time (Standard)	t_{ACC}	CC	–	–	70[1]	ns
Flash module access time (Grade A)	t_{ACC}	CC	–	–	50[1]	ns
Programming time per 128-byte block	t_{PR}	CC	–	2[2]	5	ms
Erase time per sector	t_{ER}	CC	–	200[2]	500	ms

1) The actual access time is also influenced by the system frequency, so the frequency ranges are not fully linear. See **Table 18**.

2) Programming and erase time depends on the system frequency. Typical values are valid for 40 MHz.

Example: For an operating frequency of 40 MHz (clock cycle = 25 ns), Standard devices must be operated with 2 waitstates: ((2+1) × 25 ns) ≥ 70 ns.
Grade A devices can be operated with 1 waitstate: ((1+1) × 25 ns) ≥ 50 ns.

Table 18 indicates the interrelation of waitstates, system frequency, and speed grade.

Table 18 Flash Access Waitstates

Required Waitstates	Frequency Range for Standard Flash Speed	Frequency Range for Flash Speed Grade A
0 WS (WSFLASH = 00_B)	$f_{CPU} \leq 16$ MHz	$f_{CPU} \leq 20$ MHz
1 WS (WSFLASH = 01_B)	$f_{CPU} \leq 28$ MHz	$f_{CPU} \leq 40$ MHz
2 WS (WSFLASH = 10_B)	$f_{CPU} \leq 40$ MHz	$f_{CPU} \leq 40$ MHz

Note: The maximum achievable system frequency is limited by the properties of the respective derivative, i.e. 40 MHz (or 20 MHz for xxx-32F20F devices).

4.4.5 External Bus Timing

Table 20 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	40/30/25[1]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/33/40 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

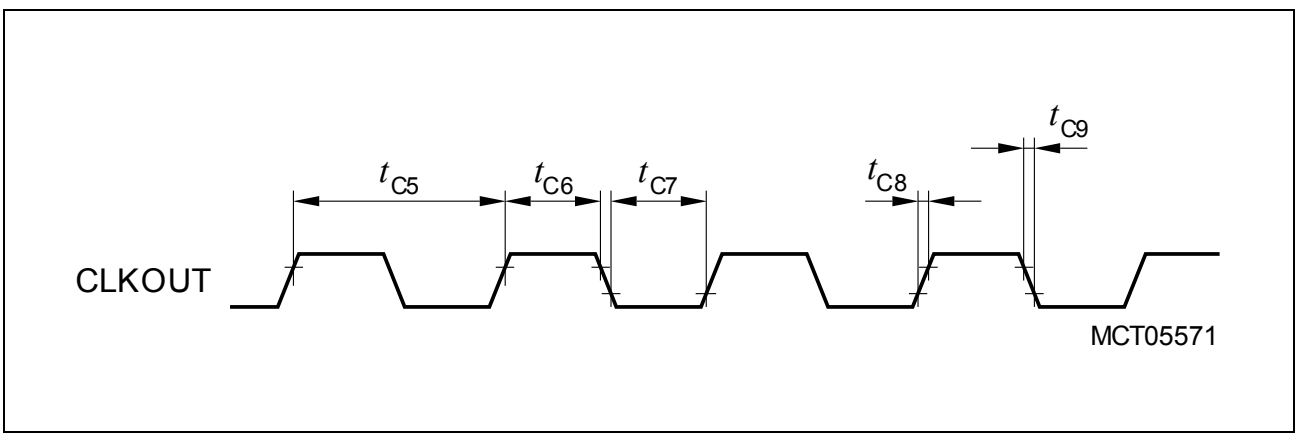

Figure 19 CLKOUT Signal Timing

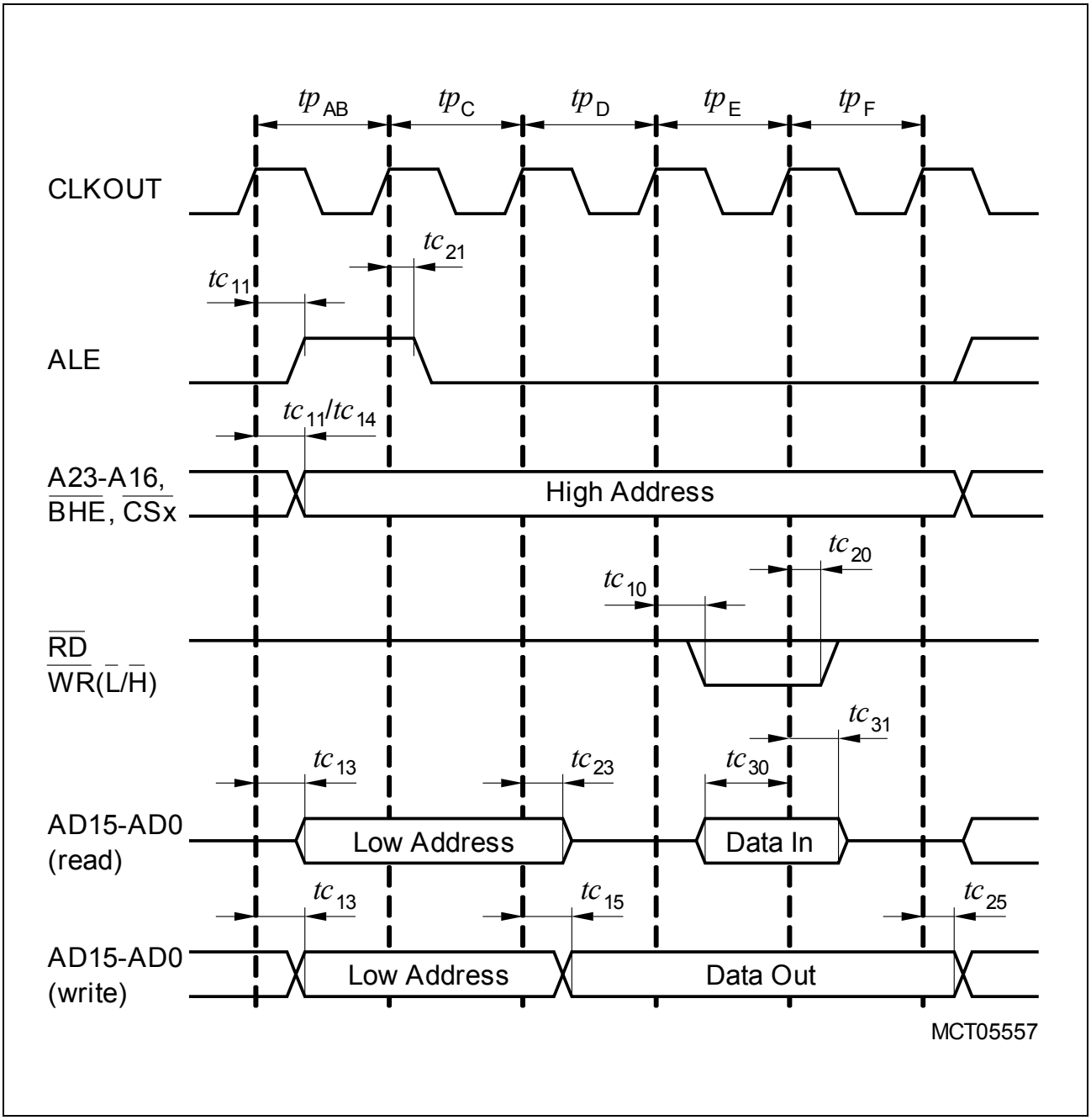

Figure 20 Multiplexed Bus Cycle

Bus Cycle Control via READY Input

The duration of an external bus cycle can be controlled by the external circuitry via the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous READY puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage. The minimum duration of an asynchronous READY signal to be safely synchronized must be one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next following bus cycle is READY-controlled, an active READY signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the programmed phases of the next following cycle.

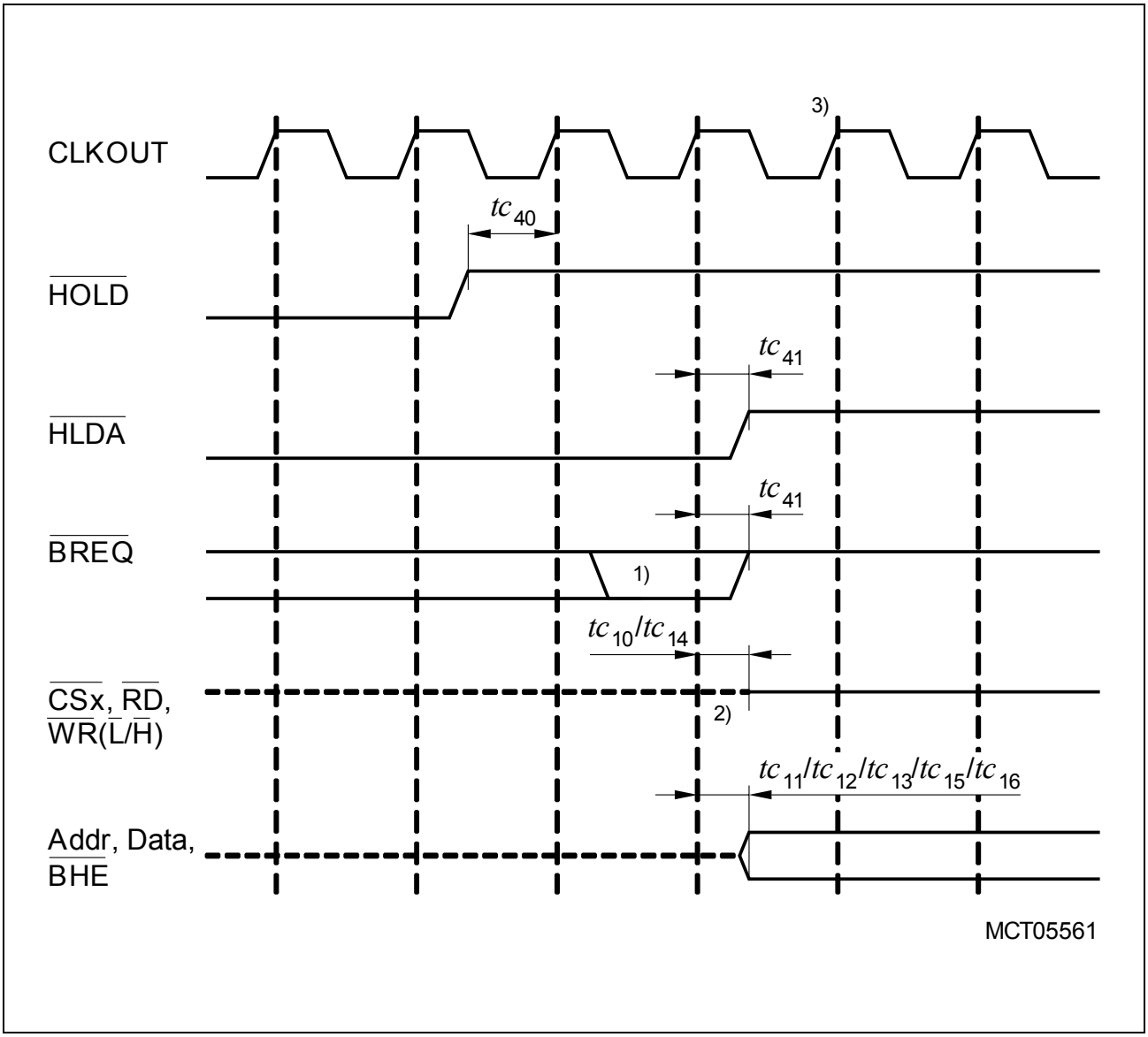

Figure 24 External Bus Arbitration, Regaining the Bus

Notes

1. *This is the last chance for BREQ to trigger the indicated regain-sequence. Even if BREQ is activated earlier, the regain-sequence is initiated by HOLD going high. Please note that HOLD may also be deactivated without the XC161 requesting the bus.*
2. *The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).*
3. *The next XC161 driven bus cycle may start here.*

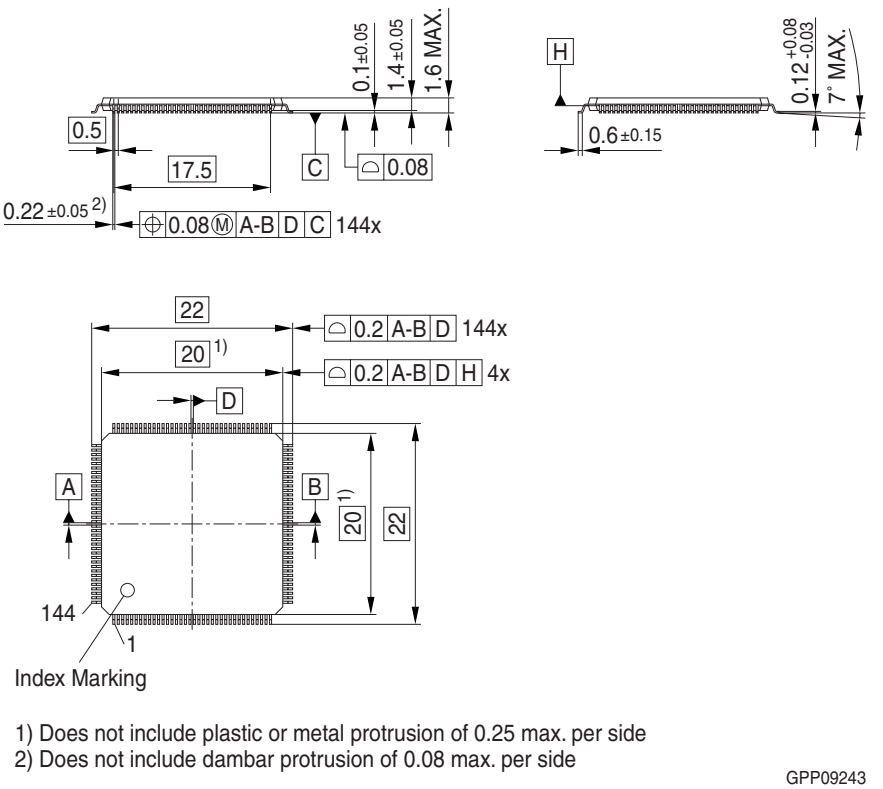

Figure 26 P-TQFP-144-19 (Plastic - Thin Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mm