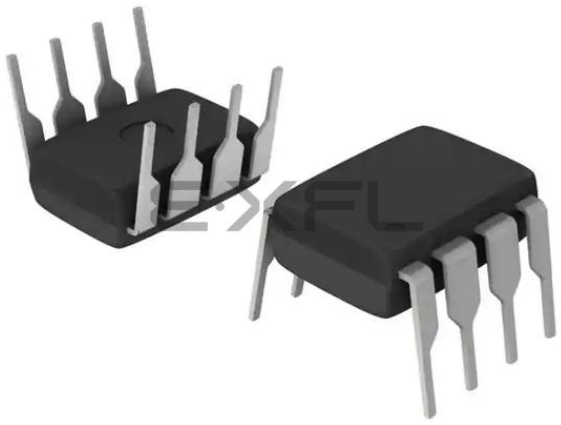

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RS08 |
| Core Size | 8-Bit |
| Speed | 10MHz |
| Connectivity | - |
| Peripherals | LVD, POR, WDT |
| Number of I/O | 4 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 63 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 8-DIP (0.300", 7.62mm) |
| Supplier Device Package | 8-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/pc9rs08ka2pae |

# MC9RS08KA2 Series Data Sheet

Covers: MC9RS08KA2
MC9RS08KA1

MC9RS08KA2
Rev. 4
12/2008

freescale™
semiconductor

# Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com

The following revision history table summarizes changes contained in this document.

| Revision Number | Revision Date | Description of Changes |
|---|---|---|
| 1.0 | 04/2006 | Initial public release version |
| 2 | 12/2006 | Added MC9RS08KA1 |
| 3 | 09/2007 | Corrected Instruction Set Summary LDX ,X row operand to read 0E 0F. Revised the Analog Comparator Electrical Specifications including the ACMP Bandgap reference voltage values. Corrected a transposition in the DFN drawing no. Updated the ICS Characteristic table in the Electricals Appendix to include the ICS factory trim and reference the parameters $t_{ir\_wu}$ and $t_{fll\_wu}$ that are discussed in the ICS chapter. |
| 4 | 12/2008 | Revised Figure 1-2. Updated “How to Reach Us” information.<br>Changed the mechanical drawing of 6-pin DFN in the Appendix B, “Ordering Information and Mechanical Drawings.” |

## Chapter 8
## Central Processor Unit (RS08CPUV1)

## Appendix A
## Electrical Characteristics



## Appendix B
## Ordering Information and Mechanical Drawings

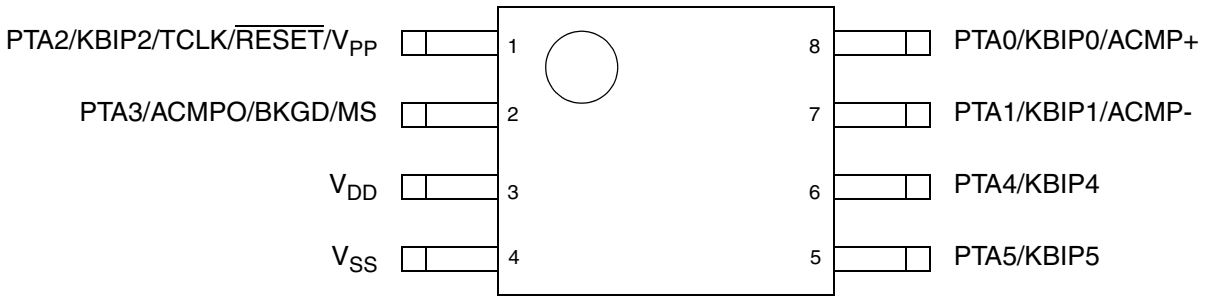


**Figure 2-3. MC9RS08KA2 Series in 8-Pin Narrow Body SOIC**

## 2.3 Recommended System Connections

Figure 2-4 shows reference connection for background debug and Flash programming.

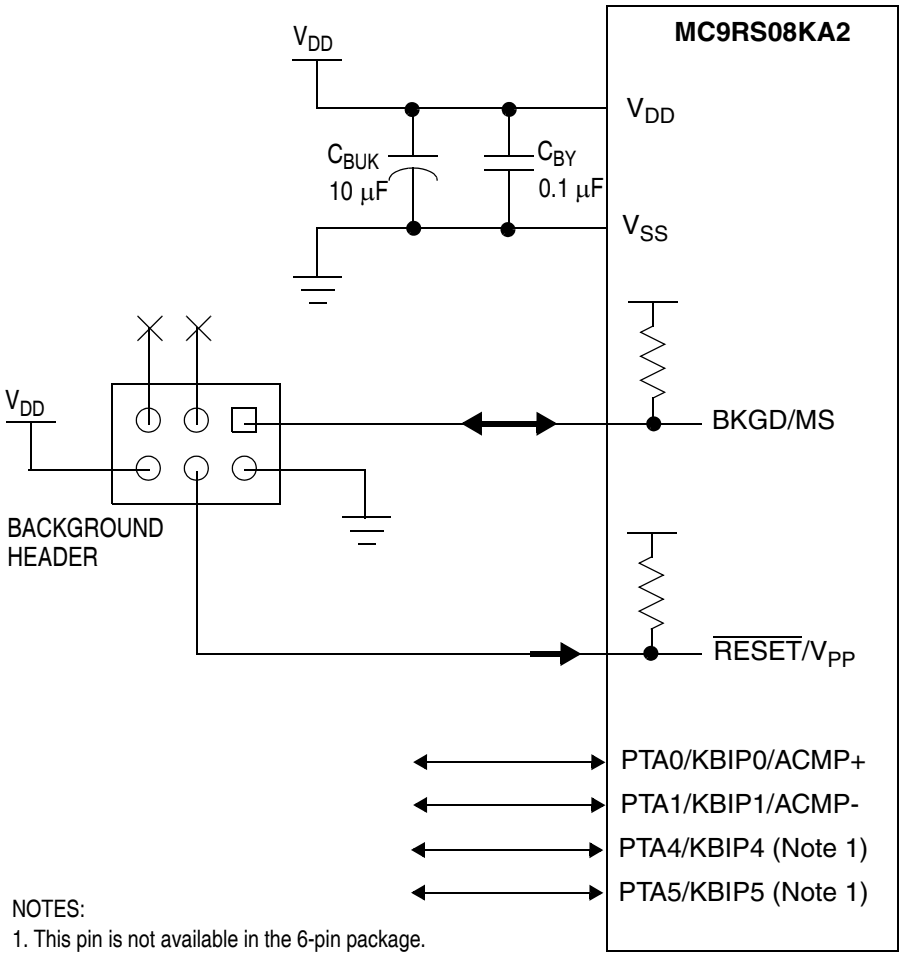


**Figure 2-4. Reference System Connection Diagram**

## 2.4 Pin Detail

This section provides a detailed description of system connections.

cables and the absolute value of the internal pullup device play almost no role in determining rise and fall times on the BKGD pin.

### 2.4.4 General-Purpose I/O and Peripheral Ports

The remaining pins are shared among general-purpose I/O and on-chip peripheral functions such as timers and analog comparator. Immediately after reset, all of these pins are configured as high-impedance general-purpose inputs with internal pullup/pulldown devices disabled.

**NOTE**

To avoid extra current drain from floating input pins, the reset initialization routine in the application program should either enable on-chip pullup/pulldown devices or change the direction of unused pins to outputs.

**Table 2-1. Pin Sharing Reference**

| Pin Name | Direction | Pullup/Pulldown[1] | Alternative Functions[2] | |
|---|---|---|---|---|
| $V_{DD}$ | — | — | Power | |
| $V_{SS}$ | — | — | Ground | |
| PTA0 | I/O | SWC | PTA0<br>KBIP0<br>ACMP+ | General-purpose input/output (GPIO)<br>Keyboard interrupt (stop/wait wakeup only)<br>Analog comparator input |
| PTA1 | I/O | SWC | PTA1<br>KBIP1<br>ACMP- | General-purpose input/output (GPIO)<br>Keyboard interrupt (stop/wait wakeup only)<br>Analog comparator input |
| PTA2 | I | SWC[4] | PTA2<br>KBIP2<br>TCLK<br>$\overline{\text{RESET}}$<br>$V_{PP}$ | General-purpose input<br>Keyboard interrupt (stop/wait wakeup only)<br>Modulo timer clock source<br>Reset<br>$V_{PP}$ |
| PTA3 | I/O[3] | —[4] | PTA3<br>ACMPO<br>BKGD<br>MS | General-purpose output<br>Analog comparator output<br>Background debug data<br>Mode select |
| PTA4[5] | I/O | SWC | PTA4<br>KBIP4 | General-purpose input/output (GPIO)<br>Keyboard interrupt (stop/wait wakeup only) |
| PTA5[5] | I/O | SWC | PTA5<br>KBIP5 | General-purpose input/output (GPIO)<br>Keyboard interrupt (stop/wait wakeup only) |

1 SWC is software-controlled pullup/pulldown resistor; the register is associated with the respective port.

2 Alternative functions are listed lowest priority first. For example, GPIO is the lowest priority alternative function of the PTA0 pin; ACMP+ is the highest priority alternative function of the PTA0 pin.

3 Output-only when configured as PTA3 function.

4 When PTA2 or PTA3 is configured as $\overline{\text{RESET}}$ or BKGD/MS, respectively, pullup is enabled. When $V_{PP}$ is attached, pullup/pulldown is disabled automatically.

5 This pin is not available in 6-pin package. Enabling either the pullup or pulldown device is recommended to prevent extra current leakage from the floating input pin.

**Table 4-1. Register Summary (continued)**

| Address | Register Name | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| $020C–$020F | Unimplemented | — | — | — | — | — | — | — | — |
| $0210 | FOPT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SECD |
| $0211 | FLCR | 0 | 0 | 0 | 0 | HVEN | MASS | 0 | PGM |
| $0212–$0213 | Reserved | — | — | — | — | — | — | — | — |
| $0214–$021F | Unimplemented | — — | — — | — — | — — | — — | — — | — — | — — |
| $0220 | PTAPE | 0 | 0 | PTAPE5 | PTAPE4 | 0 | PTAPE2 | PTAPE1 | PTAPE0 |
| $0221 | PTAPUD | 0 | 0 | PTAPUD5 | PTAPUD4 | 0 | PTAPUD2 | PTAPUD1 | PTAPUD0 |
| $0222 | PTASE | 0 | 0 | PTASE5 | PTASE4 | PTASE3 | 0 | PTASE1 | PTASE0 |
| $0223–$023F | Unimplemented | — | — | — | — | — | — | — | — |
| $3FF8 | Reserved | — | — | — | — | — | — | — | — |
| $3FF9 | Reserved | — | — | — | — | — | — | — | — |
| $3FFA[2] | Reserved | Reserved for Room Temperature ICS Trim | | | | | | | |
| $3FFB[2] | Reserved | Reserved | | | | | | | FTRIM |
| $3FFC | NVOPT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SECD |

= Unimplemented or Reserved

1 Physical RAM in $000E can be accessed through D[X] register when the content of the index register X is $0E.

2 If using the MCU untrimmed, $3FFA and $3FFB may be used by applications.

## 4.5 RAM

The device includes two sections of static RAM. The locations from $0000 to $000D can be directly accessed using the more efficient tiny addressing mode instructions and short addressing mode instructions. Location $000E RAM can either be accessed through D[X] register when register X is $0E or through the paging window location $00CE when PAGESEL register is $00. The second section of RAM starts from $0020 to $004F, and it can be accessed using direct addressing mode instructions.

The RAM retains data when the MCU is in low-power wait and stop mode. RAM data is unaffected by any reset provided that the supply voltage does not drop below the minimum value for RAM retention.

## 4.6 Flash

The Flash memory is intended primarily for program storage. In-circuit programming allows the operating program to be loaded into the Flash memory after final assembly of the application product. It is possible to program the entire array through the single-wire background debug interface. Because the device does not include on-chip charge pump circuitry, external $V_{PP}$ is required for program and erase operations.

### 4.6.1 Features

Features of the Flash memory include:

- Up to 1000 program/erase cycles at typical voltage and temperature
- Security feature for Flash

### 4.6.2 Flash Programming Procedure

Programming of Flash memory is done on a row basis. A row consists of 64 consecutive bytes starting from addresses $3X00, $3X40, $3X80, or $3XC0. Use the following procedure to program a row of Flash memory:

1. Apply external $V_{PP}$.
2. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
3. Write any data to any Flash location, via the high page accessing window $00C0–$00FF, within the address range of the row to be programmed. (Prior to the data writing operation, the PAGESEL register must be configured correctly to map the high page accessing window to the corresponding Flash row).
4. Wait for a time, $t_{nvs}$.
5. Set the HVEN bit.
6. Wait for a time, $t_{pgs}$.
7. Write data to the Flash location to be programmed.
8. Wait for a time, $t_{prog}$.
9. Repeat steps 7 and 8 until all bytes within the row are programmed.
10. Clear the PGM bit.
11. Wait for a time, $t_{nvh}$.
12. Clear the HVEN bit.
13. After time, $t_{rcv}$, the memory can be accessed in read mode again.
14. Remove external $V_{PP}$.

This program sequence is repeated throughout the memory until all data is programmed.

**NOTE**

Flash memory cannot be programmed or erased by software code executed from Flash locations. To program or erase Flash, commands must be executed from RAM or BDC commands. User code should not enter wait or stop during erase or program sequence.

These operations must be performed in the order shown; other unrelated operations may occur between the steps.

### 4.6.3 Flash Mass Erase Operation

Use the following procedure to mass erase the entire Flash memory:

1. Apply external $V_{PP}$.
2. Set the MASS bit in the Flash control register.

corresponding pulling device enable register bit. The pulling device is also disabled if the pin is controlled by an analog function.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | PTAPE5 | PTAPE4 | 0 | PTAPE2 | PTAPE1 | PTAPE0 |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-4. Internal Pulling Device Enable for Port A Register (PTAPE)**

**Table 6-3. PTAPE Register Field Descriptions**

| Field | Description |
|---|---|
| 5:4,2:0<br>PTAPE[5:4,2:0] | **Internal Pulling Device Enable for Port A Bits** — Each of these control bits determines whether the internal pulling device is enabled for the associated PTA pin. For port A pins that are configured as outputs, these bits have no effect and the internal pullup devices are disabled.<br>0 Internal pulling device disabled for port A bit n.<br>1 Internal pulling device enabled for port A bit n. |

### 6.3.1.2 Pullup/Pulldown Control

Pullup/pulldown control is used to select the pullup or pulldown device enabled by the corresponding PTAPE bit.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | PTAPUD5 | PTAPUD4 | 0 | PTAPUD2 | PTAPUD1 | PTAPUD0 |
| W | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-5. Pullup/Pulldown Device Control for Port A (PTAPUD)**

**Table 6-4. PTAPUD Register Field Descriptions**

| Field | Description |
|---|---|
| 5:4,2:0<br>PTAPUD[5:4,2:0] | **Pullup/Pulldown Device Control for Port A Bits** — Each of these control bits determines whether the internal pullup or pulldown device is selected for the associated PTA pin. The actual pullup/pulldown device is only enabled by enabling the associated PTAPE bit.<br>0 Internal pullup device is selected for port A bit n.<br>1 Internal pulldown device is selected for port A bit n. |

### 6.3.1.3 Output Slew Rate Control Enable

Slew rate control can be enabled for each port pin by setting the corresponding bit in the slew rate control register (PTASEn). When enabled, slew control limits the rate at which an output can transition in order to reduce EMC emissions. Slew rate control has no effect on pins that are configured as inputs.

### 8.3.5 Short Addressing Mode (SRT)

SRT addressing mode is capable of addressing only the first 32 bytes in the address map, from $0000 to $001F. This addressing mode is available for CLR, LDA, and STA instructions. A system can be optimized by placing the most computation-intensive data in this area of memory.

Because the 5-bit address is embedded in the opcode, only the least significant five bits of the address must be included in the instruction; this saves program space and execution time. During execution, the CPU adds nine high-order 0s to the 5-bit operand address and uses the combined 14-bit address ($000x or $001x) to access the intended operand.

### 8.3.6 Direct Addressing Mode (DIR)

DIR addressing mode is used to access operands located in direct address space ($0000 through $00FF).

During execution, the CPU adds six high-order 0s to the low byte of the direct address operand that follows the opcode. The CPU uses the combined 14-bit address ($00xx) to access the intended operand.

### 8.3.7 Extended Addressing Mode (EXT)

In the extended addressing mode, the 14-bit address of the operand is included in the object code in the low-order 14 bits of the next two bytes after the opcode. This addressing mode is only used in JSR and JMP instructions for jump destination address in RS08 MCUs.

### 8.3.8 Indexed Addressing Mode (IX, Implemented by Pseudo Instructions)

Indexed addressing mode is sometimes called indirect addressing mode because an index register is used as a reference to access the intended operand.

An important feature of indexed addressing mode is that the operand address is computed during execution based on the current contents of the X index register located in $000F of the memory map rather than being a constant address location that was determined during program assembly. This allows writing of a program that accesses different operand locations depending on the results of earlier program instructions (rather than accessing a location that was determined when the program was written).

The index addressing mode supported by the RS08 Family uses the register X located at $000F as an index and D[X] register located at $000E as the indexed data register. By programming the index register X, any location in the direct page can be read/written via the indexed data register D[X].

These pseudo instructions can be used with all instructions supporting direct, short, and tiny addressing modes by using the D[X] as the operand.

## 8.4 Special Operations

Most of what the CPU does is described by the instruction set, but a few special operations must be considered, such as how the CPU starts at the beginning of an application program after power is first applied. After the program begins running, the current instruction normally determines what the CPU will do next. Two exceptional events can cause the CPU to temporarily suspend normal program execution:

#### 9.4.1.4 Stop

ICS stop mode is entered whenever the MCU enters stop. In this mode, all ICS clocks are stopped except ICSIRCLK which will remaining running if IREFSTEN is written to a 1.

When the MCU is interrupted from stop, the ICS will go back to the operating mode that was running when the MCU entered stop. If the internal reference was not running in stop (IREFSTEN = 0), the ICS will take some time, $t_{ir\_wu}$, for the internal reference to wakeup. If the internal reference was already running in stop (IREFSTEN = 1), entering into FEI will take some time, $t_{fll\_wu}$, for the FLL to return its previous acquired frequency.

### 9.4.2 Mode Switching

When changing from FBILP to either FEI or FBI, or anytime the trim value is written, the user should wait the FLL acquisition time, $t_{acquire}$, before FLL will be guaranteed to be at desired frequency.

### 9.4.3 Bus Frequency Divider

The BDIV bits can be changed at anytime and the actual switch to the new frequency will occur immediately.

### 9.4.4 Low Power Bit Usage

The low power bit (LP) is provided to allow the FLL to be disabled and thus conserve power when it is not being used. However, in some applications it may be desirable to enable the FLL and allow it to lock for maximum accuracy before switching to an FLL engaged mode. The FLL is disabled in bypass mode when LP = 1.

### 9.4.5 Internal Reference Clock

The ICSIRCLK frequency can be re-targeted by trimming the period of the internal reference clock. This can be done by writing a new value to the TRIM bits in the ICSTRM register. Writing a larger value will slow down the ICSIRCLK frequency, and writing a smaller value to the ICSTRM register will speed up the ICSIRCLK frequency. The TRIM bits will affect the ICSOUT frequency if the ICS is in FLL engaged internal (FEI), FLL bypassed internal (FBI), or FLL bypassed internal low power (FBILP) mode. The TRIM and FTRIM values will not be affected by a reset. For the ICS to run in stop, the LVDE and LVDSE bits in the SPMSC1 must both be set before entering stop.

Until ICSIRCLK is trimmed, ICSOUT frequencies may exceed the maximum chip-level frequency and violate the chip-level clock timing specifications (see the Device Overview chapter). The BDIV is reset to a divide by 2 to prevent the bus frequency from exceeding the maximum. The user should trim the device to an allowable frequency before changing BDIV to a divide by 1 operation.

### 10.1.1 Features

The ACMP has the following features:

- Full rail-to-rail supply operation
- Less than 40 mV of input offset
- Less than 15 mV of hysteresis
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Option to compare to fixed internal bandgap reference voltage
- Option to allow comparator output to be visible on a pin, ACMPO
- Remains operational in stop mode

### 10.1.2 Modes of Operation

This section defines the ACMP operation in wait, stop, and background debug modes.

#### 10.1.2.1 Operation in Wait Mode

The ACMP continues to operate in wait mode if enabled before executing the WAIT instruction. Therefore, the ACMP can be used to bring the MCU out of wait mode if the ACMP interrupt is enabled (ACIE = 1). For lowest possible current consumption, the ACMP should be disabled by software if not required as an interrupt source during wait mode.

#### 10.1.2.2 Operation in Stop Mode

The ACMP continues to operate in stop mode if enabled and compare operation remains active. If ACOPE is enabled, comparator output operates as in the normal operating mode and comparator output is placed onto the external pin. The MCU is brought out of stop when a compare event occurs and ACIE is enabled; ACF flag sets accordingly.

If stop is exited with a reset, the ACMP will be put into its reset state.

#### 10.1.2.3 Operation in Active Background Mode

When the MCU is in active background mode, the ACMP will continue to operate normally.

### 10.1.3 Block Diagram

The block diagram for the analog comparator module is shown in Figure 10-2.

The BDC serial communication protocol requires the host to know the target BDC clock speed. Commands and data are sent most significant bit first (MSB-first) at 16 BDC clock cycles per bit. The interface times out if 512 BDC clock cycles occur between falling edges from the host. Any BDC command that was in progress when this timeout occurs is aborted without affecting the memory or operating mode of the target MCU system.

Figure 12-3 shows an external host transmitting a logic 1 or 0 to the BKGD pin of a target MCU. The host is asynchronous to the target so there is a 0-to-1 cycle delay from the host-generated falling edge to where the target perceives the beginning of the bit time. Ten target BDC clock cycles later, the target senses the bit level on the BKGD pin. Typically, the host actively drives the pseudo-open-drain BKGD pin during host-to-target transmissions to speed up rising edges. Because the target does not drive the BKGD pin during the host-to-target period, there is no need to treat the line as an open-drain signal during this period.

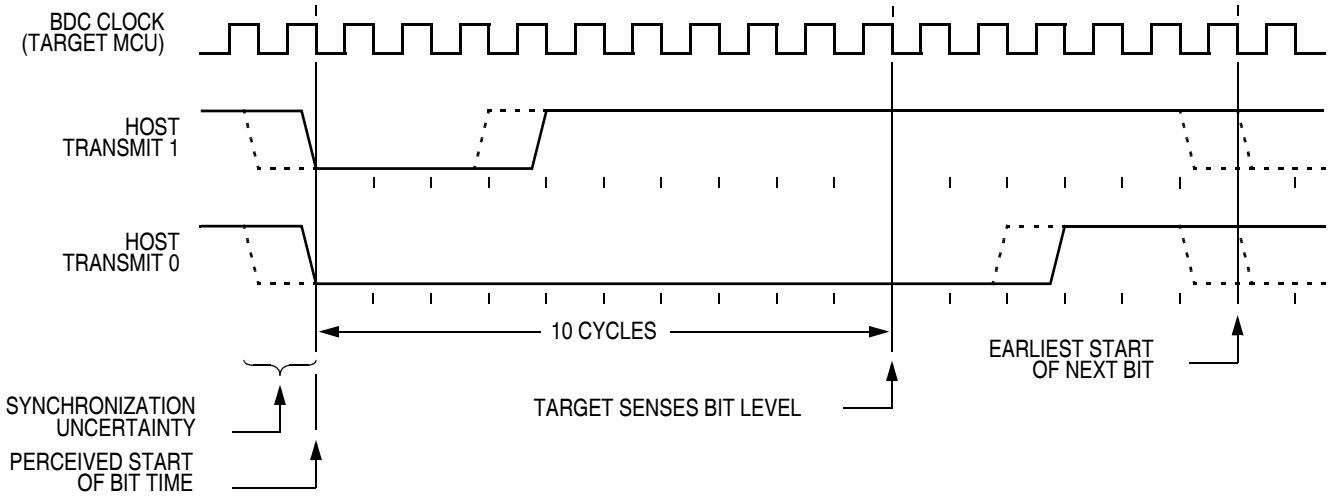


**Figure 12-3. BDC Host-to-Target Serial Bit Timing**

Figure 12-4 shows the host receiving a logic 1 from the target MCU. Because the host is asynchronous to the target, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target. The host holds the BKGD pin low long enough for the target to recognize it (at least two target BDC cycles). The host must release the low drive before the target drives a brief active-high speedup pulse seven cycles after the perceived start of the bit time. The host must sample the bit level approximately 10 cycles after it started the bit time.

- Subsequent bits must occur within 512 BDC cycles of the last bit sent.

## 12.4 BDC Registers and Control Bits

The BDC contains two non-CPU accessible registers:

- The BDC status and control register (BDCSCR) is an 8-bit register containing control and status bits for the background debug controller.
- The BDC breakpoint register (BDCBKPT) holds a 16-bit breakpoint match address.

These registers are accessed with dedicated serial BDC commands and are not located in the memory space of the target MCU (so they do not have addresses and cannot be accessed by user programs).

Some of the bits in the BDCSCR have write limitations; otherwise, these registers may be read or written at any time. For example, the ENBDM control bit may not be written while the MCU is in active background mode. This prevents the ambiguous condition of the control bit forbidding active background mode while the MCU is already in active background mode. Also, the status bits (BDMACT, WS, and WSF) are read-only status indicators and can never be written by the WRITE_CONTROL serial BDC command.

### 12.4.1 BDC Status and Control Register (BDCSCR)

This register can be read or written by serial BDC commands (READ_STATUS and WRITE_CONTROL) but is not accessible to user programs because it is not located in the normal memory map of the MCU.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | ENBDM | BDMACT | BKPTEN | FTS | 0 | WS | WSF | 0 |
| W | | | | | | | | |
| Normal Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset in Active BDM: | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 12-6. BDC Status and Control Register (BDCSCR)**

**Table 12-1. BDCSCR Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>ENBDM | **Enable BDM (Permit Active Background Mode)** — Typically, this bit is written to 1 by the debug host shortly after the beginning of a debug session or whenever the debug host resets the target and remains 1 until a normal reset clears it. If the application can go into stop mode, this bit is required to be set if debugging capabilities are required.<br>0 BDM cannot be made active (non-intrusive commands still allowed).<br>1 BDM can be made active to allow active background mode commands. |
| 6<br>BDMACT | **Background Mode Active Status** — This is a read-only status bit.<br>0 BDM not active (user application program running).<br>1 BDM active and waiting for serial commands. |

# Appendix A
# Electrical Characteristics

## A.1 Introduction

This chapter contains electrical and timing specifications.

## A.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table A-1 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either $V_{SS}$ or $V_{DD}$) or the programmable pull-up resistor associated with the pin is enabled.

**Table A-1. Absolute Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | –0.3 to +5.8 | V |
| Maximum current into $V_{DD}$ | $I_{DD}$ | 120 | mA |
| Digital input voltage | $V_{In}$ | –0.3 to $V_{DD}$ + 0.3 | V |
| Instantaneous maximum current<br>Single pin limit (applies to all port pins)[1, 2, 3] | $I_D$ | ± 25 | mA |
| Storage temperature range | $T_{stg}$ | –55 to 150 | °C |

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ($V_{DD}$) and negative ($V_{SS}$) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to $V_{SS}$ and $V_{DD}$ except the $\overline{\text{RESET}}/V_{PP}$ pin which is internally clamped to $V_{SS}$ only.

3 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. A-2}$$

Solving Equation A-1 and Equation A-2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. A-3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation A-3 by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations 1 and 2 iteratively for any value of $T_A$.

## A.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage. All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table A-3. ESD Protection Characteristics**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| ESD Target for Machine Model (MM)<br>MM circuit description | $V_{THMM}$ | 200 | V |
| ESD Target for Human Body Model (HBM)<br>HBM circuit description | $V_{THHBM}$ | 2000 | V |

## A.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

**Table A-4. DC Characteristics**
**(Temperature Range = –40 to 85°C Ambient)**

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage (run, wait and stop modes.)<br>$0 < f_{Bus} < 10MHz$ | $V_{DD}$ | 1.8 | — | 5.5 | V |
| Minimum RAM retention supply voltage applied to $V_{DD}$ | $V_{RAM}$ | 0.8 [1] | — | — | V |
| Low-voltage Detection threshold<br>($V_{DD}$ falling)<br>($V_{DD}$ rising) | $V_{LVD}$ | 1.80<br>1.88 | 1.86<br>1.94 | 1.95<br>2.03 | V |
| Power on RESET (POR) voltage | $V_{POR}$ | 0.9 | 1.4 | 1.7 | V |
| Input high voltage ($V_{DD} > 2.3V$) (all digital inputs) | $V_{IH}$ | $0.70 \times V_{DD}$ | — | — | V |
| Input high voltage ($1.8\ V \le V_{DD} \le 2.3\ V$) (all digital inputs) | $V_{IH}$ | $0.85 \times V_{DD}$ | — | — | V |

**Table A-4. DC Characteristics (continued)**
**(Temperature Range = –40 to 85°C Ambient)**

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Input low voltage ($V_{DD}$ > 2.3 V) (all digital inputs) | $V_{IL}$ | — | — | 0.30 × $V_{DD}$ | V |
| Input low voltage (1.8 V ≤ $V_{DD}$ ≤ 2.3 V) (all digital inputs) | $V_{IL}$ | — | — | 0.30 × $V_{DD}$ | V |
| Input hysteresis (all digital inputs) | $V_{hys}$ | 0.06 × $V_{DD}$ | — | — | V |
| Input leakage current (per pin) $V_{In}$ = $V_{DD}$ or $V_{SS}$, all input only pins | $\lvert I_{In} \rvert$ | — | 0.025 | 1.0 | µA |
| High impedance (off-state) leakage current (per pin) $V_{In}$ = $V_{DD}$ or $V_{SS}$, all input/output | $\lvert I_{OZ} \rvert$ | — | 0.025 | 1.0 | µA |
| Internal pullup/pulldown resistors[2] (all port pins) | $R_{PU}$ | 20 | 45 | 65 | kΩ |
| Output high voltage (port A)<br>$I_{OH}$ = –5 mA ($V_{DD}$ ≥ 4.5 V)<br>$I_{OH}$ = –3 mA ($V_{DD}$ ≥ 3 V)<br>$I_{OH}$ = –2 mA ($V_{DD}$ ≥ 1.8 V) | $V_{OH}$ | $V_{DD}$ – 0.8 | — | —<br>—<br>— | V |
| Maximum total $I_{OH}$ for all port pins | $\lvert I_{OHT} \rvert$ | — | — | 40 | mA |
| Output low voltage (port A)<br>$I_{OL}$ = 5 mA ($V_{DD}$ ≥ 4.5 V)<br>$I_{OL}$ = 3 mA ($V_{DD}$ ≥ 3 V)<br>$I_{OL}$ = 2 mA ($V_{DD}$ ≥ 1.8 V) | $V_{OL}$ | — | — | 0.8<br>0.8<br>0.8 | V |
| Maximum total $I_{OL}$ for all port pins | $I_{OLT}$ | — | — | 40 | mA |
| dc injection current[3, 4, 5 6]<br>$V_{In}$ < $V_{SS}$, $V_{In}$ > $V_{DD}$<br>Single pin limit<br>Total MCU limit, includes sum of all stressed pins | $\lvert I_{IC} \rvert$ | — | — | <br>0.2<br>0.8 | <br>mA<br>mA |
| Input capacitance (all non-supply pins) | $C_{In}$ | — | — | 7 | pF |

1 This parameter is characterized and not tested on each device.

2 Measurement condition for pull resistors: $V_{In}$ = $V_{SS}$ for pullup and $V_{In}$ = $V_{DD}$ for pulldown.

3 All functional non-supply pins are internally clamped to $V_{SS}$ and $V_{DD}$ except the $\overline{\text{RESET}}$/$V_{PP}$ which is internally clamped to $V_{SS}$ only.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In}$ > $V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

6 This parameter is characterized and not tested on each device.