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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	HCS08
Core Size	8-Bit
Speed	48MHz
Connectivity	LINbus, SCI, SPI, USB
Peripherals	LVD, POR, PWM
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN-EP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08js16cfk

MC9S08JS16

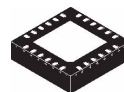
MC9S08JS16 Series

Covers:

MC9S08JS16
MC9S08JS8
MC9S08JS16L
MC9S08JS8L



20 W-SOIC
Case 751D



24 QFN
Case 1982-01

Features:

- 8-Bit HCS08 Central Processor Unit (CPU)
 - 48 MHz HCS08 CPU (central processor unit)
 - 24 MHz internal bus frequency
 - Support for up to 32 interrupt/reset sources
- Memory Options
 - Up to 16 KB of on-chip in-circuit programmable flash memory with block protection and security options
 - Up to 512 bytes of on-chip RAM
 - 256 bytes of USB RAM
- Clock Source Options
 - Clock source options include crystal, resonator, external clock
 - MCG (multi-purpose clock generator) — PLL and FLL; internal reference clock with trim adjustment
- System Protection
 - Optional computer operating properly (COP) reset with option to run from independent 1 kHz internal clock source or the bus clock
 - Low-voltage detection
 - Illegal opcode detection with reset
 - Illegal address detection with reset
- Power-Saving Modes
 - Wait plus two stops
- USB Bootload
 - Mass erase entire flash array
 - Partial erase flash array — erase all flash blocks except for the first 1 KB of flash
 - Program flash
- Peripherals
 - **USB** — USB 2.0 full-speed (12 Mbps) with dedicated on-chip 3.3 V regulator and transceiver; supports endpoint 0 and up to 6 additional endpoints
 - **SPI** — One 8- or 16-bit selectable serial peripheral interface module with a receive data buffer hardware match function
 - **SCI** — One serial communications interface module with optional 13 bit break. Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
 - **MTIM** — One 8-bit modulo counter with 8-bit prescaler and overflow interrupt
 - **TPM** — One 2-channel 16-bit timer/pulse-width modulator (TPM) module; selectable input capture, output compare, and edge-aligned PWM capability on each channel; timer module may be configured for buffered, centered PWM (CPWM) on all channels
 - **KBI** — 8-pin keyboard interrupt module
 - **RTC** — Real-time counter with binary- or decimal-based prescaler
 - **CRC** — Hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16}+x^{12}+x^5+1$ polynomial
- Input/Output
 - Software selectable pullups on ports when used as inputs
 - Software selectable slew rate control on ports when used as outputs
 - Software selectable drive strength on ports when used as outputs
 - Master reset pin and power-on reset (POR)
 - Internal pullup on RESET, IRQ, and BKGD/MS pins to reduce customer system cost
- Package Options
 - 24-pin quad flat no-lead (QFN)
 - 20-pin small outline IC package (SOIC)

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	9/1/2008	Initial public released
2	1/8/2009	In Table 7 , changed the parameter description of RI_{DD} and $S3I_{DD}$, the typicals of RI_{DD} were changed as well.
3	3/9/2009	Corrected the 24-pin QFN case number and doc. number information.
4	4/24/2009	Added new parts information about MC9S08JS16L and MC9S08JS8L.

Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9S08JS16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9S08JS16 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number (Package)		<-- Lowest Priority --> Highest		
24 (QFN)	20 (SOIC)	Port Pin	Alt 1	Alt 2
1	4	PTB0	IRQ	TCLK
2	5	PTB1		RESET
3	6	PTB2	BKGD	MS
4	7	PTB3		BLMS
5	8	PTA0	KBIP0	TPMCH0
6	—	NC		
7	9	PTA1	KBIP1	MISO
8	10	PTA2	KBIP2	MOSI
9	11	PTA3	KBIP3	SPSCK
10	12	PTA4	KBIP4	SS
11	13			V _{DD}
12	—	NC		
13	14			V _{SS}
14	15			USBDN
15	16			USBDP
16	17			V _{USB33}
17	18	PTA5	KBIP5	TPMCH1
18	—	NC		
19	19	PTA6	KBIP6	RxD
20	20	PTA7	KBIP7	TxD
21	1	PTB4	XTAL	
22	2	PTB5	EXTAL	
23	3			V _{SSOSC}
24	—	NC		

3 Electrical Characteristics

This chapter contains electrical and timing specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The above classifications are used in the column labeled “C” in applicable tables of this data sheet.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the limits specified in [Table 3](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	2.7 to 5.5	V
Input voltage	V_{In}	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	± 25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	-55 to 150	°C
Maximum junction temperature	T_J	150	°C

Electrical Characteristics

$P_D = P_{int} + P_{I/O}P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

3.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage. This device was qualified to AEC-Q100 Rev E. A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD Protection Characteristics

Parameter	Symbol	Value	Unit
ESD Target for Machine Model (MM) — MM circuit description	V_{THMM}	200	V
ESD Target for Human Body Model (HBM) — HBM circuit description	V_{THHBM}	2000	V

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 6. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1		Operating voltage ²	—	2.7	—	5.5	V

Table 6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, I _{Load} = -2 mA 3 V, I _{Load} = -0.6 mA 5 V, I _{Load} = -0.4 mA 3 V, I _{Load} = -0.24 mA	V _{OH}	V _{DD} - 1.5 V _{DD} - 1.5 V _{DD} - 0.8 V _{DD} - 0.8	— — — —	— — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I _{Load} = -10 mA 3 V, I _{Load} = -3 mA 5 V, I _{Load} = -2 mA 3 V, I _{Load} = -0.4 mA		V _{DD} - 1.5 V _{DD} - 1.5 V _{DD} - 0.8 V _{DD} - 0.8	— — — —	— — — —	
3	P	Output low voltage — Low drive (PTxDSn = 0) 5 V, I _{Load} = 2 mA 3 V, I _{Load} = 0.6 mA 5 V, I _{Load} = 0.4 mA 3 V, I _{Load} = 0.24 mA	V _{OL}	1.5 1.5 0.8 0.8	— — — —	— — — —	V
		Output low voltage — High drive (PTxDSn = 1) 5 V, I _{Load} = 10 mA 3 V, I _{Load} = 3 mA 5 V, I _{Load} = 2 mA 3 V, I _{Load} = 0.4 mA		1.5 1.5 0.8 0.8	— — — —	— — — —	
4	P	Output high current — Max total I _{OH} for all ports 5 V 3 V	I _{OHT}	— —	— —	100 60	mA
5	P	Output low current — Max total I _{OL} for all ports 5 V 3 V	I _{OLT}	— —	— —	100 60	mA
6	P	Input high voltage; all digital inputs	V _{IH}	0.65 × V _{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V _{IL}	—	—	0.35 × V _{DD}	
8	P	Input hysteresis; all digital inputs	V _{hys}	0.06 × V _{DD}	—	—	mV
9	P	Input leakage current; input only pins ³	I _{IN}	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current ³	I _{OZ}	—	0.1	1	μA
11	P	Internal pullup resistors ⁴	R _{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors ⁵	R _{PD}	20	45	65	kΩ
13	C	Internal pullup resistor to USB DP (to V _{USB33}) Idle Transmit	R _{PUPD}	900 1425	— —	1575 3090	kΩ
14	C	Input capacitance; all non-supply pins	C _{IN}	—	—	8	pF
15	C	RAM retention voltage	V _{RAM}	0.6	1.0	—	V
16	P	POR rearm voltage	V _{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t _{POR}	10	—	—	μs

Table 6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	3.9 4.0	4.0 4.1	4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	2.48 2.54	2.56 2.62	2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	4.5 4.6	4.6 4.7	4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	4.2 4.3	4.3 4.4	4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	2.84 2.90	2.92 2.98	3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	2.66 2.72	2.74 2.80	2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	— —	100 60	— —	mV

¹ Typical values are based on characterization data at 25 °C unless otherwise stated.

² Operating voltage with USB enabled can be found in [Section 3.11, “USB Electricals.”](#)

³ Measured with $V_{In} = V_{DD}$ or V_{SS} .

⁴ Measured with $V_{In} = V_{SS}$.

⁵ Measured with $V_{In} = V_{DD}$.

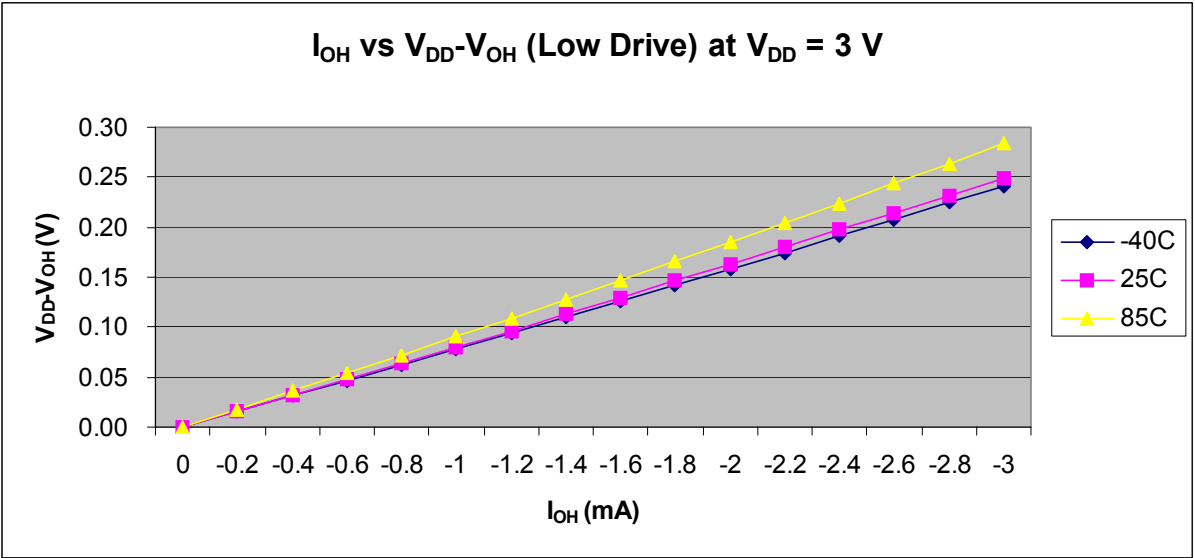


Figure 4. Typical I_{OH} (Low Drive) vs $V_{DD}-V_{OH}$ at $V_{DD} = 3\text{ V}$

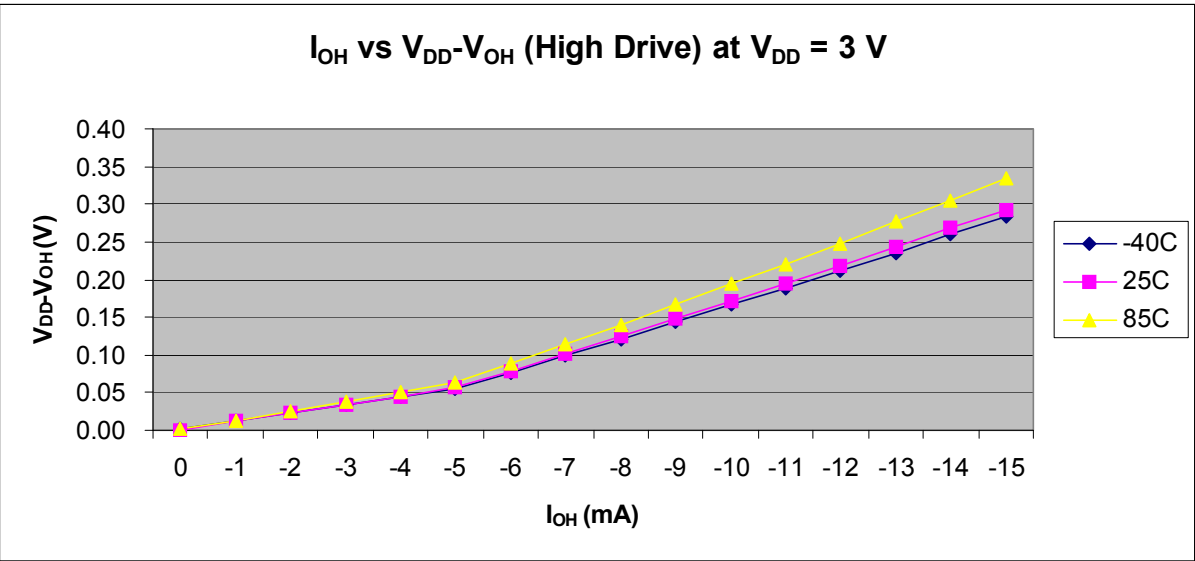


Figure 5. Typical I_{OH} (High Drive) vs $V_{DD}-V_{OH}$ at $V_{DD} = 3\text{ V}$

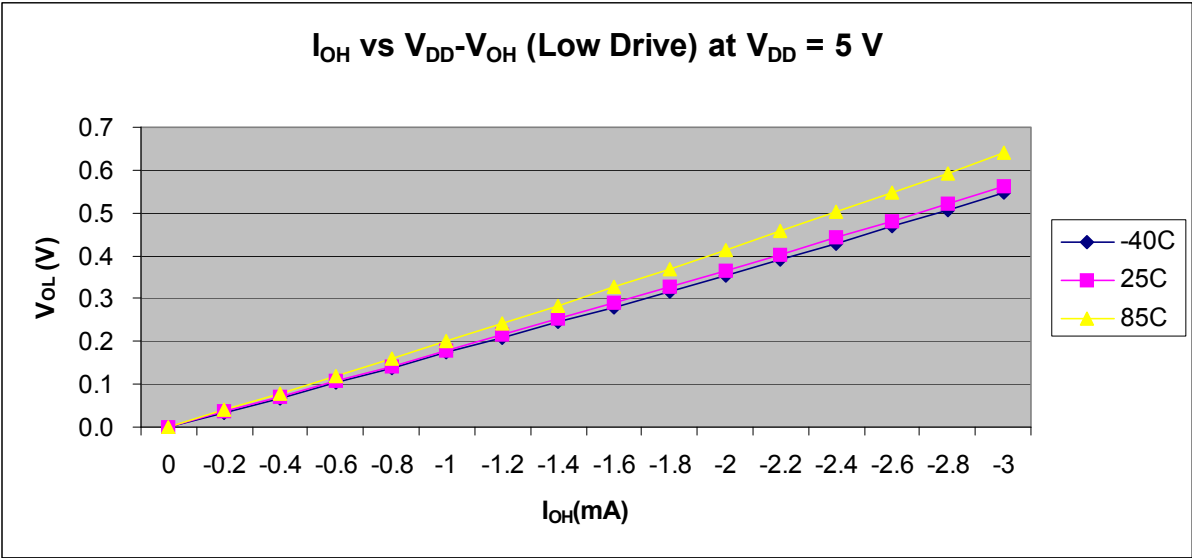


Figure 6. Typical I_{OH} (Low Drive) vs $V_{DD}-V_{OH}$ at $V_{DD} = 5\text{ V}$

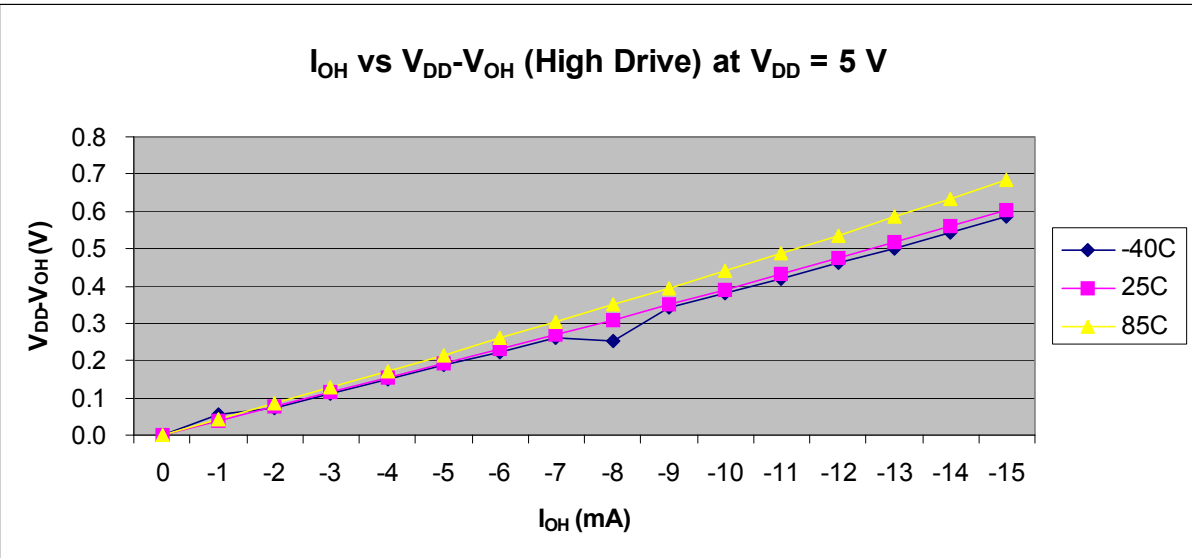


Figure 7. Typical I_{OH} (High Drive) vs $V_{DD}-V_{OH}$ at $V_{DD} = 5\text{ V}$

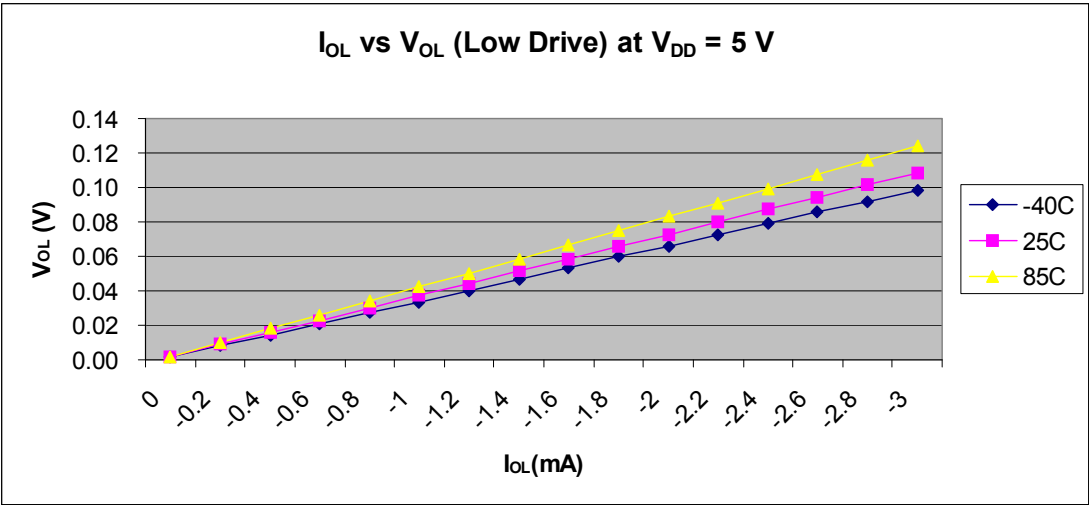


Figure 8. I_{OL} vs V_{OL} (Low Drive) at $V_{DD} = 5\text{ V}$

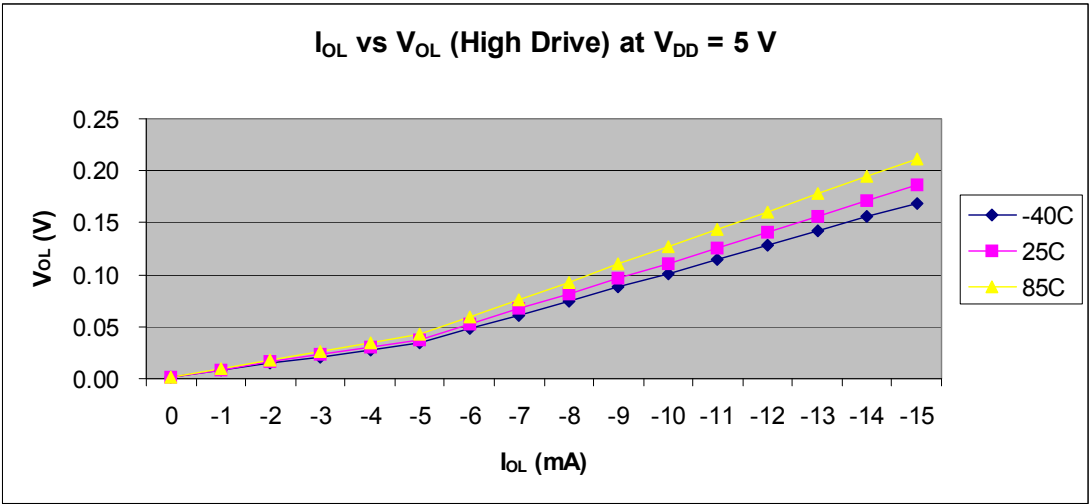


Figure 9. I_{OL} vs V_{OL} (High Drive) at $V_{DD} = 5\text{ V}$

3.6 Supply Current Characteristics

Table 7. Supply Current Characteristics

Num	C	Parameter	Symbol	V _{DD} (V)	Typical ¹	Max ²	Unit
1	C	Run supply current ³ measured at (CPU clock = 2 MHz, f _{BUS} = 1 MHz, BLPE mode)	R _I DD	5	1.03	—	mA
				3	0.83	—	
2	P	Run supply current ³ measured at (CPU clock = 48 MHz, f _{BUS} = 24 MHz, PEE mode, all module on)	R _I DD	5	19.93	—	mA
				3	18.74	—	
3	P	Stop2 mode supply current	S2I _{DD}	5	1.36	—	μA
				3	1.18	—	μA
4	P	Stop3 mode supply current, all module off	S3I _{DD}	5	1.50	—	μA
				3	1.31	—	μA
5	P	RTC adder to stop2 or stop3 ³ , 25 °C	ΔI _{SRTC}	5	300	—	nA
				3	300	—	nA
6	P	LVD adder to stop3 (LVDE = LVDSE = 1)	ΔI _{SLVD}	5	106.7	—	μA
				3	95.6	—	μA
7	P	Adder to stop3 for oscillator enabled ⁴ (ERCLKEN = 1 and EREFSTEN = 1)	ΔI _{SOSC}	5	5.6	—	μA
				3	5.3	—	μA
8	T	USB module enable current ⁵	ΔI _{USBE}	5	1.5	—	mA
9	T	USB suspend current ⁶	I _{SUSP}	5	273.3	—	μA

¹ Typicals are measured at 25 °C. See Figure 12 through Figure 10 for typical curves across voltage/temperature.

² Values given here are preliminary estimates prior to completing characterization.

³ Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 560 μA at 5 V and 422 μA at 3 V with f_{BUS} = 1 MHz.

⁴ Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

⁵ Here USB module is enabled and clocked at 48 MHz (USBEN = 1, USBVREN = 1, USBPHYEN = 1 and USBPU = 1), and D+ and D– pulled down by two 15.1 kΩ resistors independently. The current consumption may be much higher when the packets are being transmitted through the attached cable.

⁶ MCU enters stop3 mode, USB bus in idle state. The USB suspend current will be dominated by the D+ pullup resistor.

3.8 MCG Specifications

Table 9. MCG Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	—	39.0625	kHz
3	T	Internal reference startup time	t_{irefst}	—	60	100	μs
4	C	DCO output frequency range — untrimmed	f_{dco_ut}	25.6	33.48	42.66	MHz
5	P	DCO output frequency range — trimmed	f_{dco_t}	32	—	40	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco_res_t}$	—	±0.1	±0.2	% f_{dco}
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco_res_t}$	—	±0.2	±0.4	% f_{dco}
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	% f_{dco}
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C	Δf_{dco_t}	—	±0.5	±1	% f_{dco}
10	C	FLL acquisition time ¹	$t_{fll_acquire}$	—	—	1	ms
11	D	PLL acquisition time ²	$t_{pll_acquire}$	—	—	1	ms
12	C	Long term Jitter of DCO output clock (averaged over 2ms interval) ³	C_{Jitter}	—	0.02	0.2	% f_{dco}
13	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
14	D	PLL reference frequency range	f_{pll_ref}	1.0	—	2.0	MHz
15	T	Long term accuracy of PLL output clock (averaged over 2 ms)	$f_{pll_jitter_2ms}$	—	0.590 ⁴	—	%
16	T	Jitter of PLL output clock measured over 625 ns ⁵	$f_{pll_jitter_625ns}$	—	0.566 ⁴	—	%
17	D	Lock entry frequency tolerance ⁶	D_{lock}	±1.49	—	±2.98	%
18	D	Lock exit frequency tolerance ⁷	D_{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t_{fll_lock}	—	—	$t_{fll_acquire} + 1075(1/f_{int_t})$	s
20	D	Lock time — PLL	t_{pll_lock}	—	—	$t_{pll_acquire} + 1075(1/f_{pll_ref})$	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f_{loc_low}	(3/5) × f_{int}	—	—	kHz
22	D	Loss of external clock minimum frequency — RANGE = 1	f_{loc_high}	(16/5) × f_{int}	—	—	kHz

¹ This specification applies any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

² This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

- ³ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.
- ⁴ Jitter measurements are based upon a 48 MHz clock frequency.
- ⁵ 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.
- ⁶ Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.
- ⁷ Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.1 Control Timing

Figure 13. Control Timing

Num	C	Parameter	Symbol	Min	Typical ¹	Max	Unit
1	D	Bus frequency ($t_{\text{cyc}} = 1/f_{\text{BUS}}$)	f_{BUS}	DC	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width ² ($t_{\text{cyc}} = 1/f_{\text{Self_reset}}$)	t_{extrst}	$1.5 \times t_{\text{Self_reset}}$	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$66 \times t_{\text{cyc}}$	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	25	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	25	—	—	ns
7	D	IRQ pulse width Asynchronous path ² Synchronous path ³	$t_{\text{ILIH}}, t_{\text{IHIL}}$	100 $1.5 \times t_{\text{cyc}}$	—	—	ns
8	D	KBIPx pulse width Asynchronous path ² Synchronous path ³	$t_{\text{ILIH}}, t_{\text{IHIL}}$	100 $1.5 \times t_{\text{cyc}}$	—	—	ns
9	C	Port rise and fall time (load = 50 pF) ⁴ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{\text{Rise}}, t_{\text{Fall}}$	— —	3 30	— —	ns

¹ Typical values are based on characterization data at $V_{\text{DD}} = 5.0 \text{ V}$, 25°C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ This is the minimum pulse width guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40°C to 85°C .

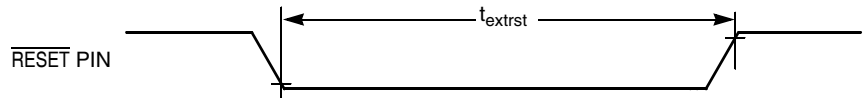


Figure 14. Reset Timing

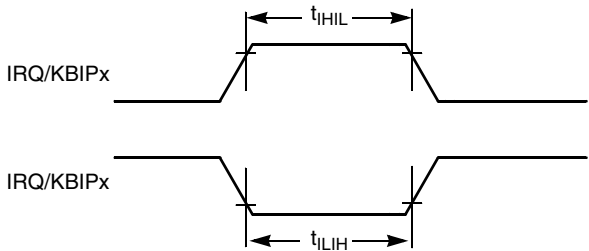


Figure 15. IRQ/KBIPx Timing

3.9.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 10. TPM Input Timing

Num	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	dc	$f_{\text{Bus}}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

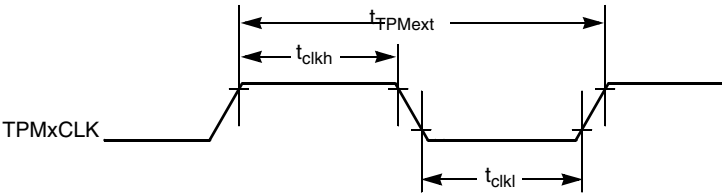


Figure 16. Timer External Clock

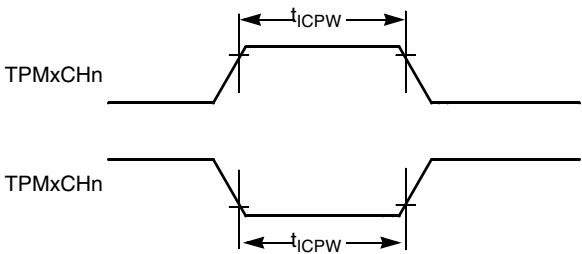


Figure 17. Timer Input Capture Pulse

3.10 SPI Characteristics

Table 11 and Figure 18 through Figure 21 describe the timing requirements for the SPI system.

Table 11. SPI Electrical Characteristic

Num ¹	C	Characteristic ²	Symbol	Min	Typical	Max	Unit
1	D	Operating frequency ³ Master Slave	f_{op} f_{op}	$f_{Bus}/2048DC$	— —	$f_{Bus}/2$ $f_{Bus}/4$	Hz
2	D	Cycle time Master Slave	t_{SCK} t_{SCK}	2 4	— —	2048 —	t_{cyc}
3	D	Enable lead time Master Slave	t_{Lead} t_{Lead}	— —	1/2 1/2	— —	t_{SCK}
4	D	Enable lag time Master Slave	t_{Lag} t_{Lag}	— —	1/2 1/2	— —	t_{SCK}
5	D	Clock (SPSCK) high time Master Slave	t_{SCKH}	— $1/2 t_{SCK} - 25$	$1/2 t_{SCK}$ $1/2 t_{SCK}$	— —	ns
6	D	Clock (SPSCK) low time Master Slave	t_{SCKL}	— $1/2 t_{SCK} - 25$	$1/2 t_{SCK}$ $1/2 t_{SCK}$	— —	ns
7	D	Data setup time (inputs) Master Slave	$t_{SI(M)}$ $t_{SI(S)}$	30 30	— —	— —	ns
8	D	Data hold time (inputs) Master Slave	$t_{HI(M)}$ $t_{HI(S)}$	30 30	— —	— —	ns
9	D	Access time, slave ⁴	t_A	—	—	40	ns
10	D	Disable time, slave ⁵	t_{dis}	—	—	40	ns
11	D	Data setup time (outputs) Master Slave	t_{SO} t_{SO}	— —	— —	25 25	ns
12	D	Data hold time (outputs) Master Slave	t_{HO} t_{HO}	-10 -10	— —	— —	ns

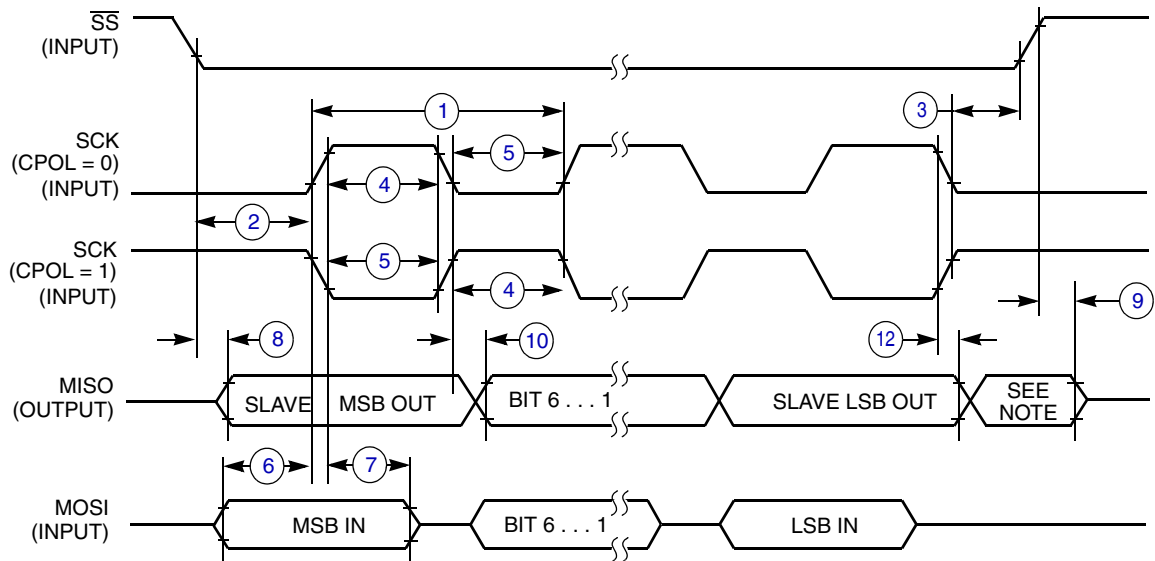
¹ Refer to Figure 18 through Figure 21.

² All timing is shown with respect to 20% V_{DD} and 80% V_{DD} , unless noted; 50 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

³ The maximum frequency is 8 MHz when input filter on SPI pins is disabled.

⁴ Time to data active from high-impedance state.

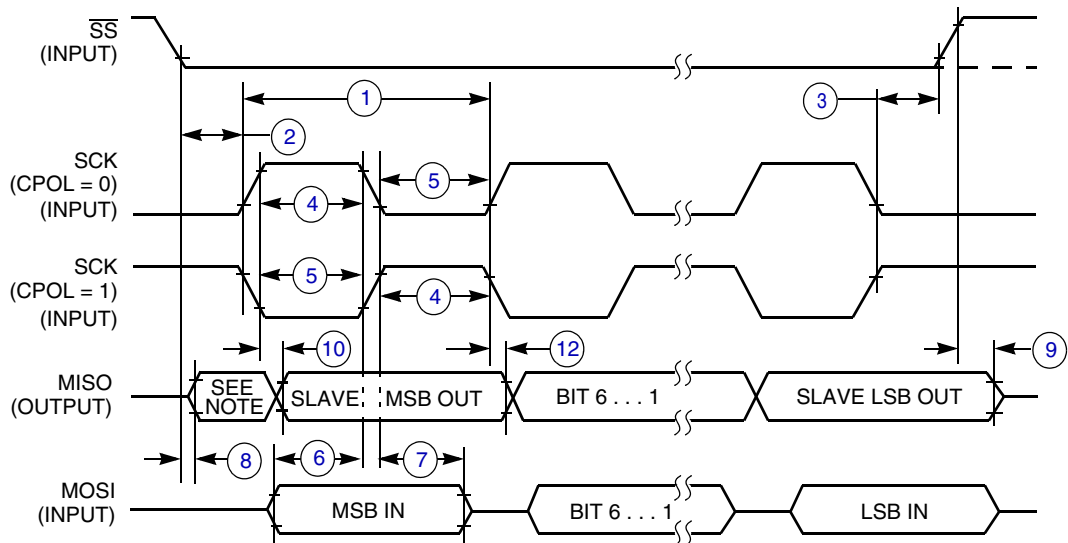
⁵ Hold time to high-impedance state.



NOTE:

1. Not defined but normally MSB of character just received

Figure 20. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 21. SPI Slave Timing (CPHA = 1)

3.11 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. Program and erase operations do not require any special power sources other than the normal V_{DD} supply.



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