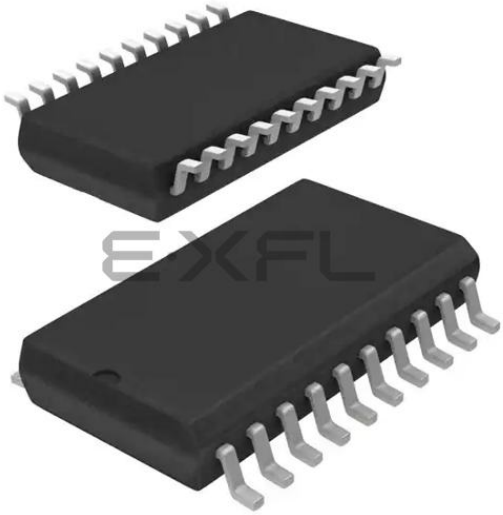

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	48MHz
Connectivity	LINbus, SCI, SPI, USB
Peripherals	LVD, POR, PWM
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08js16cwj

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	9/1/2008	Initial public released
2	1/8/2009	In Table 7, changed the parameter description of RI_{DD} and $S3I_{DD,}$ the typicals of RI_{DD} were changed as well.
3	3/9/2009	Corrected the 24-pin QFN case number and doc. number information.
4	4/24/2009	Added new parts information about MC9S08JS16L and MC9S08JS8L.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08JS16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 85	°C
Thermal resistance [1,2,3,4]			
24-pin QFN			
1s	θ_{JA}	92	°C/W
2s2p		33	
20-pin SOIC			
1s		86	
2s2p		58	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

Table 6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA 5 V, I_{Load} = –0.4 mA 3 V, I_{Load} = –0.24 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA 5 V, I_{Load} = 0.4 mA 3 V, I_{Load} = 0.24 mA	V_{OL}	 1.5 1.5 0.8 0.8	 — — — —	 — — — —	V
		Output low voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.4 mA		 1.5 1.5 0.8 0.8	 — — — —	 — — — —	
4	P	Output high current — Max total I_{OH} for all ports 5 V 3 V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs	V_{IH}	0.65 × V_{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 × V_{DD}	
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 × V_{DD}	—	—	mV
9	P	Input leakage current; input only pins[3]	$\|I_{In}\|$	—	0.1	1	µA
10	P	High Impedance (off-state) leakage current[3]	$\|I_{OZ}\|$	—	0.1	1	µA
11	P	Internal pullup resistors[4]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[5]	R_{PD}	20	45	65	kΩ
13	C	Internal pullup resistor to USBDP (to V_{USB33}) Idle Transmit	R_{PUPD}	 900 1425	 — —	 1575 3090	kΩ
14	C	Input capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	C	RAM retention voltage	V_{RAM}	0.6	1.0	—	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	µs

Table 6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	 — —	 100 60	 — —	mV

1 Typical values are based on characterization data at 25 °C unless otherwise stated.

2 Operating voltage with USB enabled can be found in Section 3.11, “USB Electricals.”

3 Measured with $V_{In} = V_{DD}$ or V_{SS}.

4 Measured with $V_{In} = V_{SS}$.

5 Measured with $V_{In} = V_{DD}$.

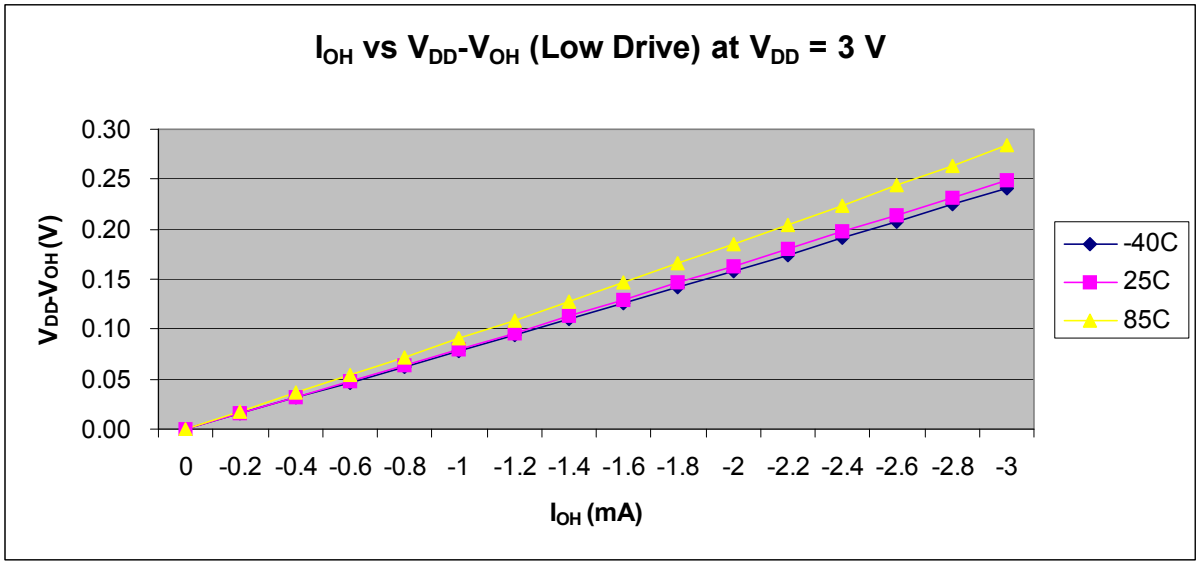


Figure 4. Typical I_{OH} (Low Drive) vs V_{DD}–V_{OH} at V_{DD} = 3 V

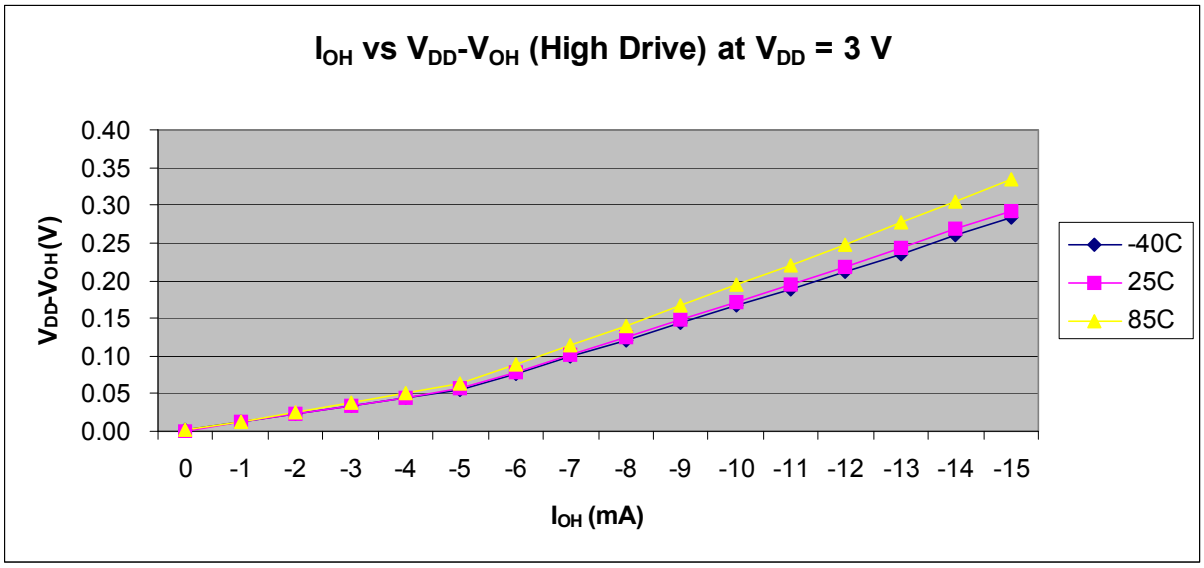


Figure 5. Typical I_{OH} (High Drive) vs V_{DD}–V_{OH} at V_{DD} = 3 V

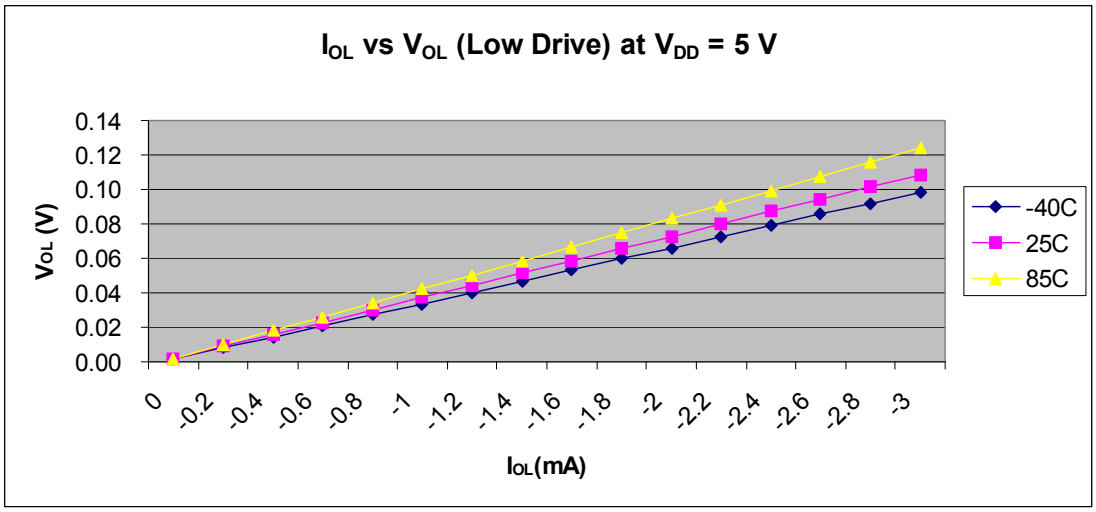


Figure 8. I_{OL} vs V_{OL} (Low Drive) at V_{DD} = 5 V

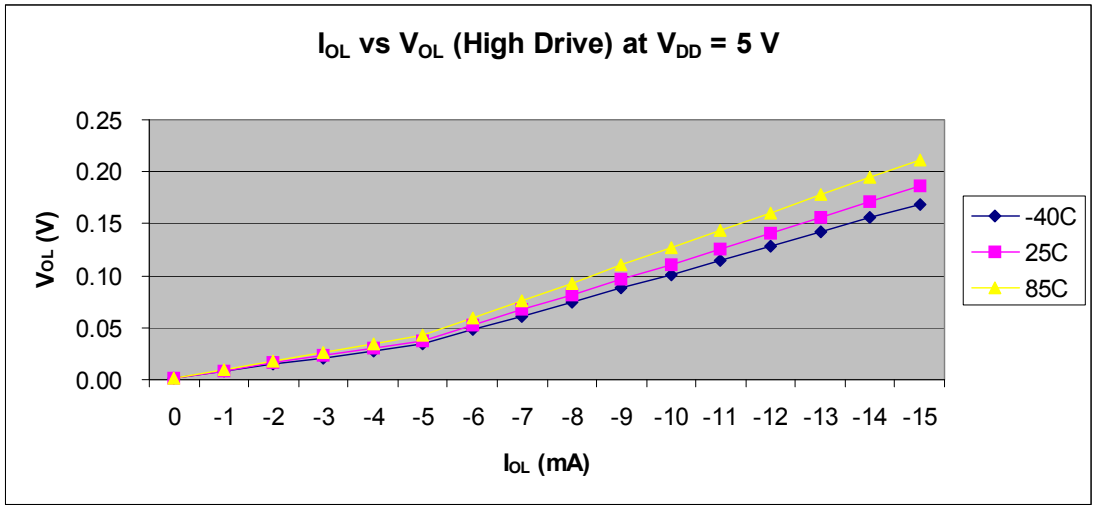


Figure 9. I_{OL} vs V_{OL} (High Drive) at V_{DD} = 5 V

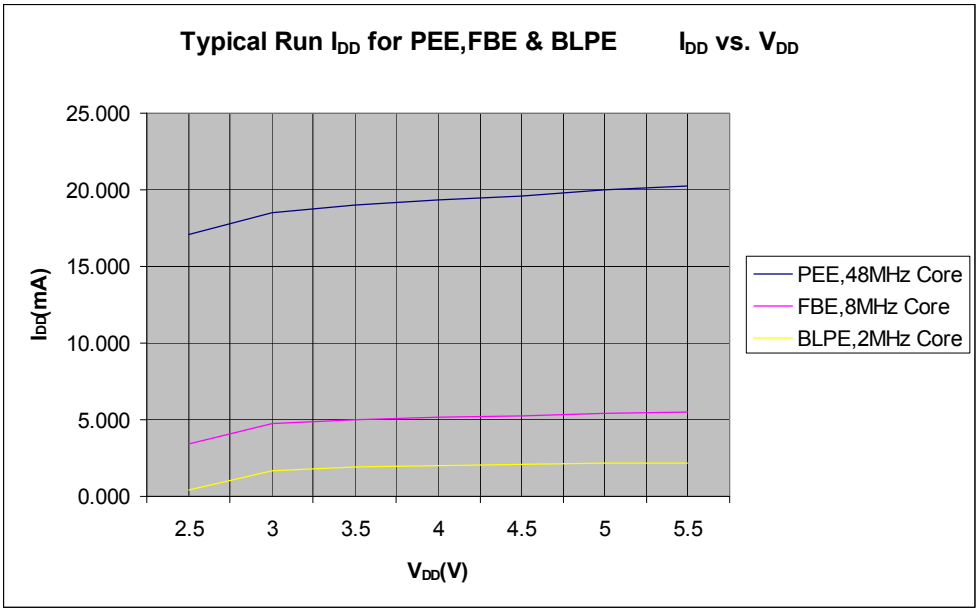


Figure 12. Typical Run I_{DD} for PEE, FBE and BLPE Modes (I_{DD} vs. V_{DD})

3.8 MCG Specifications

Table 9. MCG Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	—	39.0625	kHz
3	T	Internal reference startup time	t_{irefst}	—	60	100	µs
4	C	DCO output frequency range — untrimmed	f_{dco_ut}	25.6	33.48	42.66	MHz
5	P	DCO output frequency range — trimmed	f_{dco_t}	32	—	40	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[1]	$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time[2]	$t_{pll\_acquire}$	—	—	1	ms
12	C	Long term Jitter of DCO output clock (averaged over 2ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
14	D	PLL reference frequency range	f_{pll_ref}	1.0	—	2.0	MHz
15	T	Long term accuracy of PLL output clock (averaged over 2 ms)	$f_{pll\_jitter\_2ms}$	—	0.590[4]	—	%
16	T	Jitter of PLL output clock measured over 625 ns[5]	$f_{pll\_jitter\_625ns}$	—	0.566[4]	—	%
17	D	Lock entry frequency tolerance[6]	D_{lock}	±1.49	—	±2.98	%
18	D	Lock exit frequency tolerance[7]	D_{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
20	D	Lock time — PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f_{loc_low}	(3/5) x f_{int}	—	—	kHz
22	D	Loss of external clock minimum frequency — RANGE = 1	f_{loc_high}	(16/5) x f_{int}	—	—	kHz

1 This specification applies any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

2 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

4 Jitter measurements are based upon a 48 MHz clock frequency.

5 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

6 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

7 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.1 Control Timing

Figure 13. Control Timing

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	$1.5 \times t_{Self\_reset}$	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	25	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	25	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	—	—	ns
8	D	KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	—	—	ns
9	C	Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 3 30	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

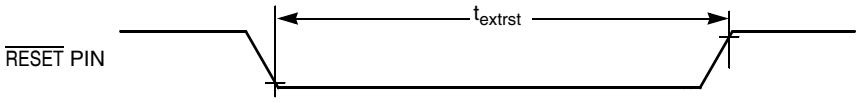


Figure 14. Reset Timing

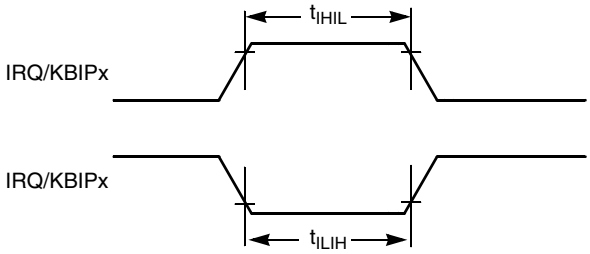


Figure 15. IRQ/KBIPx Timing

3.9.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 10. TPM Input Timing

Num	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

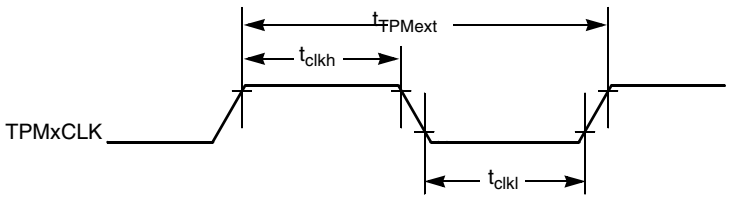


Figure 16. Timer External Clock

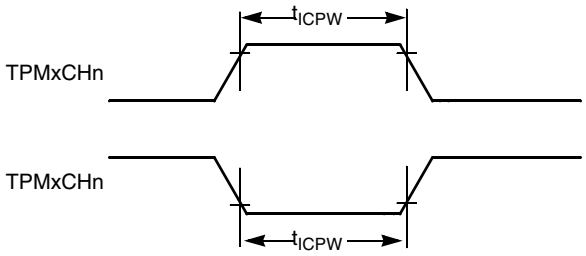


Figure 17. Timer Input Capture Pulse

3.10 SPI Characteristics

Table 11 and Figure 18 through Figure 21 describe the timing requirements for the SPI system.

Table 11. SPI Electrical Characteristic

Num[1]	C	Characteristic[2]	Symbol	Min	Typical	Max	Unit
1	D	Operating frequency[3] Master Slave	f_{op} f_{op}	$f_{Bus}/2048$DC	— —	$f_{Bus}/2$ $f_{Bus}/4$	Hz
2	D	Cycle time Master Slave	t_{SCK} t_{SCK}	2 4	— —	2048 —	t_{cyc}
3	D	Enable lead time Master Slave	t_{Lead} t_{Lead}	— —	1/2 1/2	— —	t_{SCK}
4	D	Enable lag time Master Slave	t_{Lag} t_{Lag}	— —	1/2 1/2	— —	t_{SCK}
5	D	Clock (SPSCK) high time Master Slave	t_{SCKH}	— 1/2 t_{SCK} – 25	1/2 t_{SCK} 1/2 t_{SCK}	— —	ns
6	D	Clock (SPSCK) low time Master Slave	t_{SCKL}	— 1/2 t_{SCK} – 25	1/2 t_{SCK} 1/2 t_{SCK}	— —	ns
7	D	Data setup time (inputs) Master Slave	$t_{SI(M)}$ $t_{SI(S)}$	30 30	— —	— —	ns
8	D	Data hold time (inputs) Master Slave	$t_{HI(M)}$ $t_{HI(S)}$	30 30	— —	— —	ns
9	D	Access time, slave[4]	t_A	—	—	40	ns
10	D	Disable time, slave[5]	t_{dis}	—	—	40	ns
11	D	Data setup time (outputs) Master Slave	t_{SO} t_{SO}	— —	— —	25 25	ns
12	D	Data hold time (outputs) Master Slave	t_{HO} t_{HO}	–10 –10	— —	— —	ns

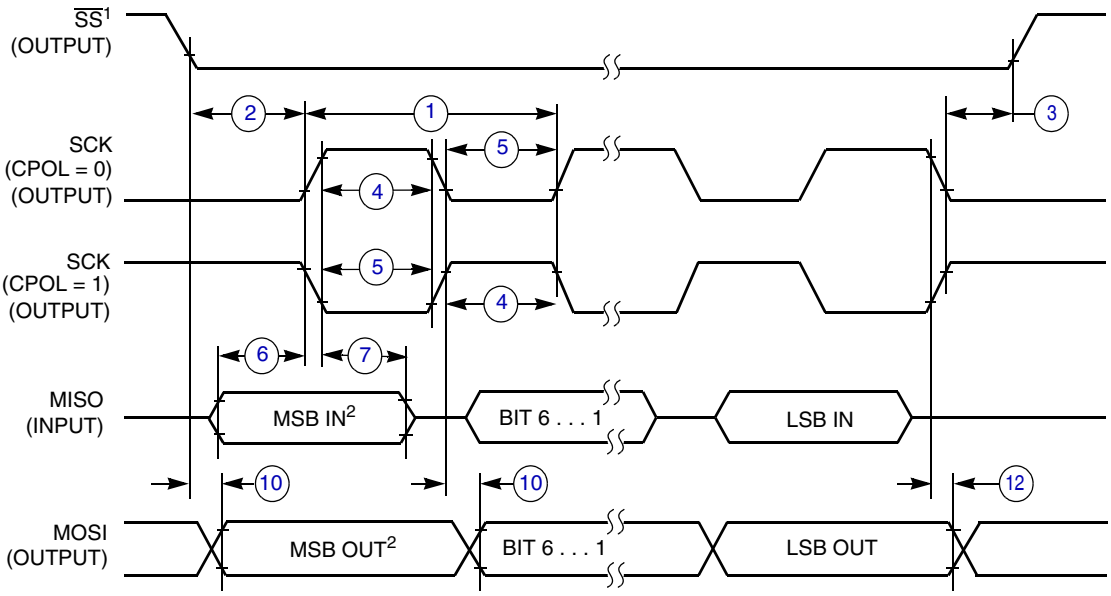
1 Refer to Figure 18 through Figure 21.

2 All timing is shown with respect to 20% V_{DD} and 80% V_{DD}, unless noted; 50 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 The maximum frequency is 8 MHz when input filter on SPI pins is disabled.

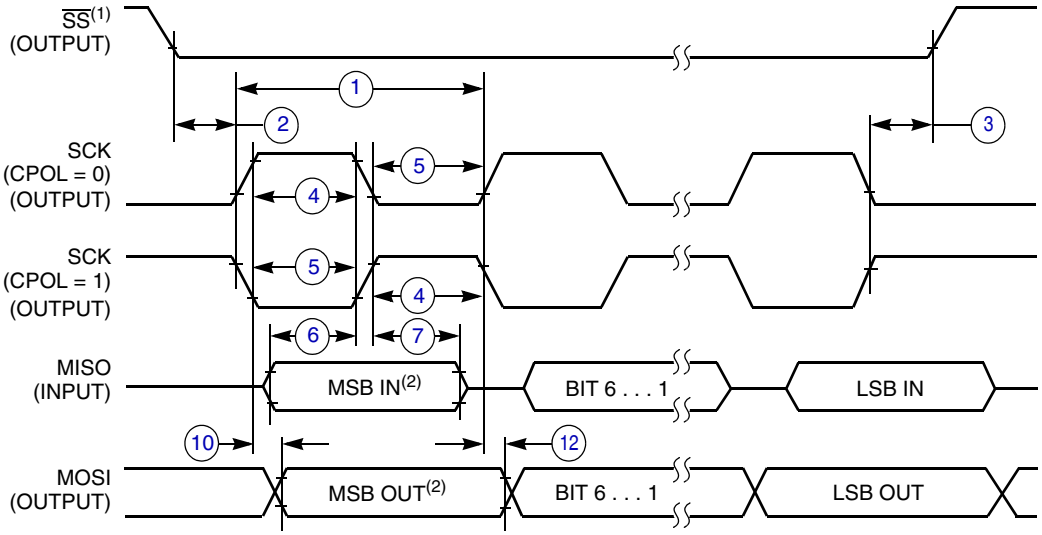
4 Time to data active from high-impedance state.

5 Hold time to high-impedance state.



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. SPI Master Timing (CPHA = 1)

Table 12. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	D	Supply voltage for program/erase	$V_{prog/erase}$	2.7	—	5.5	V
2	D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	D	Internal FCLK frequency[2]	f_{FCLK}	150	—	200	kHz
4	D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
5	P	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	P	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to 85 °C T = 25 °C	—	10,000 —	— 100,000	— —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 Typical endurance for flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

3.12 USB Electricals

The USB electricals for the S08USBV1 module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale S08USBV1 implementation requires additional or deviant electrical characteristics, this space would be used to communicate that information.

Table 13. Internal USB 3.3 V Voltage Regulator Characteristics

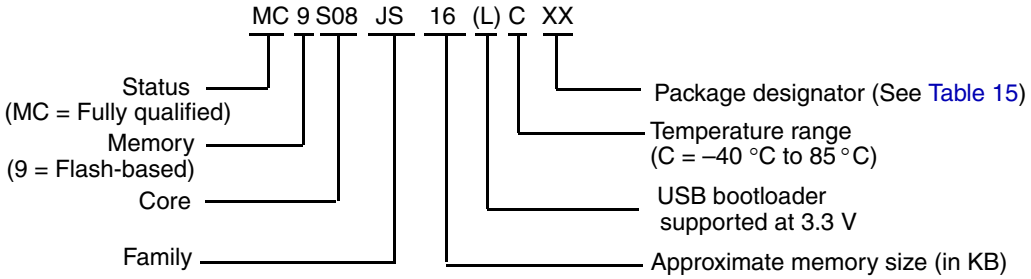
	Symbol	Min	Typical	Max	Unit
Regulator operating voltage	V_{regin}	3.9	—	5.5	V
V_{reg} output	V_{regout}	3	3.3	3.6	V
V_{reg} filter capacitor	C_{usbreg}	—	100	—	pF
V_{usb33} input with internal V_{reg} disabled	$V_{usb33in}$	3	3.3	3.6	V

Table 14. External 3.3 V Voltage Regulator Supply for V_{usb33} Pin

	Symbol	Min	Typical	Max	Unit
External 3.3 V regulator output current	—	39	—	—	mA

4 Ordering Information

This section contains ordering information for Device Numbering System. See below for an example of the device numbering system.



4.1 Package Information

Table 15. Package Descriptions

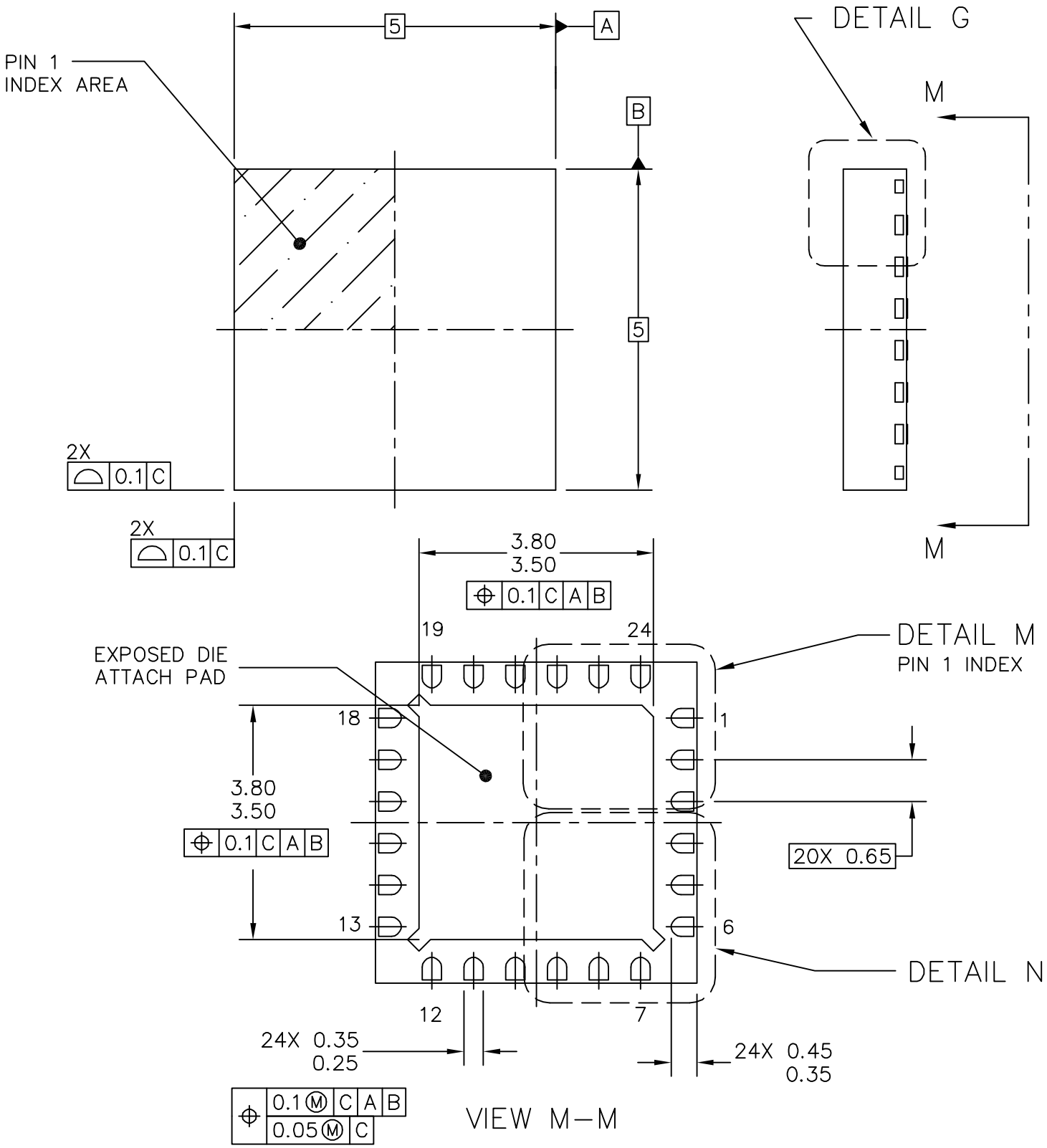
Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
24	Quad Flat No-Leads	QFN	FK	1982-01	98ARL10608D
20	Wide Body Small Outline Integrated Circuit	W-SOIC	WJ	751D	98ASB42343B

4.2 Mechanical Drawings

This following pages contain mechanical specifications for MC9S08JS16 series package options.

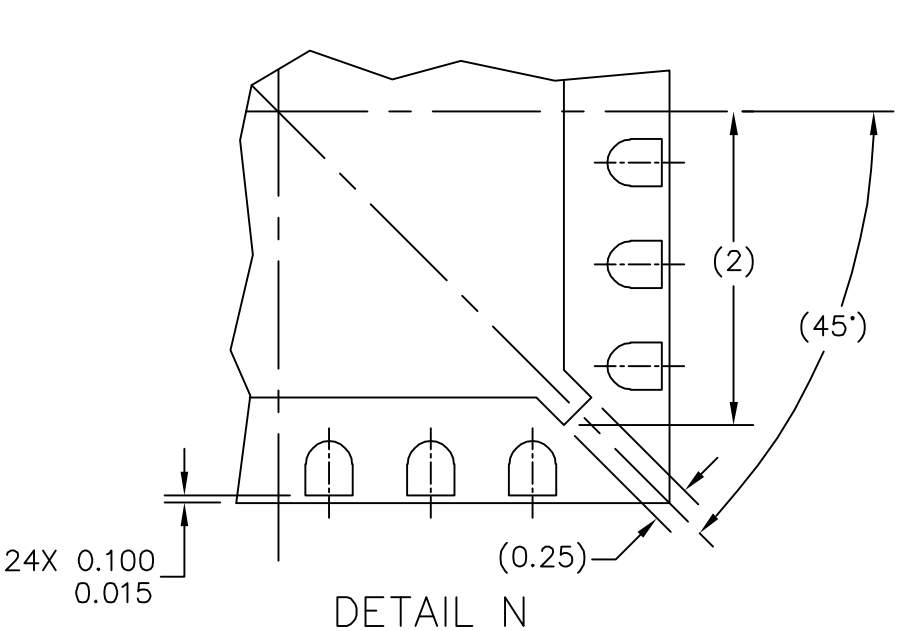
- 24-pin QFN (quad flat no-lead)
- 20-pin W-SOIC (wide body small outline integrated circuit)

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARL10608D
	PAGE: 1982
DO NOT SCALE THIS DRAWING	REV: O

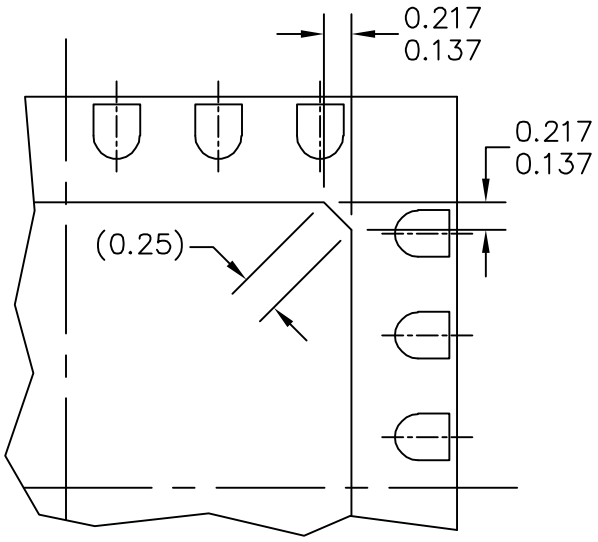


TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)	CASE NUMBER: 1982–01	
	STANDARD: JEDEC–MO–220 VHHC–1	
	PACKAGE CODE: 6238	SHEET: 1 OF 4

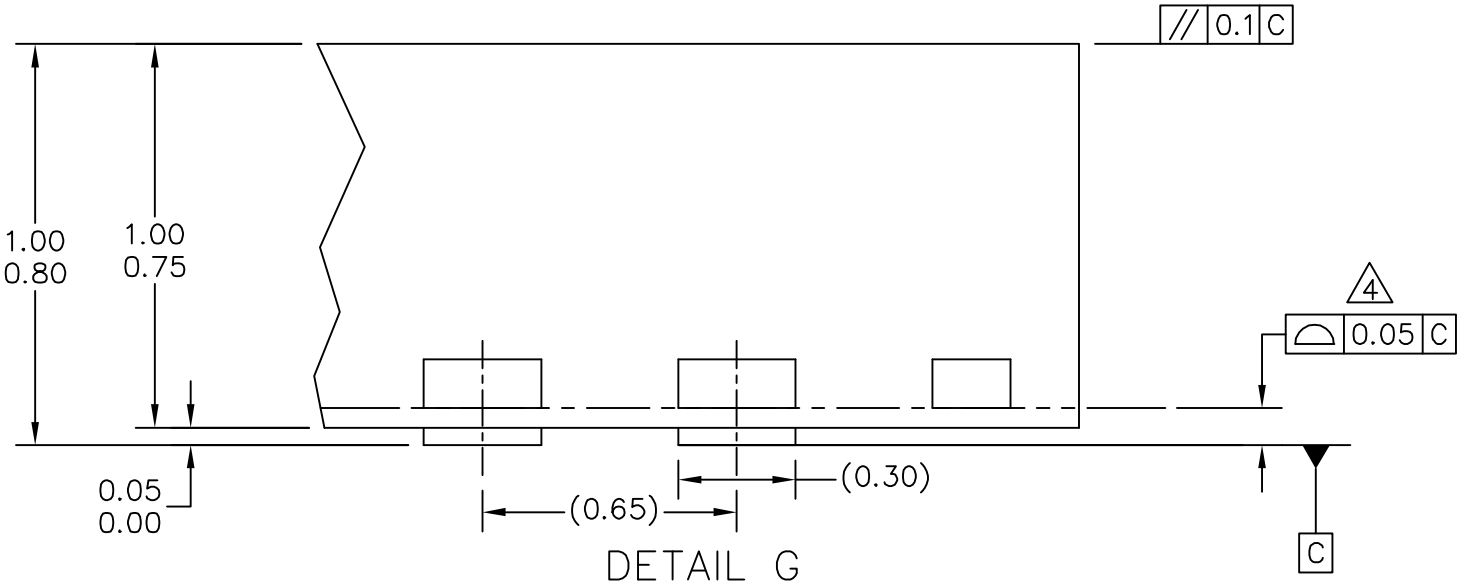
MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARL10608D
	PAGE: 1982
DO NOT SCALE THIS DRAWING	REV: O



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



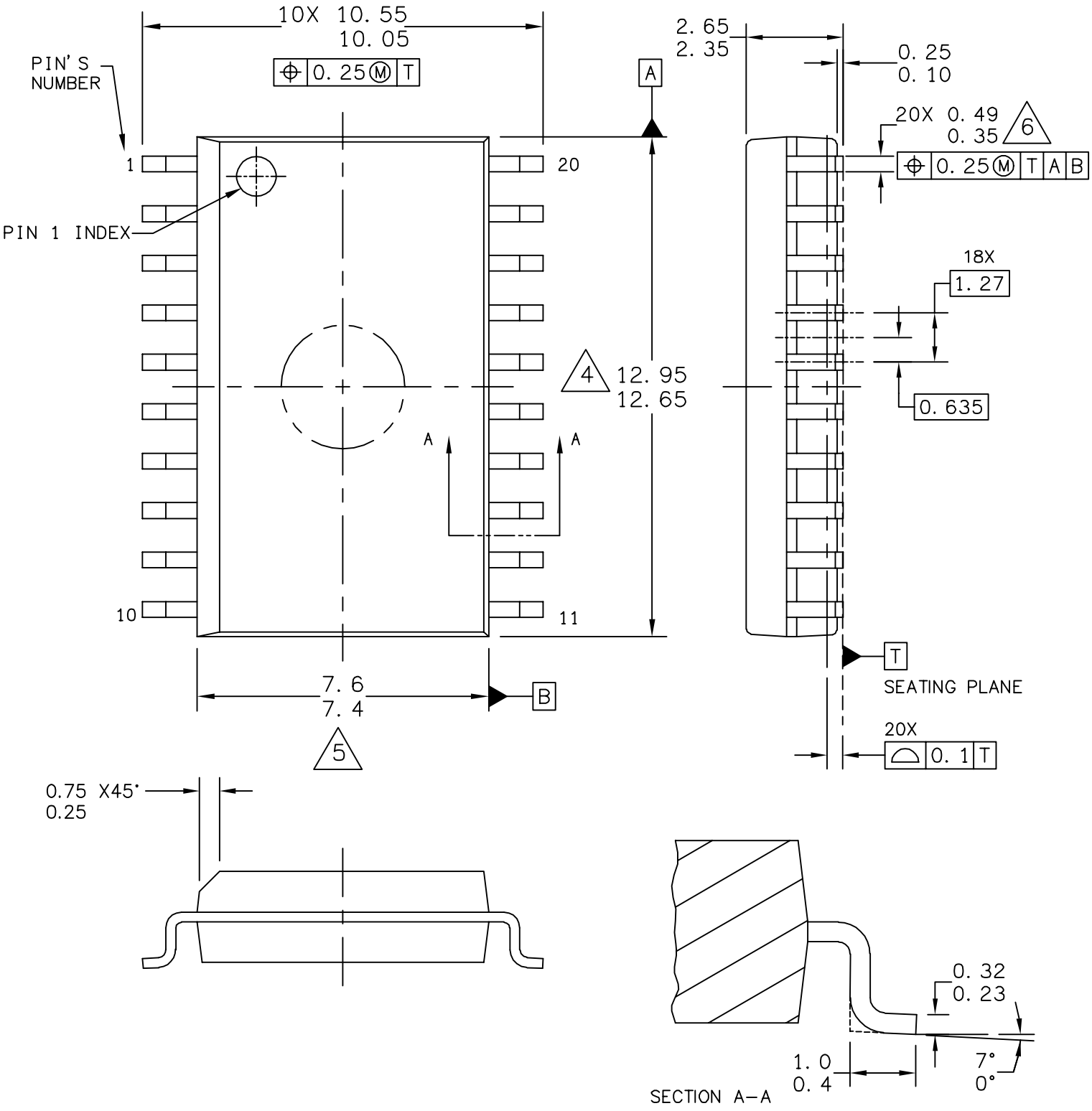
DETAIL G
VIEW ROTATED 90° CW

SEATING PLANE

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)	CASE NUMBER: 1982-01	
	STANDARD: JEDEC-MO-220 VHHC-1	
	PACKAGE CODE: 6238	SHEET: 2 OF 4

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42343B	REV: J
20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

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