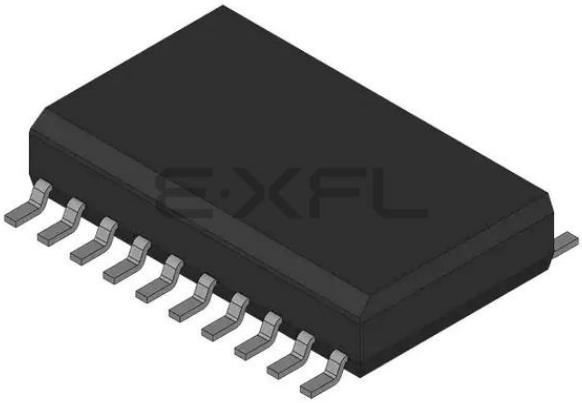


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	48MHz
Connectivity	LINbus, SCI, SPI, USB
Peripherals	LVD, POR, PWM
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08js16lcwj

Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08JS16
Rev. 4, 4/2009

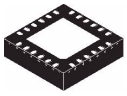
RoHS

MC9S08JS16

MC9S08JS16 Series

Covers:
MC9S08JS16
MC9S08JS8
MC9S08JS16L
MC9S08JS8L

20 W-SOIC
Case 751D



24 QFN
Case 1982-01

Features:

- 8-Bit HCS08 Central Processor Unit (CPU)
  - 48 MHz HCS08 CPU (central processor unit)
  - 24 MHz internal bus frequency
  - Support for up to 32 interrupt/reset sources
- Memory Options
  - Up to 16 KB of on-chip in-circuit programmable flash memory with block protection and security options
  - Up to 512 bytes of on-chip RAM
  - 256 bytes of USB RAM
- Clock Source Options
  - Clock source options include crystal, resonator, external clock
  - MCG (multi-purpose clock generator) — PLL and FLL; internal reference clock with trim adjustment
- System Protection
  - Optional computer operating properly (COP) reset with option to run from independent 1 kHz internal clock source or the bus clock
  - Low-voltage detection
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Power-Saving Modes
  - Wait plus two stops
- USB Bootload
  - Mass erase entire flash array
  - Partial erase flash array — erase all flash blocks except for the first 1 KB of flash
  - Program flash
- Peripherals
  - **USB** — USB 2.0 full-speed (12 Mbps) with dedicated on-chip 3.3 V regulator and transceiver; supports endpoint 0 and up to 6 additional endpoints
  - **SPI** — One 8- or 16-bit selectable serial peripheral interface module with a receive data buffer hardware match function
  - **SCI** — One serial communications interface module with optional 13 bit break. Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
  - **MTIM** — One 8-bit modulo counter with 8-bit prescaler and overflow interrupt
  - **TPM** — One 2-channel 16-bit timer/pulse-width modulator (TPM) module; selectable input capture, output compare, and edge-aligned PWM capability on each channel; timer module may be configured for buffered, centered PWM (CPWM) on all channels
  - **KBI** — 8-pin keyboard interrupt module
  - **RTC** — Real-time counter with binary- or decimal-based prescaler
  - **CRC** — Hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16}+x^{12}+x^5+1$ polynomial
- Input/Output
  - Software selectable pullups on ports when used as inputs
  - Software selectable slew rate control on ports when used as outputs
  - Software selectable drive strength on ports when used as outputs
  - Master reset pin and power-on reset (POR)
  - Internal pullup on $\overline{\text{RESET}}$, IRQ, and BKGD/MS pins to reduce customer system cost
- Package Options
  - 24-pin quad flat no-lead (QFN)
  - 20-pin small outline IC package (SOIC)

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

freescale semiconductor

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	9/1/2008	Initial public released
2	1/8/2009	In Table 7, changed the parameter description of RI_{DD} and $S3I_{DD,}$ the typicals of RI_{DD} were changed as well.
3	3/9/2009	Corrected the 24-pin QFN case number and doc. number information.
4	4/24/2009	Added new parts information about MC9S08JS16L and MC9S08JS8L.

Related Documentation

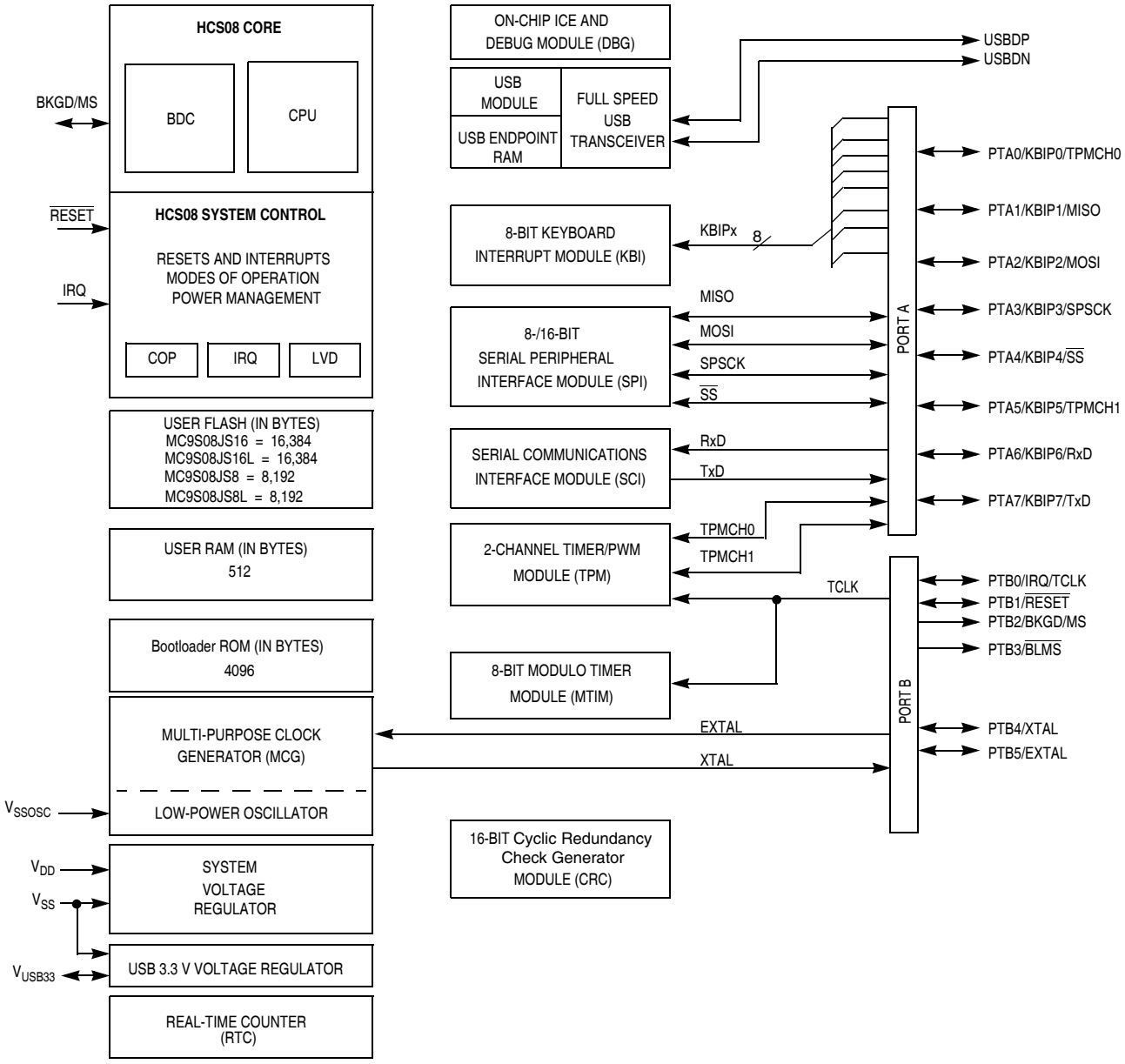
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08JS16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08JS16 series MCU.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ is enabled (IRQPE = 1). Pulldown is enabled if rising edge detect is selected (IRQEDG = 1).
3. IRQ does not have a clamp diode to V_{DD}. IRQ must not be driven above V_{DD}.
4. RESET contains integrated pullup device if PTB1 enabled as reset pin function (RSTPE = 1).
5. Pin contains integrated pullup device.
6. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

Figure 1. MC9S08JS16 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9S08JS16 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number (Package)		<-- Lowest **Priority** --> Highest		
24 (QFN)	**20 (SOIC)**	**Port Pin**	**Alt 1**	**Alt 2**
1	4	PTB0	IRQ	TCLK
2	5	PTB1		$\overline{\text{RESET}}$
3	6	PTB2	BKGD	MS
4	7	PTB3		$\overline{\text{BLMS}}$
5	8	PTA0	KBIP0	TPMCH0
6	—	NC		
7	9	PTA1	KBIP1	MISO
8	10	PTA2	KBIP2	MOSI
9	11	PTA3	KBIP3	SPSCK
10	12	PTA4	KBIP4	$\overline{\text{SS}}$
11	13			V_{DD}
12	—	NC		
13	14			V_{SS}
14	15			USBDN
15	16			USBDP
16	17			V_{USB33}
17	18	PTA5	KBIP5	TPMCH1
18	—	NC		
19	19	PTA6	KBIP6	RxD
20	20	PTA7	KBIP7	TxD
21	1	PTB4	XTAL	
22	2	PTB5	EXTAL	
23	3			V_{SSOSC}
24	—	NC		

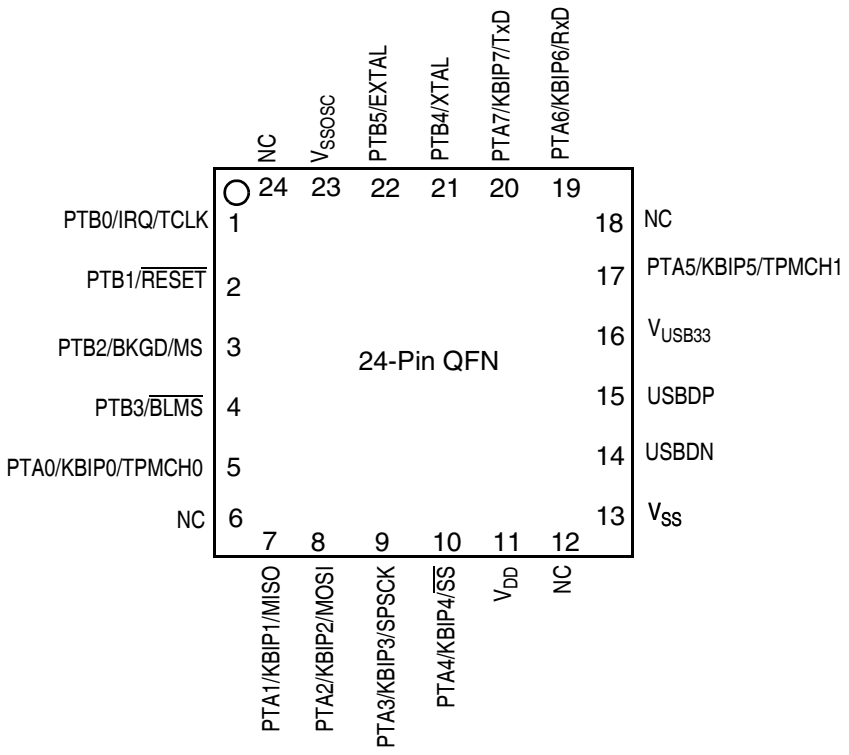


Figure 2. MC9S08JS16 Series in 24-QFN Package

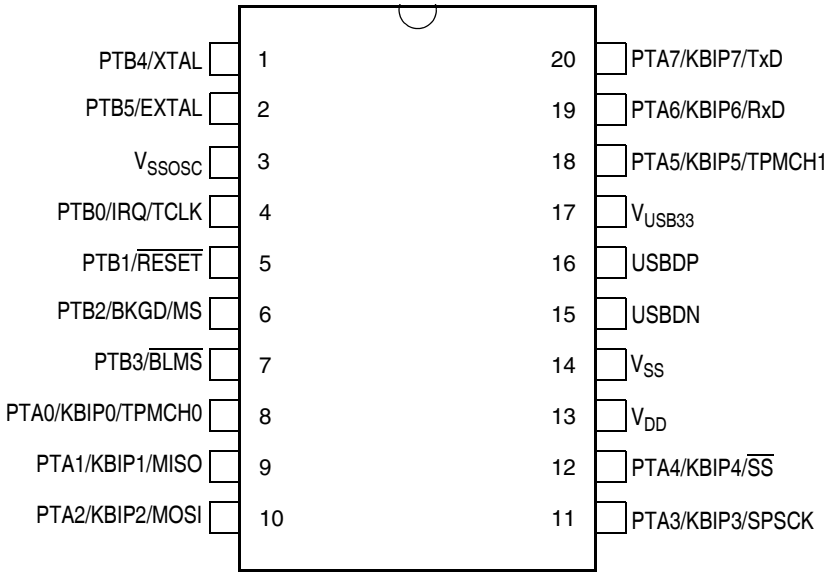


Figure 3. MC9S08JS16 Series in 20-pin SOIC Package

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 85	°C
Thermal resistance [1,2,3,4]			
24-pin QFN			
1s	θ_{JA}	92	°C/W
2s2p		33	
20-pin SOIC			
1s		86	
2s2p		58	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O} P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage. This device was qualified to AEC-Q100 Rev E. A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD Protection Characteristics

Parameter	Symbol	Value	Unit
ESD Target for Machine Model (MM) — MM circuit description	V_{THMM}	200	V
ESD Target for Human Body Model (HBM) — HBM circuit description	V_{THHBM}	2000	V

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 6. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1		Operating voltage[2]	—	2.7	—	5.5	V

Table 6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA 5 V, I_{Load} = –0.4 mA 3 V, I_{Load} = –0.24 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA 5 V, I_{Load} = 0.4 mA 3 V, I_{Load} = 0.24 mA	V_{OL}	 1.5 1.5 0.8 0.8	 — — — —	 — — — —	V
		Output low voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.4 mA		 1.5 1.5 0.8 0.8	 — — — —	 — — — —	
4	P	Output high current — Max total I_{OH} for all ports 5 V 3 V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs	V_{IH}	0.65 × V_{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 × V_{DD}	
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 × V_{DD}	—	—	mV
9	P	Input leakage current; input only pins[3]	$\|I_{In}\|$	—	0.1	1	µA
10	P	High Impedance (off-state) leakage current[3]	$\|I_{OZ}\|$	—	0.1	1	µA
11	P	Internal pullup resistors[4]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[5]	R_{PD}	20	45	65	kΩ
13	C	Internal pullup resistor to USBDP (to V_{USB33}) Idle Transmit	R_{PUPD}	 900 1425	 — —	 1575 3090	kΩ
14	C	Input capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	C	RAM retention voltage	V_{RAM}	0.6	1.0	—	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	µs

Table 6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	 — —	 100 60	 — —	mV

1 Typical values are based on characterization data at 25 °C unless otherwise stated.

2 Operating voltage with USB enabled can be found in Section 3.11, “USB Electricals.”

3 Measured with $V_{In} = V_{DD}$ or V_{SS}.

4 Measured with $V_{In} = V_{SS}$.

5 Measured with $V_{In} = V_{DD}$.

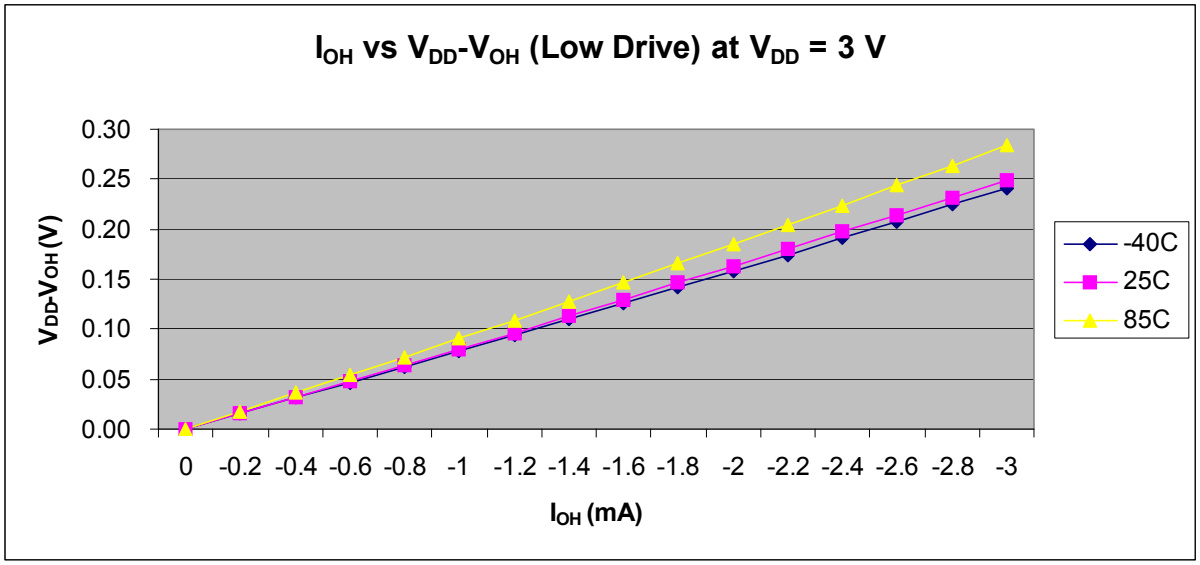


Figure 4. Typical I_{OH} (Low Drive) vs V_{DD}–V_{OH} at V_{DD} = 3 V

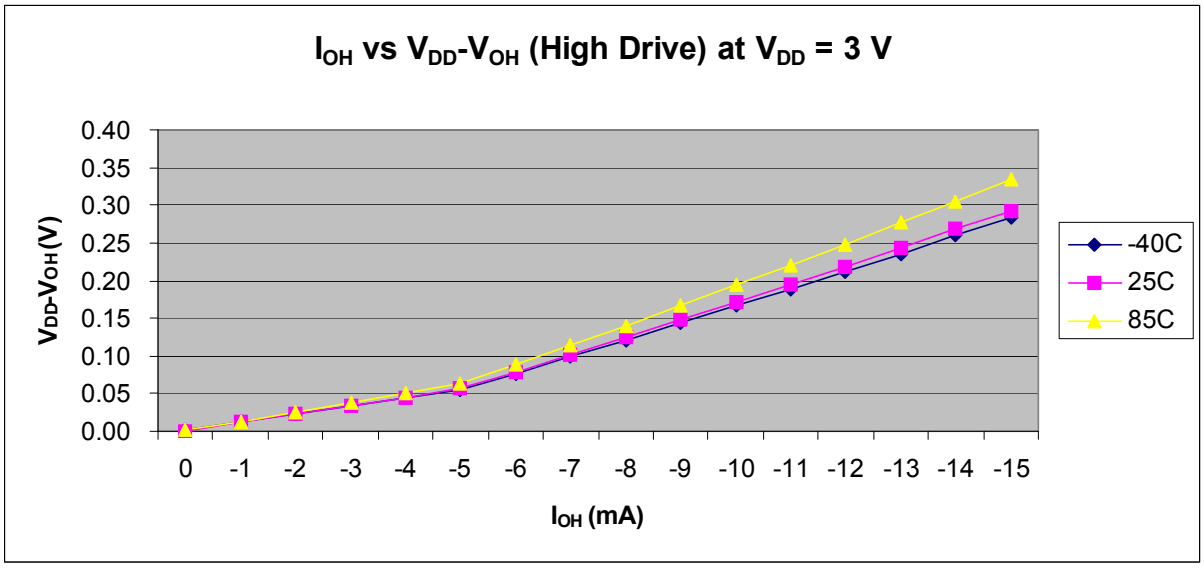


Figure 5. Typical I_{OH} (High Drive) vs V_{DD}–V_{OH} at V_{DD} = 3 V

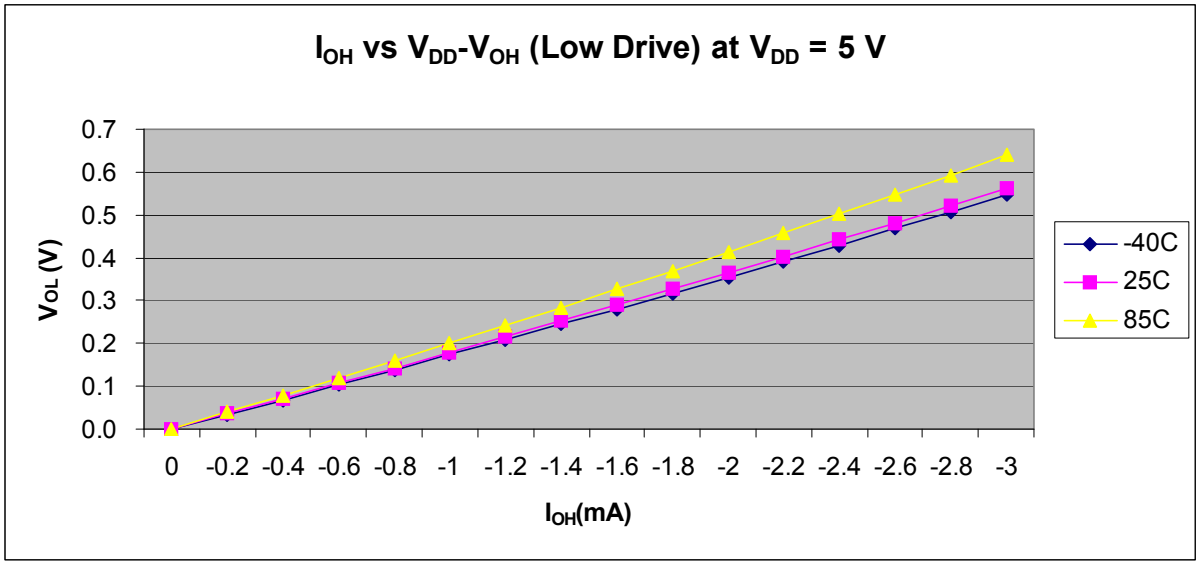


Figure 6. Typical I_{OH} (Low Drive) vs V_{DD}–V_{OH} at V_{DD} = 5 V

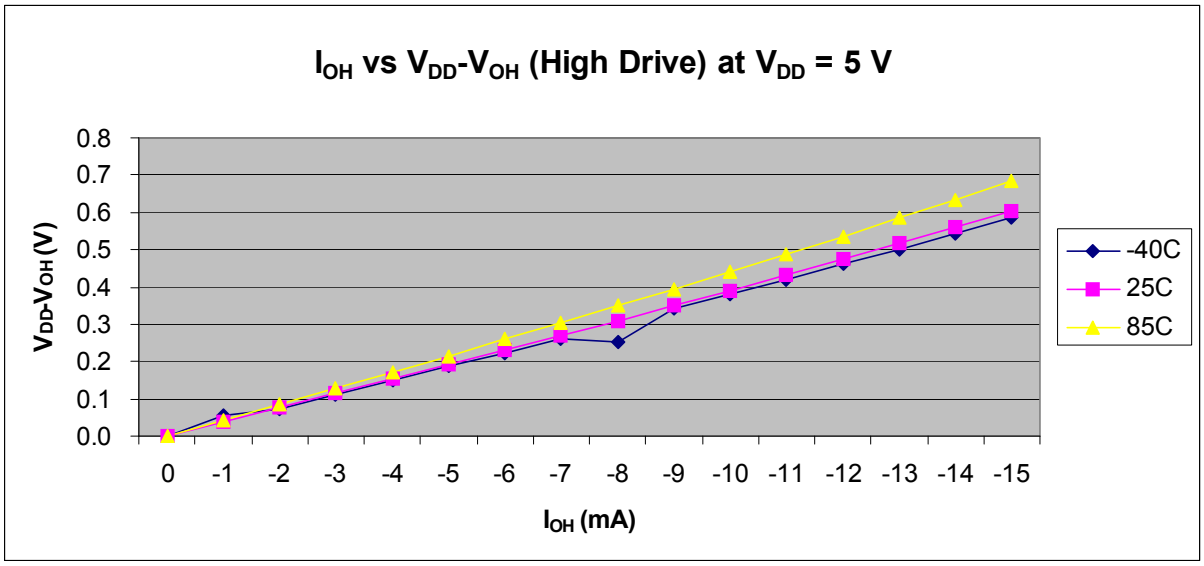


Figure 7. Typical I_{OH} (High Drive) vs V_{DD}–V_{OH} at V_{DD} = 5 V

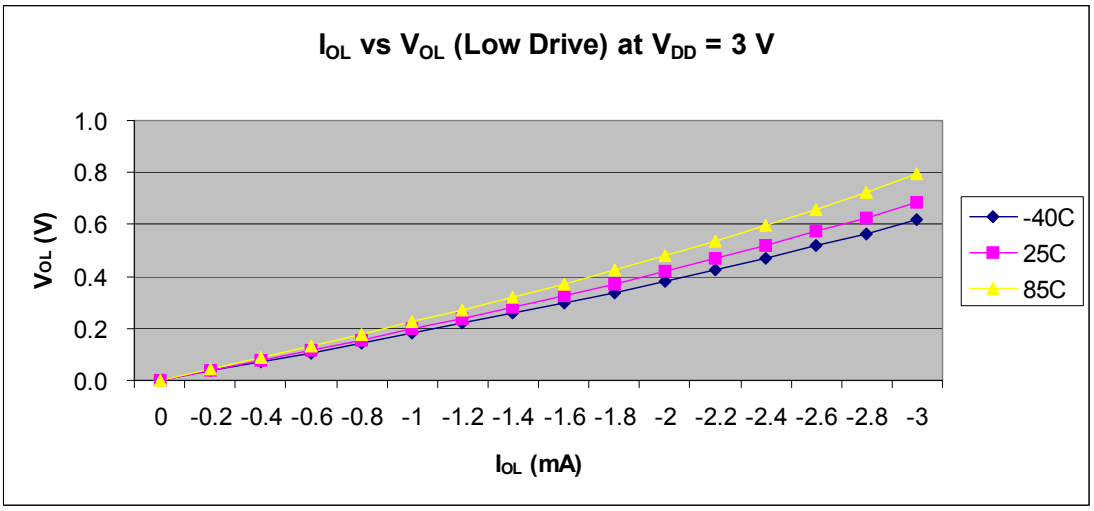


Figure 10. I_{OL} vs V_{OL} (Low Drive) at V_{DD} = 3 V

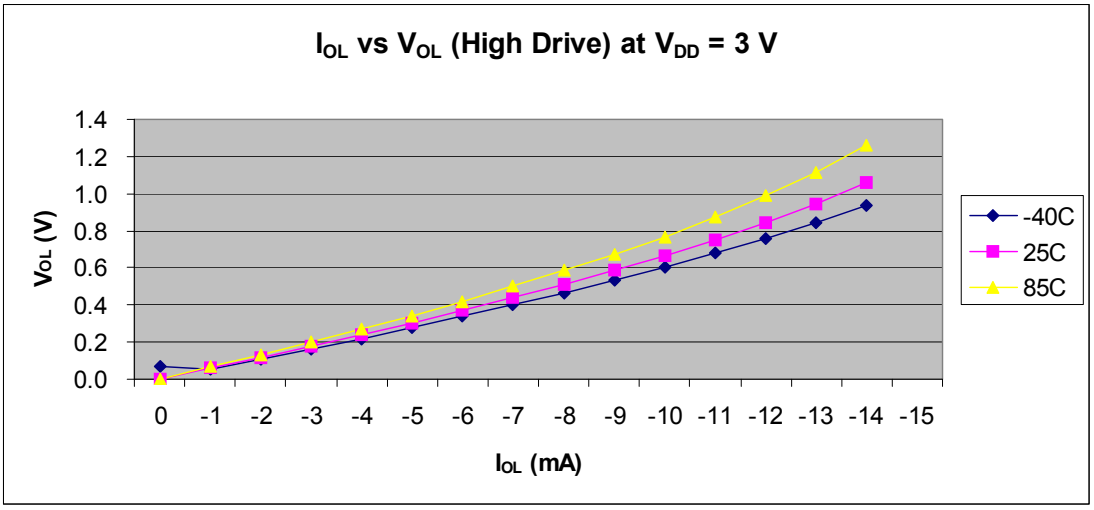


Figure 11. I_{OL} vs V_{OL} (High Drive) at V_{DD} = 3 V

3.8 MCG Specifications

Table 9. MCG Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	—	39.0625	kHz
3	T	Internal reference startup time	t_{irefst}	—	60	100	µs
4	C	DCO output frequency range — untrimmed	f_{dco_ut}	25.6	33.48	42.66	MHz
5	P	DCO output frequency range — trimmed	f_{dco_t}	32	—	40	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[1]	$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time[2]	$t_{pll\_acquire}$	—	—	1	ms
12	C	Long term Jitter of DCO output clock (averaged over 2ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
14	D	PLL reference frequency range	f_{pll_ref}	1.0	—	2.0	MHz
15	T	Long term accuracy of PLL output clock (averaged over 2 ms)	$f_{pll\_jitter\_2ms}$	—	0.590[4]	—	%
16	T	Jitter of PLL output clock measured over 625 ns[5]	$f_{pll\_jitter\_625ns}$	—	0.566[4]	—	%
17	D	Lock entry frequency tolerance[6]	D_{lock}	±1.49	—	±2.98	%
18	D	Lock exit frequency tolerance[7]	D_{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
20	D	Lock time — PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f_{loc_low}	(3/5) x f_{int}	—	—	kHz
22	D	Loss of external clock minimum frequency — RANGE = 1	f_{loc_high}	(16/5) x f_{int}	—	—	kHz

1 This specification applies any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

2 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

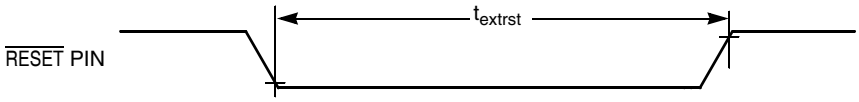


Figure 14. Reset Timing

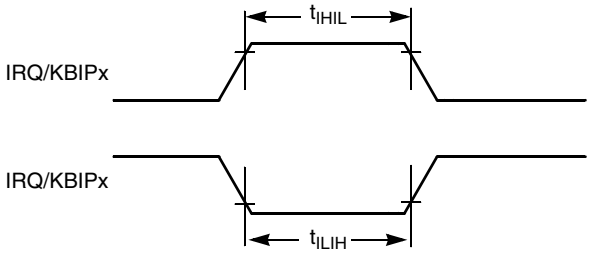


Figure 15. IRQ/KBIPx Timing

3.9.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 10. TPM Input Timing

Num	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

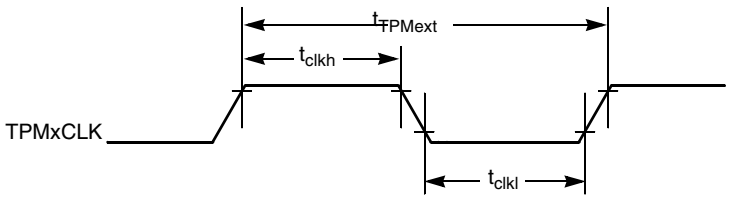
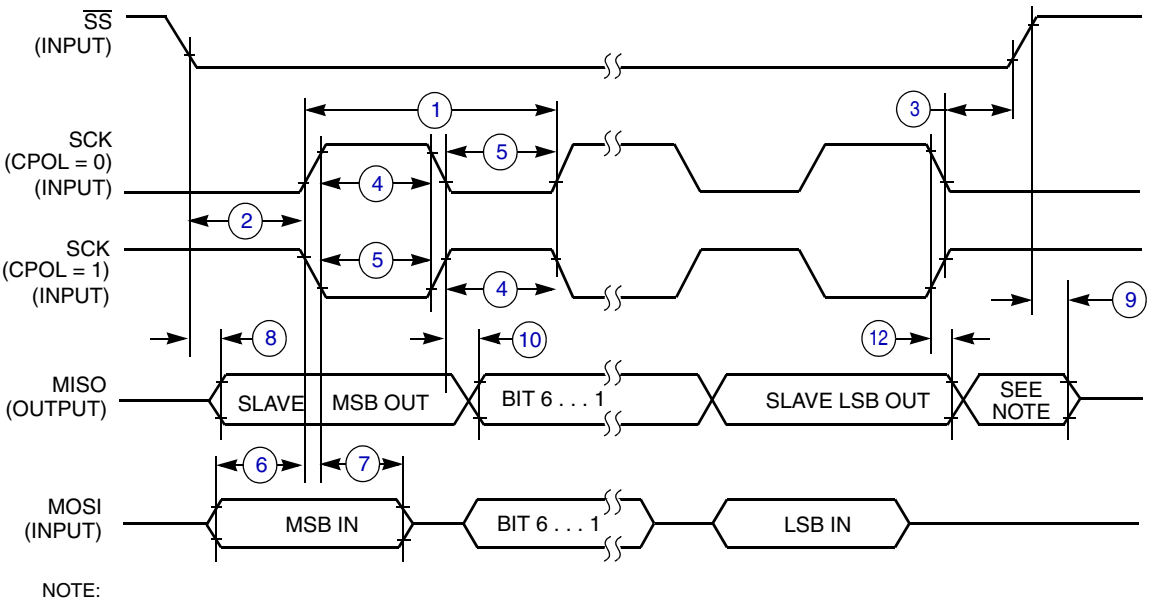
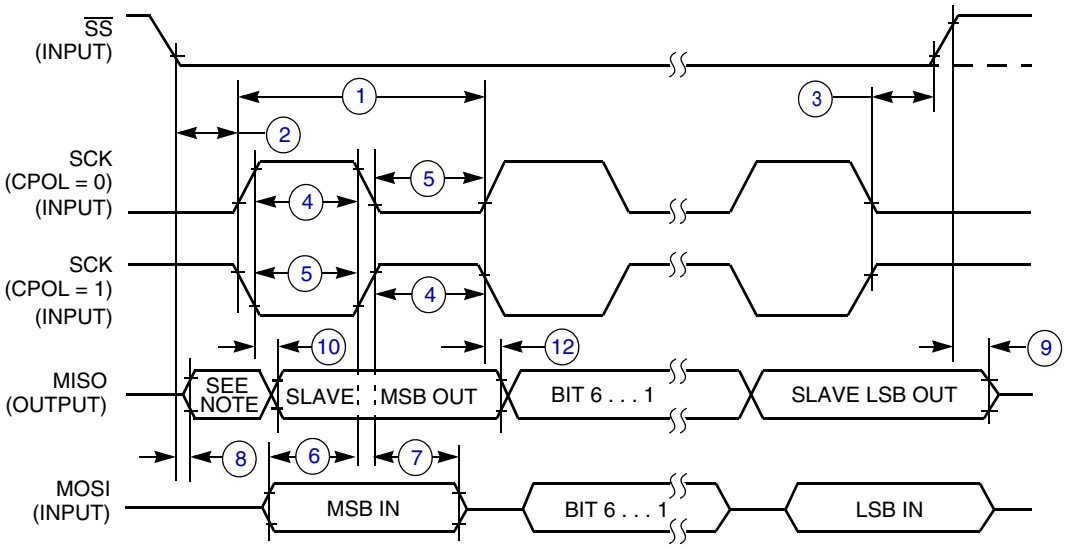


Figure 16. Timer External Clock



NOTE:
1. Not defined but normally MSB of character just received

Figure 20. SPI Slave Timing (CPHA = 0)



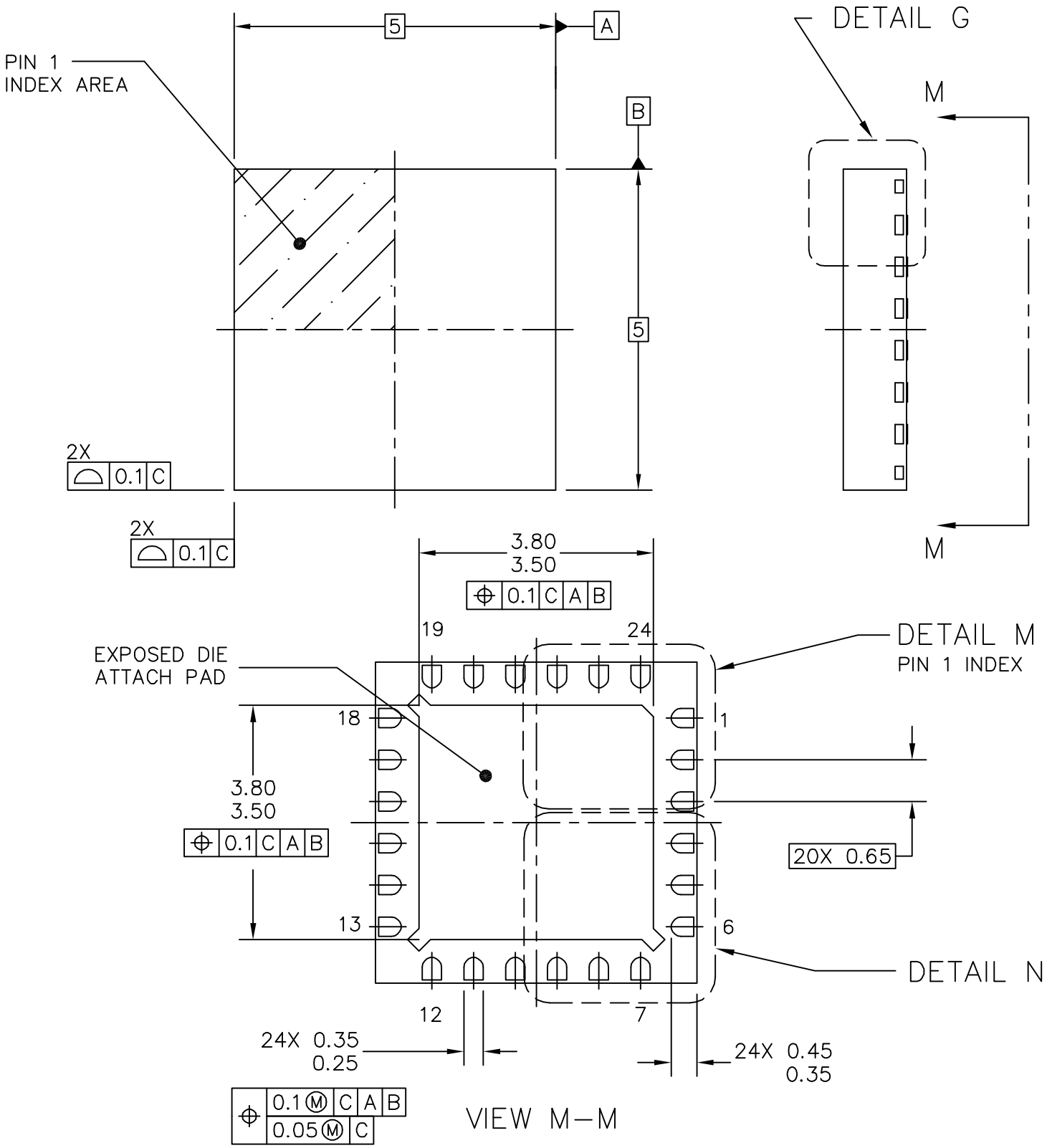
NOTE:
1. Not defined but normally LSB of character just received

Figure 21. SPI Slave Timing (CPHA = 1)

3.11 Flash Specifications

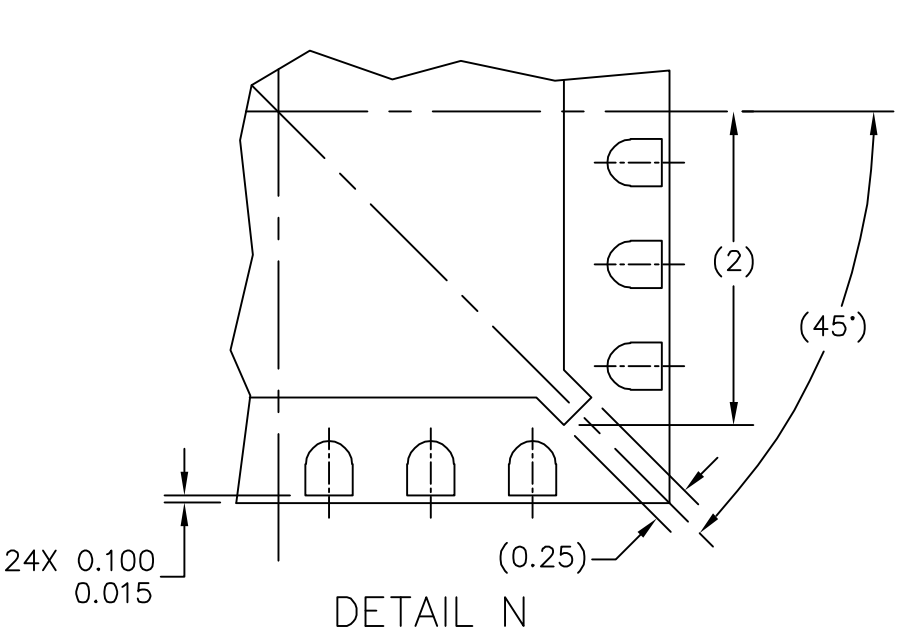
This section provides details about program/erase times and program-erase endurance for the flash memory. Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARL10608D
	PAGE: 1982
DO NOT SCALE THIS DRAWING	REV: O

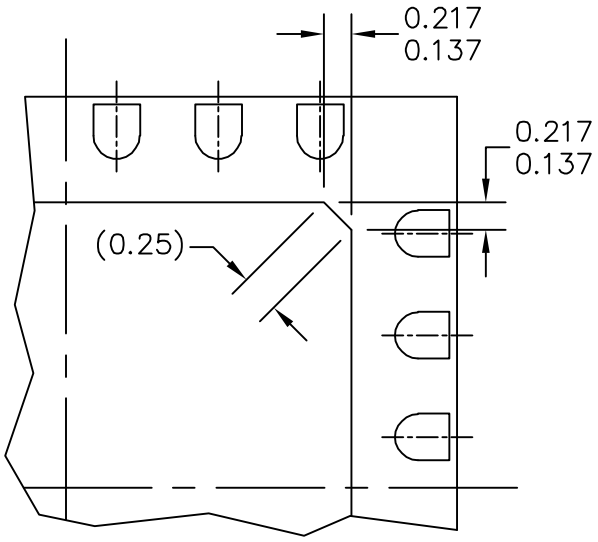


TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)	CASE NUMBER: 1982–01	
	STANDARD: JEDEC–MO–220 VHHC–1	
	PACKAGE CODE: 6238	SHEET: 1 OF 4

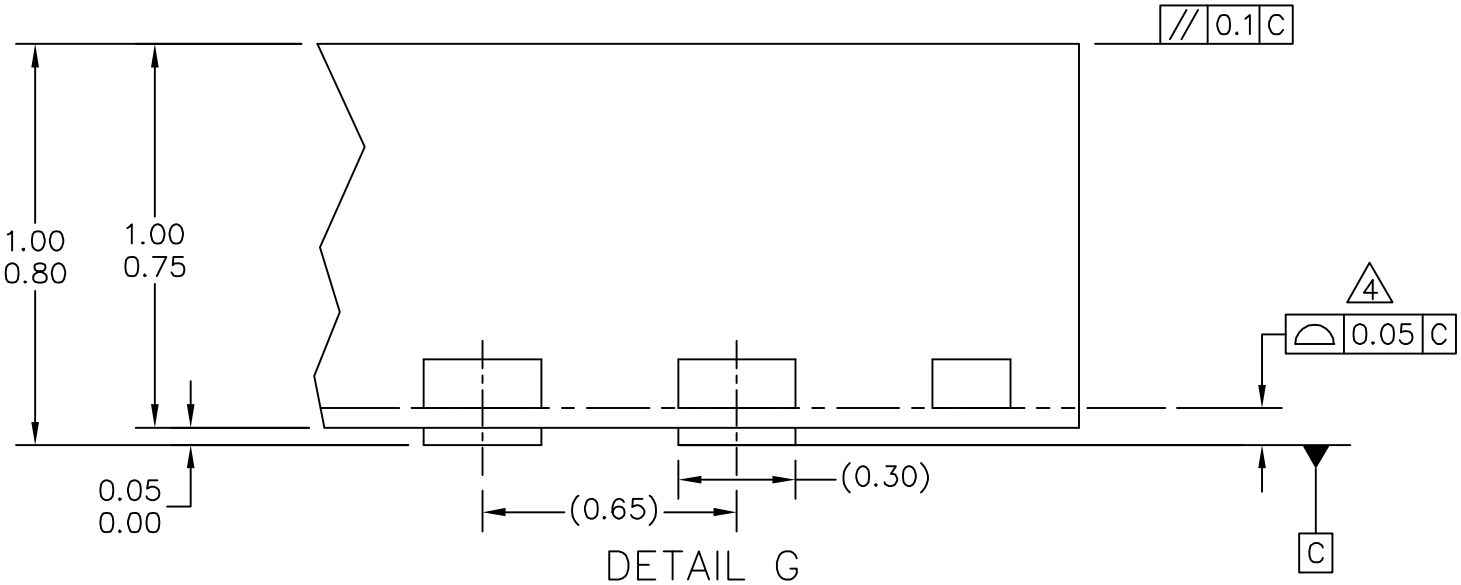
MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARL10608D
	PAGE: 1982
DO NOT SCALE THIS DRAWING	REV: O



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90° CW

SEATING PLANE

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)	CASE NUMBER: 1982-01	
	STANDARD: JEDEC-MO-220 VHHC-1	
	PACKAGE CODE: 6238	SHEET: 2 OF 4

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42343B	REV: J
20LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	CASE NUMBER: 751D–07	23 MAR 2005
	STANDARD: JEDEC MS–013AC	

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MC9S08JS16
Rev. 4
4/2009