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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq@UltraScale+™ FPGA, 103K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (Tj)
Package / Case	784-BFBGA, FCBGA
Supplier Device Package	784-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu2eg-1sfvc784i

ARM Mali-400 Based GPU

- Supports OpenGL ES 1.1 and 2.0
- Supports OpenVG 1.1
- GPU frequency: Up to 667MHz
- Single Geometry Processor, Two Pixel Processors
- Pixel Fill Rate: 2 Mpixels/sec/MHz
- Triangle Rate: 0.11 Mtriangles/sec/MHz
- 64KB L2 Cache
- Power island gating

External Memory Interfaces

- Multi-protocol dynamic memory controller
- 32-bit or 64-bit interfaces to DDR4, DDR3, DDR3L, or LPDDR3 memories, and 32-bit interface to LPDDR4 memory
- ECC support in 64-bit and 32-bit modes
- Up to 32GB of address space using single or dual rank of 8-, 16-, or 32-bit-wide memories
- Static memory interfaces
 - eMMC4.51 Managed NAND flash support
 - ONFI3.1 NAND flash with 24-bit ECC
 - 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash

8-Channel DMA Controller

- Two DMA controllers of 8-channels each
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

Serial Transceivers

- Four dedicated PS-GTR receivers and transmitters supports up to 6.0Gb/s data rates
 - Supports SGMII tri-speed Ethernet, PCI Express® Gen2, Serial-ATA (SATA), USB3.0, and DisplayPort

Dedicated I/O Peripherals and Interfaces

- PCI Express — Compliant with PCIe® 2.1 base specification
 - Root complex and End Point configurations
 - x1, x2, and x4 at Gen1 or Gen2 rates
- SATA Host
 - 1.5, 3.0, and 6.0Gb/s data rates as defined by SATA Specification, revision 3.1
 - Supports up to two channels
- DisplayPort Controller
 - Up to 5.4Gb/s rate
 - Up to two TX lanes (no RX support)

- Four 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
 - Scatter-gather DMA capability
 - Recognition of IEEE Std 1588 rev.2 PTP frames
 - GMII, RGMII, and SGMII interfaces
 - Jumbo frames
- Two USB 3.0/2.0 Device, Host, or OTG peripherals, each supporting up to 12 endpoints
 - USB 3.0/2.0 compliant device IP core
 - Super-speed, high-speed, full-speed, and low-speed modes
 - Intel XHCI-compliant USB host
- Two full CAN 2.0B-compliant CAN bus interfaces
 - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
- Two SD/SDIO 2.0/eMMC4.51 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1Mb/s)
- Two master and slave I2C interfaces
- Up to 78 flexible multiplexed I/O (MIO) (up to three banks of 26 I/Os) for peripheral pin assignment
- Up to 96 EMIOs (up to three banks of 32 I/Os) connected to the PL

Interconnect

- High-bandwidth connectivity within PS and between PS and PL
- ARM AMBA® AXI4-based
- QoS support for latency and bandwidth control
- Cache Coherent Interconnect (CCI)

System Memory Management

- System Memory Management Unit (SMMU)
- Xilinx Memory Protection Unit (XMPU)

Platform Management Unit

- Power gates PS peripherals, power islands, and power domains
- Clock gates PS peripheral user firmware option

Configuration and Security Unit

- Boots PS and configures PL
- Supports secure and non-secure boot modes

System Monitor in PS

- On-chip voltage and temperature sensing

Feature Summary

Table 1: Zynq UltraScale+ MPSoC: CG Device Feature Summary

	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Application Processing Unit	Dual-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache						
Real-Time Processing Unit	Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM						
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC						
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters						
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII						
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8
Block RAM Blocks	150	216	128	144	714	312	912
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1
UltraRAM Blocks	0	0	48	64	0	96	0
UltraRAM (Mb)	0	0	14.0	18.0	0	27.0	0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520
CMTs	3	3	4	4	4	8	4
Max. HP I/O ⁽¹⁾	156	156	156	156	208	416	208
Max. HD I/O ⁽²⁾	96	96	96	96	120	48	120
System Monitor	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s ⁽³⁾	0	0	16	16	24	24	24
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0
Transceiver Fractional PLLs	0	0	8	8	12	12	12
PCIe Gen3 x16 and Gen4 x8	0	0	2	2	0	2	0
150G Interlaken	0	0	0	0	0	0	0
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 2](#).

Table 3: Zynq UltraScale+ MPSoC: EG Device Feature Summary

	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache										
Real-Time Processing Unit	Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM										
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC										
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters										
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII										
Graphic Processing Unit	ARM Mali™-400 MP2; 64KB L2 Cache										
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550	653,100	746,550	926,194	1,143,450
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160	597,120	682,560	846,806	1,045,440
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080	298,560	341,280	423,403	522,720
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
Block RAM Blocks	150	216	128	144	714	312	912	600	744	796	984
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
UltraRAM Blocks	0	0	48	64	0	96	0	80	112	102	128
UltraRAM (Mb)	0	0	14.0	18.0	0	27.0	0	22.5	31.5	28.7	36.0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
CMTs	3	3	4	4	4	8	4	8	4	11	11
Max. HP I/O ⁽¹⁾	156	156	156	156	208	416	208	416	208	572	572
Max. HD I/O ⁽²⁾	96	96	96	96	120	48	120	96	120	96	96
System Monitor	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s ⁽³⁾	0	0	16	16	24	24	24	32	24	44	44
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0	16	0	28	28
Transceiver Fractional PLLs	0	0	8	8	12	12	12	24	12	36	36
PCIe Gen3 x16 and Gen4 x8	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	1	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	2	0	2	4

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 4](#).

ASIC-class capabilities afforded by the UltraScale MPSoC architecture while supporting rapid system development.

The inclusion of an application processor enables high-level operating system support, e.g., Linux. Other standard operating systems used with the Cortex-A53 processor are also available for the Zynq UltraScale+ MPSoC family. The PS and the PL are on separate power domains, enabling users to power down the PL for power management if required. The processors in the PS always boot first, allowing a software centric approach for PL configuration. PL configuration is managed by software running on the CPU, so it boots similar to an ASSP.

Real-Time Processing Unit (RPU)

- Dual-core ARM Cortex-R5 MPCores. Features associated with each core include:
 - ARM v7-R Architecture (32-bit)
 - Operating target frequency: Up to 600MHz
 - A32/T32 instruction set support
 - 4-way set-associative Level 1 caches (separate instruction and data, 32KB each) with ECC support
 - Integrated Memory Protection Unit (MPU) per processor
 - 128KB Tightly Coupled Memory (TCM) with ECC support
 - TCMs can be combined to become 256KB in lockstep mode
- Ability to operate in single-processor or dual-processor modes (split and lock-step)
- Little and big endian support
- Dedicated SWDT and two Triple Timer Counters (TTC)
- CoreSight debug and trace support
 - Embedded Trace Macrocell (ETM) for instruction and trace
 - Cross trigger interface (CTI) enabling hardware breakpoints and triggers
- Optional eFUSE disable

Full-Power Domain DMA (FPD-DMA) and Low-Power Domain DMA (LPD-DMA)

- Two general-purpose DMA controllers one in the full-power domain (FPD-DMA) and one in the low-power domain (LPD-DMA)
- Eight independent channels per DMA
- Multiple transfer types:
 - Memory-to-memory
 - Memory-to-peripheral
 - Peripheral-to-memory and
 - Scatter-gather
- 8 peripheral interfaces per DMA
- TrustZone per DMA for optional secure operation

- Low power modes
 - Active/precharge power down
 - Self-refresh, including clean exit from self-refresh after a controller power cycle
- Enhanced DDR training by allowing software to measure read/write eye and make delay adjustments dynamically
- Independent performance monitors for read path and write path
- Integration of PHY Debug Access Port (DAP) into JTAG for testing

The DDR memory controller is multi-ported and enables the PS and the PL to have shared access to a common memory. The DDR controller features six AXI slave ports for this purpose:

- Two 128-bit AXI ports from the ARM Cortex-A53 CPU(s), RPU (ARM Cortex-R5 and LPD peripherals), GPU, high speed peripherals (USB3, PCIe & SATA), and High Performance Ports (HP0 & HP1) from the PL through the Cache Coherent Interconnect (CCI)
- One 64-bit port is dedicated for the ARM Cortex-R5 CPU(s)
- One 128-bit AXI port from the DisplayPort and HP2 port from the PL
- One 128-bit AXI port from HP3 and HP4 ports from the PL
- One 128-bit AXI port from General DMA and HP5 from the PL

High-Speed Connectivity Peripherals

PCIe

- Compliant with the PCI Express Base Specification 2.1
- Fully compliant with PCI Express transaction ordering rules
- Lane width: x1, x2, or x4 at Gen1 or Gen2 rates
- 1 Virtual Channel
- Full duplex PCIe port
- End Point and single PCIe link Root Port
- Root Port supports Enhanced Configuration Access Mechanism (ECAM), Cfg Transaction generation
- Root Port support for INTx, and MSI
- Endpoint support for MSI or MSI-X
 - 1 physical function, no SR-IOV
 - No relaxed or ID ordering
 - Fully configurable BARs
 - INTx not recommended, but can be generated
 - Endpoint to support configurable target/slave apertures with address translation and Interrupt capability

SATA

- Compliant with SATA 3.1 Specification
- SATA host port supports up to 2 external devices
- Compliant with Advanced Host Controller Interface ('AHCI') ver. 1.3
- 1.5Gb/s, 3.0Gb/s, and 6.0Gb/s data rates
- Power management features: supports partial and slumber modes

USB 3.0

- Two USB controllers (configurable as USB 2.0 or USB 3.0)
- Up to 5.0Gb/s data rate
- Host and Device modes
 - Super Speed, High Speed, Full Speed, and Low Speed
 - Up to 12 endpoints
 - The USB host controller registers and data structures are compliant to Intel xHCI specifications
 - 64-bit AXI master port with built-in DMA
 - Power management features: Hibernation mode

DisplayPort Controller

- 4K Display Processing with DisplayPort output
 - Maximum resolution of 4K x 2K-30 (30Hz pixel rate)
 - DisplayPort AUX channel, and Hot Plug Detect (HPD) on the output
 - RGB YCbCr, 4:2:0; 4:2:2, 4:4:4 with 6, 8, 10, and 12b/c
 - Y-only, xvYCC, RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2, and YCbCr 4:2:0 video format with 6,8,10 and 12-bits per color component
 - 256-color palette
 - Multiple frame buffer formats
 - 1, 2, 4, 8 bits per pixel (bpp) via a palette
 - 16, 24, 32bpp
 - Graphics formats such as RGBA8888, RGB555, etc.
- Accepts streaming video from the PL or dedicated DMA controller
- Enables Alpha blending of graphics and Chroma keying

Configuration Security Unit (CSU)

- Triple redundant Secure Processor Block (SPB) with built-in ECC
- Crypto Interface Block consisting of
 - 256-bit AES-GCM
 - SHA-3/384
 - 4096-bit RSA
- Key Management Unit
- Built-in DMA
- PCAP interface
- Supports ROM validation during pre-configuration stage
- Loads First Stage Boot Loader (FSBL) into OCM in either secure or non-secure boot modes
- Supports voltage, temperature, and frequency monitoring after configuration

Xilinx Peripheral Protection Unit (XPPU)

- Provides peripheral protection support
- Up to 20 masters simultaneously
- Multiple aperture sizes
- Access control for a specified set of address apertures on a per master basis
- 64KB peripheral apertures and controls access on per peripheral basis

I/O Peripherals

The IOP unit contains the data communication peripherals. Key features of the IOP include:

Triple-Speed Gigabit Ethernet

- Compatible with IEEE Std 802.3 and supports 10/100/1000Mb/s transfer rates (Full and Half duplex)
- Supports jumbo frames
- Built-in Scatter-Gather DMA capability
- Statistics counter registers for RMON/MIB
- Multiple I/O types (1.8, 2.5, 3.3V) on RGMII interface with external PHY
- GMII interface to PL to support interfaces as: TBI, SGMII, and RGMII v2.0 support
- Automatic pad and cyclic redundancy check (CRC) generation on transmitted frames
- Transmitter and Receive IP, TCP, and UDP checksum offload
- MDIO interface for physical layer management

- Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Supports IEEE Std 1588 v2

SD/SDIO 3.0 Controller

In addition to secure digital (SD) devices, this controller also supports eMMC 4.51.

- Host mode support only
- Built-in DMA
- 1/4-Bit SD Specification, version 3.0
- 1/4/8-Bit eMMC Specification, version 4.51
- Supports primary boot from SD Card and eMMC (Managed NAND)
- High speed, default speed, and low-speed support
- 1 and 4-bit data interface support
 - Low speed clock 0-400KHz
 - Default speed 0-25MHz
 - High speed clock 0-50MHz
- High speed Interface
 - SD UHS-1: 208MHz
 - eMMC HS200: 200MHz
- Memory, I/O, and SD cards
- Power control modes
- Data FIFO interface up to 512B

UART

- Programmable baud rate generator
- 6, 7, or 8 data bits
- 1, 1.5, or 2 stop bits
- Odd, even, space, mark, or no parity
- Parity, framing, and overrun error detection
- Line break generation and detection
- Automatic echo, local loopback, and remote loopback channel modes
- Modem control signals: CTS, RTS, DSR, DTR, RI, and DCD (from EMIO only)

- 2 chip selects
- Programmable access timing
- 1.8V and 3.3V I/O
- Built-in DMA for improved performance

Quad-SPI Controller

- 4 bytes (32-bit) and 3 bytes (24-bit) address width
- Maximum SPI Clock at Master Mode at 150MHz
- Single, Dual-Parallel, and Dual-Stacked mode
- 32-bit AXI Linear Address Mapping Interface for read operation
- Up to 2 chip select signals
- Write Protection Signal
- Hold signals
- 4-bit bidirectional I/O signals
- x1/x2/x4 Read speed required
- x1 write speed required only
- 64 byte Entry FIFO depth to improve QSPI read efficiency
- Built-in DMA for improved performance

Video Encoder/Decoder (VCU)

Zynq UltraScale+ MPSoCs include a Video codec (encoder/decoder) available in the devices designated with the EV suffix. The VCU is located in the PL and can be accessed from either the PL or PS.

- Simultaneous Encode and Decode through separate cores
- H.264 high profile level 5.2 (4Kx2K-60)
- H.265 (HEVC) main, main10 profile, level 5.1, high Tier, up to 4Kx2K-60 rate
- 8 and 10 bit encoding
- 4:2:0 and 4:2:2 chroma sampling
- 8Kx4K-15 rate
- Multi-stream up to total of 4Kx2K-60 rate
- Low Latency mode
- Can share the PS DRAM or use dedicated DRAM in the PL
- Clock/power management
- OpenMax Linux drivers

High-Performance AXI Ports

The high-performance AXI4 ports provide access from the PL to DDR and high-speed interconnect in the PS. The six dedicated AXI memory ports from the PL to the PS are configurable as either 128-bit, 64-bit, or 32-bit interfaces. These interfaces connect the PL to the memory interconnect via a FIFO interface. Two of the AXI interfaces support I/O coherent access to the APU caches.

Each high-performance AXI port has these characteristics:

- Reduced latency between PL and processing system memory
- 1KB deep FIFO
- Configurable either as 128-bit, 64-bit, or 32-bit AXI interfaces
- Multiple AXI command issuing to DDR

Accelerator Coherency Port (ACP)

The Zynq UltraScale+ MPSoC accelerator coherency port (ACP) is a 64-bit AXI slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACP directly connects the PL to the snoop control unit (SCU) of the ARM Cortex-A53 processors, enabling cache-coherent access to CPU data in the L2 cache. The ACP provides a low latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme. The ACP only snoops access in the CPU L2 cache, providing coherency in hardware. It does not support coherency on the PL side. So this interface is ideal for a DMA or an accelerator in the PL that only requires coherency on the CPU cache memories. For example, if a MicroBlaze™ processor in the PL is attached to the ACP interface, the cache of MicroBlaze processor will not be coherent with Cortex-A53 caches.

AXI Coherency Extension (ACE)

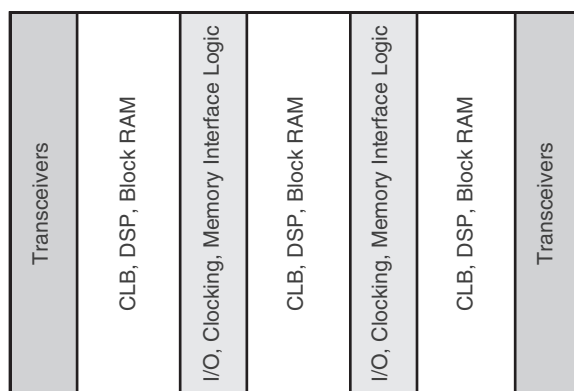
The Zynq UltraScale+ MPSoC AXI coherency extension (ACE) is a 64-bit AXI4 slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACE directly connects the PL to the snoop control unit (SCU) of the ARM Cortex-A53 processors, enabling cache-coherent access to Cache Coherent Interconnect (CCI). The ACE provides a low-latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme. The ACE snoops accesses to the CCI and the PL side, thus, providing full coherency in hardware. This interface can be used to hook up a cached interface in the PL to the PS as caches on both the Cortex-A53 memories and the PL master are snooped thus providing full coherency. For example, if a MicroBlaze processor in the PL is hooked up using an ACE interface, then Cortex-A53 and MicroBlaze processor caches will be coherent with each other.

Programmable Logic

This section covers the information about blocks in the Programmable Logic (PL).

Device Layout

UltraScale architecture-based devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of UltraScale+ MPSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. [Figure 1](#) shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.



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Figure 1: Device with Columnar Resources

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of device size or the mix of resources in the region, enabling repeatable timing results. Each segmented clock region contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. [Figure 2](#) is a representation of a device divided into regions.

Table 10: Transceiver Information

	Zynq UltraScale+ MPSoCs		
Type	PS-GTR	GTH	GTY
Qty	4	0–44	0–28
Max. Data Rate	6.0Gb/s	16.3Gb/s	32.75Gb/s
Min. Data Rate	1.25Gb/s	0.5Gb/s	0.5Gb/s
Applications	<ul style="list-style-type: none"> • PCIe Gen2 • USB • Ethernet 	<ul style="list-style-type: none"> • Backplane • PCIe Gen4 • HMC 	<ul style="list-style-type: none"> • 100G+ Optics • Chip-to-Chip • 25G+ Backplane • HMC

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for tough 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

Integrated Interface Blocks for PCI Express Designs

The MPSoC PL includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 3.1 for Gen3 and lower data rates and compatible with the PCI Express Base Specification Revision 4.0 (rev 0.5) for Gen4 data rates. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the MPSoC.

This block is highly configurable to system design requirements and can operate 1, 2, 4, 8, or 16 lanes at up to 2.5Gb/s, 5.0Gb/s, 8.0Gb/s, or 16Gb/s data rates. For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, MPSoC logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale architecture-based devices enable easy, reliable Interlaken switches and bridges.

PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

Zynq UltraScale+ MPSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

Clock Distribution

Clocks are distributed throughout Zynq UltraScale+ MPSoCs via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every Zynq UltraScale+ MPSoC includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, Zynq UltraScale+ MPSoC can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale architecture-based devices support the highest bandwidth HMC configuration of 64 lanes with a single device.

Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

Block RAM

Every UltraScale architecture-based device contains a number of 36Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Programmable Data Width

Each port can be configured as $32K \times 1$; $16K \times 2$; $8K \times 4$; $4K \times 9$ (or 8); $2K \times 18$ (or 16); $1K \times 36$ (or 32); or 512×72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from $16K \times 1$ to 512×36 . Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

UltraRAM

UltraRAM is a high-density, dual-port, synchronous memory block used in some UltraScale+ families. Both of the ports share the same clock and can address all of the $4K \times 72$ bits. Each port can independently read from or write to the memory array. UltraRAM supports two types of write enable schemes. The first mode is consistent with the block RAM byte write enable mode. The second mode allows gating the data and parity byte writes separately. Multiple UltraRAM blocks can be cascaded together to create larger memory arrays. UltraRAM blocks can be connected together to create larger memory arrays. Dedicated routing in the UltraRAM column enables the entire column height to be connected together. This makes UltraRAM an ideal solution for replacing external memories such as SRAM. Cascadable anywhere from 288Kb to 36Mb, UltraRAM provides the flexibility to fulfill many different memory requirements.

Error Detection and Correction

Each 64-bit-wide UltraRAM can generate, store and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale architecture-based devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27×18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

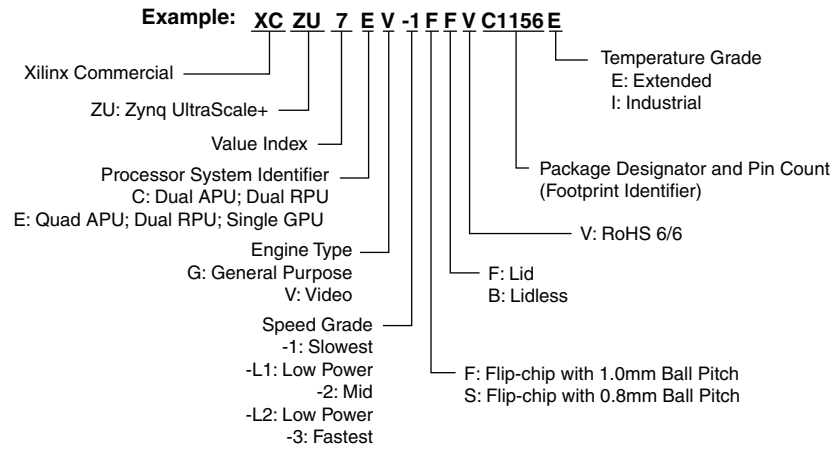
The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ devices is similar to the Kintex UltraScale and Virtex UltraScale devices but with the addition of a PMBus interface.

Zynq UltraScale+ MPSoCs contain one System Monitor in the PL and an additional block in the PS. The System Monitor in the PL has the same features as the block in UltraScale+ FPGAs. See [Table 11](#).

Table 11: Key System Monitor Features

	Zynq UltraScale+ MPSoC PL	Zynq UltraScale+ MPSoC PS
ADC	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP, PMBus	APB



1) -L1 and -L2 are the ordering codes for the low power -1L and -2L speed grades, respectively.

DS891_03_091216

Figure 3: Zynq UltraScale+ MPSoC Ordering Information

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/15/2017	1.4	Updated DSP count in Table 1 , Table 3 , and Table 5 . Updated I/O Electrical Characteristics . Updated Table 12 with -2E speed grade.
09/23/2016	1.3	Updated Table 2 ; Table 3 ; Table 4 ; Table 6 ; Graphics Processing Unit (GPU) ; and NAND ONFI 3.1 Flash Controller .
06/03/2016	1.2	Added CG devices: Updated Table 1 ; Table 2 ; Table 3 ; Table 4 ; Table 5 ; Table 6 ; and Table 12 . Added Video Encoder/Decoder (VCU) ; Table 7 ; and Power Examples (removed XPE Computed Range table). Updated: General Description ; ARM Cortex-A53 Based Application Processing Unit (APU) ; Zynq UltraScale+ MPSoCs ; Dynamic Memory Controller (DDRC) ; and Figure 3 .
01/28/2016	1.1	Updated Table 1 and Table 2 .
11/24/2015	1.0	Initial Xilinx release.

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