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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

| | |
|-------------------------|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™ -400 MP2 |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, WDT |
| Connectivity | CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 500MHz, 600MHz, 1.2GHz |
| Primary Attributes | Zynq@UltraScale+™ FPGA, 192K+ Logic Cells |
| Operating Temperature | 0°C ~ 100°C (Tj) |
| Package / Case | 900-BBGA, FCBGA |
| Supplier Device Package | 900-FCBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xczu4ev-1fbvb900e |

Feature Summary

Table 1: Zynq UltraScale+ MPSoC: CG Device Feature Summary

| | ZU2CG | ZU3CG | ZU4CG | ZU5CG | ZU6CG | ZU7CG | ZU9CG |
|---|---|---------|---------|---------|---------|---------|---------|
| Application Processing Unit | Dual-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache | | | | | | |
| Real-Time Processing Unit | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM | | | | | | |
| Embedded and External Memory | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC | | | | | | |
| General Connectivity | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters | | | | | | |
| High-Speed Connectivity | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII | | | | | | |
| System Logic Cells | 103,320 | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 |
| CLB Flip-Flops | 94,464 | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 |
| CLB LUTs | 47,232 | 70,560 | 87,840 | 117,120 | 214,604 | 230,400 | 274,080 |
| Distributed RAM (Mb) | 1.2 | 1.8 | 2.6 | 3.5 | 6.9 | 6.2 | 8.8 |
| Block RAM Blocks | 150 | 216 | 128 | 144 | 714 | 312 | 912 |
| Block RAM (Mb) | 5.3 | 7.6 | 4.5 | 5.1 | 25.1 | 11.0 | 32.1 |
| UltraRAM Blocks | 0 | 0 | 48 | 64 | 0 | 96 | 0 |
| UltraRAM (Mb) | 0 | 0 | 14.0 | 18.0 | 0 | 27.0 | 0 |
| DSP Slices | 240 | 360 | 728 | 1,248 | 1,973 | 1,728 | 2,520 |
| CMTs | 3 | 3 | 4 | 4 | 4 | 8 | 4 |
| Max. HP I/O ⁽¹⁾ | 156 | 156 | 156 | 156 | 208 | 416 | 208 |
| Max. HD I/O ⁽²⁾ | 96 | 96 | 96 | 96 | 120 | 48 | 120 |
| System Monitor | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GTH Transceiver 16.3Gb/s ⁽³⁾ | 0 | 0 | 16 | 16 | 24 | 24 | 24 |
| GTY Transceivers 32.75Gb/s | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Transceiver Fractional PLLs | 0 | 0 | 8 | 8 | 12 | 12 | 12 |
| PCIe Gen3 x16 and Gen4 x8 | 0 | 0 | 2 | 2 | 0 | 2 | 0 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 100G Ethernet w/ RS-FEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 2](#).

Table 2: Zynq UltraScale+ MPSoC: CG Device-Package Combinations and Maximum I/Os

| Package (1)(2)(3)(4)(5) | Package Dimensions (mm) | ZU2CG | ZU3CG | ZU4CG | ZU5CG | ZU6CG | ZU7CG | ZU9CG |
|----------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| | | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY |
| SBVA484(6) | 19x19 | 24, 58 0, 0 | 24, 58 0, 0 | | | | | |
| SFVA625 | 21x21 | 24, 156 0, 0 | 24, 156 0, 0 | | | | | |
| SFVC784(7) | 23x23 | 96, 156 0, 0 | 96, 156 0, 0 | 96, 156 4, 0 | 96, 156 4, 0 | | | |
| FBVB900 | 31x31 | | | 48, 156 16, 0 | 48, 156 16, 0 | | 48, 156 16, 0 | |
| FFVC900 | 31x31 | | | | | 48, 156 16, 0 | | 48, 156 16, 0 |
| FFVB1156 | 35x35 | | | | | 120, 208 24, 0 | | 120, 208 24, 0 |
| FFVC1156 | 35x35 | | | | | | 48, 312 20, 0 | |
| FFVF1517 | 40x40 | | | | | | 48, 416 24, 0 | |

Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2CG and ZU3CG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CCO} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Table 3: Zynq UltraScale+ MPSoC: EG Device Feature Summary

| | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|---|---|---------|---------|---------|---------|---------|---------|---------|---------|---------|-----------|
| Application Processing Unit | Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache | | | | | | | | | | |
| Real-Time Processing Unit | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM | | | | | | | | | | |
| Embedded and External Memory | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC | | | | | | | | | | |
| General Connectivity | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters | | | | | | | | | | |
| High-Speed Connectivity | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII | | | | | | | | | | |
| Graphic Processing Unit | ARM Mali™-400 MP2; 64KB L2 Cache | | | | | | | | | | |
| System Logic Cells | 103,320 | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 | 653,100 | 746,550 | 926,194 | 1,143,450 |
| CLB Flip-Flops | 94,464 | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 | 597,120 | 682,560 | 846,806 | 1,045,440 |
| CLB LUTs | 47,232 | 70,560 | 87,840 | 117,120 | 214,604 | 230,400 | 274,080 | 298,560 | 341,280 | 423,403 | 522,720 |
| Distributed RAM (Mb) | 1.2 | 1.8 | 2.6 | 3.5 | 6.9 | 6.2 | 8.8 | 9.1 | 11.3 | 8.0 | 9.8 |
| Block RAM Blocks | 150 | 216 | 128 | 144 | 714 | 312 | 912 | 600 | 744 | 796 | 984 |
| Block RAM (Mb) | 5.3 | 7.6 | 4.5 | 5.1 | 25.1 | 11.0 | 32.1 | 21.1 | 26.2 | 28.0 | 34.6 |
| UltraRAM Blocks | 0 | 0 | 48 | 64 | 0 | 96 | 0 | 80 | 112 | 102 | 128 |
| UltraRAM (Mb) | 0 | 0 | 14.0 | 18.0 | 0 | 27.0 | 0 | 22.5 | 31.5 | 28.7 | 36.0 |
| DSP Slices | 240 | 360 | 728 | 1,248 | 1,973 | 1,728 | 2,520 | 2,928 | 3,528 | 1,590 | 1,968 |
| CMTs | 3 | 3 | 4 | 4 | 4 | 8 | 4 | 8 | 4 | 11 | 11 |
| Max. HP I/O ⁽¹⁾ | 156 | 156 | 156 | 156 | 208 | 416 | 208 | 416 | 208 | 572 | 572 |
| Max. HD I/O ⁽²⁾ | 96 | 96 | 96 | 96 | 120 | 48 | 120 | 96 | 120 | 96 | 96 |
| System Monitor | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GTH Transceiver 16.3Gb/s ⁽³⁾ | 0 | 0 | 16 | 16 | 24 | 24 | 24 | 32 | 24 | 44 | 44 |
| GTY Transceivers 32.75Gb/s | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 0 | 28 | 28 |
| Transceiver Fractional PLLs | 0 | 0 | 8 | 8 | 12 | 12 | 12 | 24 | 12 | 36 | 36 |
| PCIe Gen3 x16 and Gen4 x8 | 0 | 0 | 2 | 2 | 0 | 2 | 0 | 4 | 0 | 4 | 5 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | 4 |
| 100G Ethernet w/ RS-FEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 0 | 2 | 4 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 4](#).

Table 4: Zynq UltraScale+ MPSoC: EG Device-Package Combinations and Maximum I/Os

| Package (1)(2)(3)(4)(5) | Package Dimensions (mm) | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|----------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| | | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY |
| SBVA484(6) | 19x19 | 24, 58 0, 0 | 24, 58 0, 0 | | | | | | | | | |
| SFVA625 | 21x21 | 24, 156 0, 0 | 24, 156 0, 0 | | | | | | | | | |
| SFVC784(7) | 23x23 | 96, 156 0, 0 | 96, 156 0, 0 | 96, 156 4, 0 | 96, 156 4, 0 | | | | | | | |
| FBVB900 | 31x31 | | | 48, 156 16, 0 | 48, 156 16, 0 | | 48, 156 16, 0 | | | | | |
| FFVC900 | 31x31 | | | | | 48, 156 16, 0 | | 48, 156 16, 0 | | 48, 156 16, 0 | | |
| FFVB1156 | 35x35 | | | | | 120, 208 24, 0 | | 120, 208 24, 0 | | 120, 208 24, 0 | | |
| FFVC1156 | 35x35 | | | | | | 48, 312 20, 0 | | 48, 312 20, 0 | | | |
| FFVB1517 | 40x40 | | | | | | | | 72, 416 16, 0 | | 72, 572 16, 0 | 72, 572 16, 0 |
| FFVF1517 | 40x40 | | | | | | 48, 416 24, 0 | | 48, 416 32, 0 | | | |
| FFVC1760 | 42.5x42.5 | | | | | | | | 96, 416 32, 16 | | 96, 416 32, 16 | 96, 416 32, 16 |
| FFVD1760 | 42.5x42.5 | | | | | | | | | | 48, 260 44, 28 | 48, 260 44, 28 |
| FFVE1924 | 45x45 | | | | | | | | | | 96, 572 44, 0 | 96, 572 44, 0 |

Notes:

1. Go to [Ordering Information](#) for package designation details.(5)
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CC0} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

ASIC-class capabilities afforded by the UltraScale MPSoC architecture while supporting rapid system development.

The inclusion of an application processor enables high-level operating system support, e.g., Linux. Other standard operating systems used with the Cortex-A53 processor are also available for the Zynq UltraScale+ MPSoC family. The PS and the PL are on separate power domains, enabling users to power down the PL for power management if required. The processors in the PS always boot first, allowing a software centric approach for PL configuration. PL configuration is managed by software running on the CPU, so it boots similar to an ASSP.

Processing System

Application Processing Unit (APU)

The key features of the APU include:

- 64-bit quad-core ARM Cortex-A53 MPCores. Features associated with each core include:
 - ARM v8-A Architecture
 - Operating target frequency: up to 1.5GHz
 - Single and double precision floating point: 4 SP / 2 DP FLOPs
 - NEON Advanced SIMD support with single and double precision floating point instructions
 - A64 instruction set in 64-bit operating mode, A32/T32 instruction set in 32-bit operating mode
 - Level 1 cache (separate instruction and data, 32KB each for each Cortex-A53 CPU)
 - 2-way set-associative Instruction Cache with parity support
 - 4-way set-associative Data Cache with ECC support
 - Integrated memory management unit (MMU) per processor core
 - TrustZone for secure mode operation
 - Virtualization support
- Ability to operate in single processor, symmetric quad processor, and asymmetric quad-processor modes
- Integrated 16-way set-associative 1MB Unified Level 2 cache with ECC support
- Interrupts and Timers
 - Generic interrupt controller (GIC-400)
 - ARM generic timers (4 timers per CPU)
 - One watchdog timer (WDT)
 - One global timer
 - Two triple timers/counters (TTC)
- Little and big endian support
 - Big endian support in BE8 mode
- CoreSight debug and trace support
 - Embedded Trace Macrocell (ETM) for instruction trace
 - Cross trigger interface (CTI) enabling hardware breakpoints and triggers
- ACP interface to PL for I/O coherency and Level 2 cache allocation
- ACE interface to PL for full coherency
- Power island gating on each processor core
- Optional eFUSE disable per core

Real-Time Processing Unit (RPU)

- Dual-core ARM Cortex-R5 MPCores. Features associated with each core include:
 - ARM v7-R Architecture (32-bit)
 - Operating target frequency: Up to 600MHz
 - A32/T32 instruction set support
 - 4-way set-associative Level 1 caches (separate instruction and data, 32KB each) with ECC support
 - Integrated Memory Protection Unit (MPU) per processor
 - 128KB Tightly Coupled Memory (TCM) with ECC support
 - TCMs can be combined to become 256KB in lockstep mode
- Ability to operate in single-processor or dual-processor modes (split and lock-step)
- Little and big endian support
- Dedicated SWDT and two Triple Timer Counters (TTC)
- CoreSight debug and trace support
 - Embedded Trace Macrocell (ETM) for instruction and trace
 - Cross trigger interface (CTI) enabling hardware breakpoints and triggers
- Optional eFUSE disable

Full-Power Domain DMA (FPD-DMA) and Low-Power Domain DMA (LPD-DMA)

- Two general-purpose DMA controllers one in the full-power domain (FPD-DMA) and one in the low-power domain (LPD-DMA)
- Eight independent channels per DMA
- Multiple transfer types:
 - Memory-to-memory
 - Memory-to-peripheral
 - Peripheral-to-memory and
 - Scatter-gather
- 8 peripheral interfaces per DMA
- TrustZone per DMA for optional secure operation

- Audio support
 - A single stream carries up to 8 LPCM channels at 192kHz with 24-bit resolution
 - Supports compressed formats including DRA, Dolby MAT, and DTS HD
 - Multi-Stream Transport can extend the number of audio channels
 - Audio copy protection
 - 2-channel streaming or input from the PL
 - Multi-channel non-streaming audio from a memory audio frame buffer
- Includes a System Time Clock (STC) compliant with ISO/IEC 13818-1
- Boot-time display using minimum resources

Platform Management Unit (PMU)

- Performs system initialization during boot
- Acts as a delegate to the application and real-time processors during sleep state
- Initiates power-up and restart after the wake-up request
- Maintains the system power state at all time
- Manages the sequence of low-level events required for power-up, power-down, reset, clock gating, and power gating of islands and domains
- Provides error management (error handling and reporting)
- Provides safety check functions (e.g., memory scrubbing)

The PMU includes the following blocks:

- Platform management processor
- Fixed ROM for boot-up of the device
- 128KB RAM with ECC for optional user/firmware code
- Local and global registers to manage power-down, power-up, reset, clock gating, and power gating requests
- Interrupt controller with 16 interrupts from other modules and the inter-processor communication interface (IPI)
- GPI and GPO interfaces to and from PS I/O and PL
- JTAG interface for PMU debug
- Optional User-Defined Firmware

- Sleep Mode with automatic wake-up
- Snoop Mode
- 16-bit timestamping for receive messages
- Both internal generated reference clock and external reference clock input from MIO
- Guarantee clock sampling edge between 80 to 83% at 24MHz reference clock input
- Optional eFUSE disable per port

USB 2.0

- Two USB controllers (configurable as USB 2.0 or USB 3.0)
- Host, device and On-The-Go (OTG) modes
- High Speed, Full Speed, and Low Speed
- Up to 12 endpoints
- 8-bit ULPI External PHY Interface
- The USB host controller registers and data structures are compliant to Intel xHCI specifications.
- 64-bit AXI master port with built-in DMA
- Power management features: hibernation mode

Static Memory Interfaces

The static memory interfaces support external static memories.

- ONFI 3.1 NAND flash support with up to 24-bit ECC
- 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash
- 8-bit eMMC interface supporting managed NAND flash

NAND ONFI 3.1 Flash Controller

- ONFI 3.1 compliant
- Supports chip select reduction per ONFI 3.1 spec
- SLC NAND for boot/configuration and data storage
- ECC options based on SLC NAND
 - 1, 4, or 8 bits per 512+spare bytes
 - 24 bits per 1024+spare bytes
- Maximum throughput as follows
 - Asynchronous mode (SDR) 24.3MB/s
 - Synchronous mode (NV-DDR) 112MB/s (for 100MHz flash clock)
- 8-bit SDR NAND interface

Interconnect

All the blocks are connected to each other and to the PL through a multi-layered ARM Advanced Microprocessor Bus Architecture (AMBA) AXI interconnect. The interconnect is non-blocking and supports multiple simultaneous master-slave transactions.

The interconnect is designed with latency sensitive masters, such as the ARM CPU, having the shortest paths to memory, and bandwidth critical masters, such as the potential PL masters, having high throughput connections to the slaves with which they need to communicate.

Traffic through the interconnect can be regulated through the Quality of Service (QoS) block in the interconnect. The QoS feature is used to regulate traffic generated by the CPU, DMA controller, and a combined entity representing the masters in the IOP.

PS Interfaces

PS interfaces include external interfaces going off-chip or signals going from PS to PL.

PS External Interfaces

The Zynq UltraScale+ MPSoC's external interfaces use dedicated pins that cannot be assigned as PL pins. These include:

- Clock, reset, boot mode, and voltage reference
- Up to 78 dedicated multiplexed I/O (MIO) pins, software-configurable to connect to any of the internal I/O peripherals and static memory controllers
- 32-bit or 64-bit DDR4/DDR3/DDR3L/LPDDR3 memories with optional ECC
- 32-bit LPDDR4 memory with optional ECC
- 4 channels (TX and RX pair) for transceivers

MIO Overview

The IOP peripherals communicate to external devices through a shared pool of up to 78 dedicated multiplexed I/O (MIO) pins. Each peripheral can be assigned one of several pre-defined groups of pins, enabling a flexible assignment of multiple devices simultaneously. Although 78 pins are not enough for simultaneous use of all the I/O peripherals, most IOP interface signals are available to the PL, allowing use of standard PL I/O pins when powered up and properly configured. Extended multiplexed I/O (EMIO) allows unmapped PS peripherals to access PL I/O.

Port mappings can appear in multiple locations. For example, there are up to 12 possible port mappings for CAN pins. The PS Configuration Wizard (PCW) tool aids in peripheral and static memory pin mapping.

Table 8: MIO Peripheral Interface Mapping

| Peripheral Interface | MIO | EMIO |
|--|---|---|
| Quad-SPI NAND | Yes | No |
| USB2.0: 0,1 | Yes: External PHY | No |
| SDIO 0,1 | Yes | Yes |
| SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO | Yes CAN: External PHY GPIO: Up to 78 bits | Yes CAN: External PHY GPIO: Up to 96 bits |
| GigE: 0,1,2,3 | RGMII v2.0: External PHY | Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic |
| UART: 0,1 | Simple UART: Only two pins (TX and RX) | Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: <ul style="list-style-type: none"> Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, <i>or</i> Eight Programmable Logic (PL) pins |
| Debug Trace Ports | Yes: Up to 16 trace bits | Yes: Up to 32 trace bits |
| Processor JTAG | Yes | Yes |

Transceiver (PS-GTR)

The four PS-GTR transceivers, which reside in the full power domain (FPD), support data rates of up to 6.0Gb/s. All the protocols cannot be pinned out at the same time. At any given time, four differential pairs can be pinned out using the transceivers. This is user programmable via the high-speed I/O multiplexer (HS-MIO).

- A Quad transceiver PS-GTR (TX/RX pair) able to support following standards simultaneously
 - x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
 - 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
 - 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
 - 1 or 2 USB3.0 channels at 5.0Gb/s
 - 1-4 Ethernet SGMII channels at 1.25Gb/s
- Provides flexible host-programmable multiplexing function for connecting the transceiver resources to the PS masters (DisplayPort, PCIe, Serial-ATA, USB3.0, and GigE).

High-Performance AXI Ports

The high-performance AXI4 ports provide access from the PL to DDR and high-speed interconnect in the PS. The six dedicated AXI memory ports from the PL to the PS are configurable as either 128-bit, 64-bit, or 32-bit interfaces. These interfaces connect the PL to the memory interconnect via a FIFO interface. Two of the AXI interfaces support I/O coherent access to the APU caches.

Each high-performance AXI port has these characteristics:

- Reduced latency between PL and processing system memory
- 1KB deep FIFO
- Configurable either as 128-bit, 64-bit, or 32-bit AXI interfaces
- Multiple AXI command issuing to DDR

Accelerator Coherency Port (ACP)

The Zynq UltraScale+ MPSoC accelerator coherency port (ACP) is a 64-bit AXI slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACP directly connects the PL to the snoop control unit (SCU) of the ARM Cortex-A53 processors, enabling cache-coherent access to CPU data in the L2 cache. The ACP provides a low latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme. The ACP only snoops access in the CPU L2 cache, providing coherency in hardware. It does not support coherency on the PL side. So this interface is ideal for a DMA or an accelerator in the PL that only requires coherency on the CPU cache memories. For example, if a MicroBlaze™ processor in the PL is attached to the ACP interface, the cache of MicroBlaze processor will not be coherent with Cortex-A53 caches.

AXI Coherency Extension (ACE)

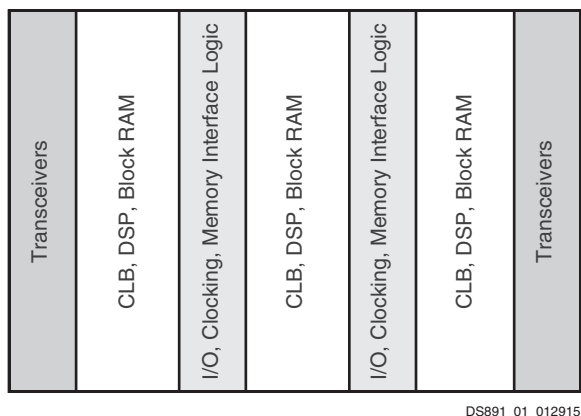
The Zynq UltraScale+ MPSoC AXI coherency extension (ACE) is a 64-bit AXI4 slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACE directly connects the PL to the snoop control unit (SCU) of the ARM Cortex-A53 processors, enabling cache-coherent access to Cache Coherent Interconnect (CCI). The ACE provides a low-latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme. The ACE snoops accesses to the CCI and the PL side, thus, providing full coherency in hardware. This interface can be used to hook up a cached interface in the PL to the PS as caches on both the Cortex-A53 memories and the PL master are snooped thus providing full coherency. For example, if a MicroBlaze processor in the PL is hooked up using an ACE interface, then Cortex-A53 and MicroBlaze processor caches will be coherent with each other.

Programmable Logic

This section covers the information about blocks in the Programmable Logic (PL).

Device Layout

UltraScale architecture-based devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of UltraScale+ MPSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. [Figure 1](#) shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.



DS891_01_012915

Figure 1: Device with Columnar Resources

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of device size or the mix of resources in the region, enabling repeatable timing results. Each segmented clock region contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. [Figure 2](#) is a representation of a device divided into regions.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CC0} or split (Thevenin) termination to $V_{CC0}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Ultra-fast serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100 Gb/s and 400 Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Three types of transceivers are used in Zynq UltraScale+ MPSoCs: GTH, GTY, and PS-GTR. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. [Table 10](#) compares the available transceivers.

PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

Zynq UltraScale+ MPSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

Clock Distribution

Clocks are distributed throughout Zynq UltraScale+ MPSoCs via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every Zynq UltraScale+ MPSoC includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, Zynq UltraScale+ MPSoC can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale architecture-based devices support the highest bandwidth HMC configuration of 64 lanes with a single device.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale architecture-based devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27×18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ devices is similar to the Kintex UltraScale and Virtex UltraScale devices but with the addition of a PMBus interface.

Zynq UltraScale+ MPSoCs contain one System Monitor in the PL and an additional block in the PS. The System Monitor in the PL has the same features as the block in UltraScale+ FPGAs. See [Table 11](#).

Table 11: Key System Monitor Features

| | Zynq UltraScale+ MPSoC PL | Zynq UltraScale+ MPSoC PS |
|------------|---------------------------|---------------------------|
| ADC | 10-bit 200kSPS | 10-bit 1MSPS |
| Interfaces | JTAG, I2C, DRP, PMBus | APB |

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor inputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the PMU in the PS.

Packaging

The UltraScale architecture-based devices are available in a variety of organic flip-chip and lidless flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

System-Level Features

Several functions span both the PS and PL and include:

- Reset Management
- Clock Management
- Power Domains
- PS Boot and Device Configuration
- Hardware and Software Debug Support

Reset Management

The reset management function provides the ability to reset the entire device or individual units within it. The PS supports these reset functions and signals:

- External and internal power-on reset signal
- Warm reset
- Watchdog timer reset
- User resets to PL
- Software, watchdog timer, or JTAG provided resets
- Security violation reset (locked down reset)

Clock Management

The PS in Zynq UltraScale+ MPSoCs is equipped with five phase-locked loops (PLLs), providing flexibility in configuring the clock domains within the PS. There are four primary clock domains of interest within the PS. These include the APU, the RPU, the DDR controller, and the I/O peripherals (IOP). The frequencies of all of these domains can be configured independently under software control.

Power Domains

The Zynq UltraScale+ MPSoC contains four separate power domains. When they are connected to separate power supplies, they can be completely powered down independently of each other without consuming any dynamic or static power. The processing system includes:

- Full Power Domain (FPD)
- Low Power Domain (LPD)
- Battery Powered Domain (BPD)

In addition to these three Processing System power domains, the PL can also be completely powered down if connected to separate power supplies.

The Full Power Domain (FPD) consists of the following major blocks:

- Application Processing Unit (APU)
- DMA (FP-DMA)
- Graphics Processing Unit (GPU)
- Dynamic Memory Controller (DDRC)
- High-Speed I/O Peripherals

The Low Power Domain (LPD) consists of the following major blocks:

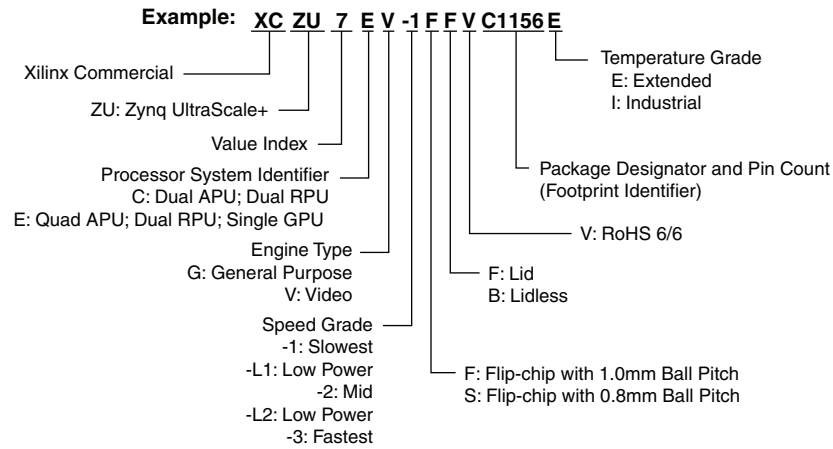
- Real-Time Processing Unit (RPU)
- DMA (LP-DMA)
- Platform Management Unit (PMU)
- Configuration Security Unit (CSU)
- Low-Speed I/O Peripherals
- Static Memory Interfaces

The Battery Power Domain (BPD) is the lowest power domain of the Zynq UltraScale+ MPSoC processing system. In this mode, all the PS is powered off except the Real-Time Clock (RTC) and battery-backed RAM (BBRAM).

Power Examples

Power for the Zynq UltraScale+ MPSoCs varies depending on the utilization of the PL resources, and the frequency of the PS and PL. To estimate power, use the Xilinx Power Estimator (XPE) at:

http://www.xilinx.com/products/design_tools/logic_design/xpe.htm



1) -L1 and -L2 are the ordering codes for the low power -1L and -2L speed grades, respectively.

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Figure 3: Zynq UltraScale+ MPSoC Ordering Information

Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|------------|---------|---|
| 02/15/2017 | 1.4 | Updated DSP count in Table 1 , Table 3 , and Table 5 . Updated I/O Electrical Characteristics . Updated Table 12 with -2E speed grade. |
| 09/23/2016 | 1.3 | Updated Table 2 ; Table 3 ; Table 4 ; Table 6 ; Graphics Processing Unit (GPU) ; and NAND ONFI 3.1 Flash Controller . |
| 06/03/2016 | 1.2 | Added CG devices: Updated Table 1 ; Table 2 ; Table 3 ; Table 4 ; Table 5 ; Table 6 ; and Table 12 . Added Video Encoder/Decoder (VCU) ; Table 7 ; and Power Examples (removed XPE Computed Range table). Updated: General Description ; ARM Cortex-A53 Based Application Processing Unit (APU) ; Zynq UltraScale+ MPSoCs ; Dynamic Memory Controller (DDRC) ; and Figure 3 . |
| 01/28/2016 | 1.1 | Updated Table 1 and Table 2 . |
| 11/24/2015 | 1.0 | Initial Xilinx release. |

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