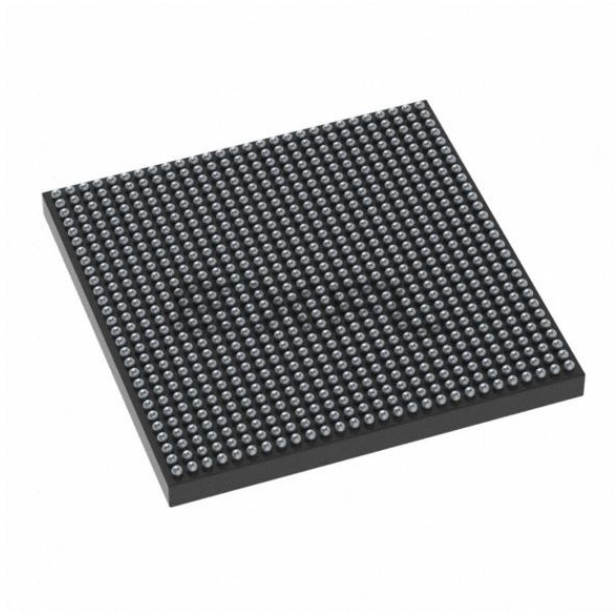
AMD Xilinx - XCZU5EG-3SFVC784E Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz, 1.5GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 256K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	784-BFBGA, FCBGA
Supplier Device Package	784-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu5eg-3sfvc784e

ARM Mali-400 Based GPU

- Supports OpenGL ES 1.1 and 2.0
- Supports OpenVG 1.1
- GPU frequency: Up to 667MHz
- Single Geometry Processor, Two Pixel Processors
- Pixel Fill Rate: 2 Mpixels/sec/MHz
- Triangle Rate: 0.11 Mtriangles/sec/MHz
- 64KB L2 Cache
- Power island gating

External Memory Interfaces

- Multi-protocol dynamic memory controller
- 32-bit or 64-bit interfaces to DDR4, DDR3, DDR3L, or LPDDR3 memories, and 32-bit interface to LPDDR4 memory
- ECC support in 64-bit and 32-bit modes
- Up to 32GB of address space using single or dual rank of 8-, 16-, or 32-bit-wide memories
- Static memory interfaces
  - eMMC4.51 Managed NAND flash support
  - ONFI3.1 NAND flash with 24-bit ECC
  - 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash

8-Channel DMA Controller

- Two DMA controllers of 8-channels each
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

Serial Transceivers

- Four dedicated PS-GTR receivers and transmitters supports up to 6.0Gb/s data rates
  - Supports SGMII tri-speed Ethernet, PCI Express® Gen2, Serial-ATA (SATA), USB3.0, and DisplayPort

Dedicated I/O Peripherals and Interfaces

- PCI Express — Compliant with PCIe® 2.1 base specification
  - Root complex and End Point configurations
  - x1, x2, and x4 at Gen1 or Gen2 rates
- SATA Host
  - 1.5, 3.0, and 6.0Gb/s data rates as defined by SATA Specification, revision 3.1
  - Supports up to two channels
- DisplayPort Controller
  - Up to 5.4Gb/s rate
  - Up to two TX lanes (no RX support)
- Four 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
  - Scatter-gather DMA capability
  - Recognition of IEEE Std 1588 rev.2 PTP frames
  - GMII, RGMII, and SGMII interfaces
  - Jumbo frames
- Two USB 3.0/2.0 Device, Host, or OTG peripherals, each supporting up to 12 endpoints
  - USB 3.0/2.0 compliant device IP core
  - Super-speed, high- speed, full-speed, and low-speed modes
  - Intel XHCI- compliant USB host
- Two full CAN 2.0B-compliant CAN bus interfaces
  - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
- Two SD/SDIO 2.0/eMMC4.51 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1Mb/s)
- Two master and slave I2C interfaces
- Up to 78 flexible multiplexed I/O (MIO) (up to three banks of 26 I/Os) for peripheral pin assignment
- Up to 96 EMIOs (up to three banks of 32 I/Os) connected to the PL

Interconnect

- High-bandwidth connectivity within PS and between PS and PL
- ARM AMBA® AXI4-based
- QoS support for latency and bandwidth control
- Cache Coherent Interconnect (CCI)

System Memory Management

- System Memory Management Unit (SMMU)
- Xilinx Memory Protection Unit (XMPU)

Platform Management Unit

- Power gates PS peripherals, power islands, and power domains
- Clock gates PS peripheral user firmware option

Configuration and Security Unit

- Boots PS and configures PL
- Supports secure and non-secure boot modes

System Monitor in PS

- On-chip voltage and temperature sensing

Feature Summary

Table 1: **Zynq UltraScale+ MPSoC: CG Device Feature Summary**

	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Application Processing Unit	Dual-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache						
Real-Time Processing Unit	Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM						
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC						
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters						
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII						
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8
Block RAM Blocks	150	216	128	144	714	312	912
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1
UltraRAM Blocks	0	0	48	64	0	96	0
UltraRAM (Mb)	0	0	14.0	18.0	0	27.0	0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520
CMTs	3	3	4	4	4	8	4
Max. HP I/O(1)	156	156	156	156	208	416	208
Max. HD I/O(2)	96	96	96	96	120	48	120
System Monitor	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s(3)	0	0	16	16	24	24	24
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0
Transceiver Fractional PLLs	0	0	8	8	12	12	12
PCIe Gen3 x16 and Gen4 x8	0	0	2	2	0	2	0
150G Interlaken	0	0	0	0	0	0	0
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See Table 2.

Table 4: **Zynq UltraScale+ MPSoC: EG Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0									
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0									
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0							
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0					
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0		48, 156 16, 0		
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0		120, 208 24, 0		
FFVC1156	35x35						48, 312 20, 0		48, 312 20, 0			
FFVB1517	40x40								72, 416 16, 0		72, 572 16, 0	72, 572 16, 0
FFVF1517	40x40						48, 416 24, 0		48, 416 32, 0			
FFVC1760	42.5x42.5								96, 416 32, 16		96, 416 32, 16	96, 416 32, 16
FFVD1760	42.5x42.5										48, 260 44, 28	48, 260 44, 28
FFVE1924	45x45										96, 572 44, 0	96, 572 44, 0

Notes:

1. Go to Ordering Information for package designation details.(5)
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CCO} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Table 6: **Zynq UltraScale+ MPSoC: EV Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)	Package Dimensions (mm)	ZU4EV	ZU5EV	ZU7EV
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SFVC784(5)	23x23	96, 156 4, 0	96, 156 4, 0	
FBVB900	31x31	48, 156 16, 0	48, 156 16, 0	48, 156 16, 0
FFVC1156	35x35			48, 312 20, 0
FFVF1517	40x40			48, 416 24, 0

Notes:

1. Go to Ordering Information for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. Packages with the same last letter and number sequence, e.g., C784, are footprint compatible with all other UltraScale devices with the same sequence. The footprint compatible devices within this family are outlined.
5. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

- Low power modes
  - Active/precharge power down
  - Self-refresh, including clean exit from self-refresh after a controller power cycle
- Enhanced DDR training by allowing software to measure read/write eye and make delay adjustments dynamically
- Independent performance monitors for read path and write path
- Integration of PHY Debug Access Port (DAP) into JTAG for testing

The DDR memory controller is multi-ported and enables the PS and the PL to have shared access to a common memory. The DDR controller features six AXI slave ports for this purpose:

- Two 128-bit AXI ports from the ARM Cortex-A53 CPU(s), RPU (ARM Cortex-R5 and LPD peripherals), GPU, high speed peripherals (USB3, PCIe & SATA), and High Performance Ports (HP0 & HP1) from the PL through the Cache Coherent Interconnect (CCI)
- One 64-bit port is dedicated for the ARM Cortex-R5 CPU(s)
- One 128-bit AXI port from the DisplayPort and HP2 port from the PL
- One 128-bit AXI port from HP3 and HP4 ports from the PL
- One 128-bit AXI port from General DMA and HP5 from the PL

High-Speed Connectivity Peripherals

PCIe

- Compliant with the PCI Express Base Specification 2.1
- Fully compliant with PCI Express transaction ordering rules
- Lane width: x1, x2, or x4 at Gen1 or Gen2 rates
- 1 Virtual Channel
- Full duplex PCIe port
- End Point and single PCIe link Root Port
- Root Port supports Enhanced Configuration Access Mechanism (ECAM), Cfg Transaction generation
- Root Port support for INTx, and MSI
- Endpoint support for MSI or MSI-X
  - 1 physical function, no SR-IOV
  - No relaxed or ID ordering
  - Fully configurable BARs
  - INTx not recommended, but can be generated
  - Endpoint to support configurable target/slave apertures with address translation and Interrupt capability

- Audio support
  - A single stream carries up to 8 LPCM channels at 192kHz with 24-bit resolution
  - Supports compressed formats including DRA, Dolby MAT, and DTS HD
  - Multi-Stream Transport can extend the number of audio channels
  - Audio copy protection
  - 2-channel streaming or input from the PL
  - Multi-channel non-streaming audio from a memory audio frame buffer
- Includes a System Time Clock (STC) compliant with ISO/IEC 13818-1
- Boot-time display using minimum resources

Platform Management Unit (PMU)

- Performs system initialization during boot
- Acts as a delegate to the application and real-time processors during sleep state
- Initiates power-up and restart after the wake-up request
- Maintains the system power state at all time
- Manages the sequence of low-level events required for power-up, power-down, reset, clock gating, and power gating of islands and domains
- Provides error management (error handling and reporting)
- Provides safety check functions (e.g., memory scrubbing)

The PMU includes the following blocks:

- Platform management processor
- Fixed ROM for boot-up of the device
- 128KB RAM with ECC for optional user/firmware code
- Local and global registers to manage power-down, power-up, reset, clock gating, and power gating requests
- Interrupt controller with 16 interrupts from other modules and the inter-processor communication interface (IPI)
- GPI and GPO interfaces to and from PS I/O and PL
- JTAG interface for PMU debug
- Optional User-Defined Firmware

Configuration Security Unit (CSU)

- Triple redundant Secure Processor Block (SPB) with built-in ECC
- Crypto Interface Block consisting of
  - 256-bit AES-GCM
  - SHA-3/384
  - 4096-bit RSA
- Key Management Unit
- Built-in DMA
- PCAP interface
- Supports ROM validation during pre-configuration stage
- Loads First Stage Boot Loader (FSBL) into OCM in either secure or non-secure boot modes
- Supports voltage, temperature, and frequency monitoring after configuration

Xilinx Peripheral Protection Unit (XPPU)

- Provides peripheral protection support
- Up to 20 masters simultaneously
- Multiple aperture sizes
- Access control for a specified set of address apertures on a per master basis
- 64KB peripheral apertures and controls access on per peripheral basis

I/O Peripherals

The IOP unit contains the data communication peripherals. Key features of the IOP include:

Triple-Speed Gigabit Ethernet

- Compatible with IEEE Std 802.3 and supports 10/100/1000Mb/s transfer rates (Full and Half duplex)
- Supports jumbo frames
- Built-in Scatter-Gather DMA capability
- Statistics counter registers for RMON/MIB
- Multiple I/O types (1.8, 2.5, 3.3V) on RGMII interface with external PHY
- GMII interface to PL to support interfaces as: TBI, SGMII, and RGMII v2.0 support
- Automatic pad and cyclic redundancy check (CRC) generation on transmitted frames
- Transmitter and Receive IP, TCP, and UDP checksum offload
- MDIO interface for physical layer management

- Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Supports IEEE Std 1588 v2

SD/SDIO 3.0 Controller

In addition to secure digital (SD) devices, this controller also supports eMMC 4.51.

- Host mode support only
- Built-in DMA
- 1/4-Bit SD Specification, version 3.0
- 1/4/8-Bit eMMC Specification, version 4.51
- Supports primary boot from SD Card and eMMC (Managed NAND)
- High speed, default speed, and low-speed support
- 1 and 4-bit data interface support
  - Low speed clock 0-400KHz
  - Default speed 0-25MHz
  - High speed clock 0-50MHz
- High speed Interface
  - SD UHS-1: 208MHz
  - eMMC HS200: 200MHz
- Memory, I/O, and SD cards
- Power control modes
- Data FIFO interface up to 512B

UART

- Programmable baud rate generator
- 6, 7, or 8 data bits
- 1, 1.5, or 2 stop bits
- Odd, even, space, mark, or no parity
- Parity, framing, and overrun error detection
- Line break generation and detection
- Automatic echo, local loopback, and remote loopback channel modes
- Modem control signals: CTS, RTS, DSR, DTR, RI, and DCD (from EMIO only)

SPI

- Full-duplex operation offers simultaneous receive and transmit
- 128B deep read and write FIFO
- Master or slave SPI mode
- Up to 3 chip select lines
- Multi-master environment
- Identifies an error condition if more than one master detected
- Selectable master clock reference
- Software can poll for status or be interrupt driven

I2C

- 128-bit buffer size
- Both normal (100kHz) and fast bus data rates (400kHz)
- Master or slave mode
- Normal or extended addressing
- I2C bus hold for slow host service

GPIO

- Up to 128 GPIO bits
  - Up to 78-bits from MIO and 96-bits from EMIO
- Each GPIO bit can be dynamically programmed as input or output
- Independent reset values for each bit of all registers
- Interrupt request generation for each GPIO signals
- Single Channel (Bit) write capability for all control registers include data output register, direction control register, and interrupt clear register
- Read back in output mode

CAN

- Conforms to the ISO 11898 -1, CAN2.0A, and CAN 2.0B standards
- Both standard (11-bit identifier) and extended (29-bit identifier) frames
- Bit rates up to 1Mb/s
- Transmit and Receive message FIFO with a depth of 64 messages
- Watermark interrupts for TXFIFO and RXFIFO
- Automatic re-transmission on errors or arbitration loss in normal mode
- Acceptance filtering of 4 acceptance filters

- Sleep Mode with automatic wake-up
- Snoop Mode
- 16-bit timestamping for receive messages
- Both internal generated reference clock and external reference clock input from MIO
- Guarantee clock sampling edge between 80 to 83% at 24MHz reference clock input
- Optional eFUSE disable per port

USB 2.0

- Two USB controllers (configurable as USB 2.0 or USB 3.0)
- Host, device and On-The-Go (OTG) modes
- High Speed, Full Speed, and Low Speed
- Up to 12 endpoints
- 8-bit ULPI External PHY Interface
- The USB host controller registers and data structures are compliant to Intel xHCI specifications.
- 64-bit AXI master port with built-in DMA
- Power management features: hibernation mode

Static Memory Interfaces

The static memory interfaces support external static memories.

- ONFI 3.1 NAND flash support with up to 24-bit ECC
- 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash
- 8-bit eMMC interface supporting managed NAND flash

NAND ONFI 3.1 Flash Controller

- ONFI 3.1 compliant
- Supports chip select reduction per ONFI 3.1 spec
- SLC NAND for boot/configuration and data storage
- ECC options based on SLC NAND
    - 1, 4, or 8 bits per 512+spare bytes
    - 24 bits per 1024+spare bytes
- Maximum throughput as follows
    - Asynchronous mode (SDR) 24.3MB/s
    - Synchronous mode (NV-DDR) 112MB/s (for 100MHz flash clock)
- 8-bit SDR NAND interface

Table 8: **MIO Peripheral Interface Mapping**

Peripheral Interface	MIO	EMIO
Quad-SPI NAND	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 78 bits	Yes CAN: External PHY GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: • Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, *or* • Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

Transceiver (PS-GTR)

The four PS-GTR transceivers, which reside in the full power domain (FPD), support data rates of up to 6.0Gb/s. All the protocols cannot be pinned out at the same time. At any given time, four differential pairs can be pinned out using the transceivers. This is user programmable via the high-speed I/O multiplexer (HS-MIO).

- A Quad transceiver PS-GTR (TX/RX pair) able to support following standards simultaneously
  - x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
  - 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
  - 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
  - 1 or 2 USB3.0 channels at 5.0Gb/s
  - 1-4 Ethernet SGMII channels at 1.25Gb/s
- Provides flexible host-programmable multiplexing function for connecting the transceiver resources to the PS masters (DisplayPort, PCIe, Serial-ATA, USB3.0, and GigE).

Table 10: **Transceiver Information**

	Zynq UltraScale+ MPSoCs		
Type	PS-GTR	GTH	GTY
Qty	4	0–44	0–28
Max. Data Rate	6.0Gb/s	16.3Gb/s	32.75Gb/s
Min. Data Rate	1.25Gb/s	0.5Gb/s	0.5Gb/s
Applications	• PCIe Gen2 • USB • Ethernet	• Backplane • PCIe Gen4 • HMC	• 100G+ Optics • Chip-to-Chip • 25G+ Backplane • HMC

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for tough 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

Integrated Interface Blocks for PCI Express Designs

The MPSoC PL includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 3.1 for Gen3 and lower data rates and compatible with the PCI Express Base Specification Revision 4.0 (rev 0.5) for Gen4 data rates. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the MPSoC.

This block is highly configurable to system design requirements and can operate 1, 2, 4, 8, or 16 lanes at up to 2.5Gb/s, 5.0Gb/s, 8.0Gb/s, or 16Gb/s data rates. For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, MPSoC logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale architecture-based devices enable easy, reliable Interlaken switches and bridges.

PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

Zynq UltraScale+ MPSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

Clock Distribution

Clocks are distributed throughout Zynq UltraScale+ MPSoCs via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every Zynq UltraScale+ MPSoC includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, Zynq UltraScale+ MPSoC can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale architecture-based devices support the highest bandwidth HMC configuration of 64 lanes with a single device.

Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

Block RAM

Every UltraScale architecture-based device contains a number of 36Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale architecture-based devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27 × 18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ devices is similar to the Kintex UltraScale and Virtex UltraScale devices but with the addition of a PMBus interface.

Zynq UltraScale+ MPSoCs contain one System Monitor in the PL and an additional block in the PS. The System Monitor in the PL has the same features as the block in UltraScale+ FPGAs. See Table 11.

Table 11: **Key System Monitor Features**

	Zynq UltraScale+ MPSoC PL	Zynq UltraScale+ MPSoC PS
ADC	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP, PMBus	APB

Clock Management

The PS in Zynq UltraScale+ MPSoCs is equipped with five phase-locked loops (PLLs), providing flexibility in configuring the clock domains within the PS. There are four primary clock domains of interest within the PS. These include the APU, the RPU, the DDR controller, and the I/O peripherals (IOP). The frequencies of all of these domains can be configured independently under software control.

Power Domains

The Zynq UltraScale+ MPSoC contains four separate power domains. When they are connected to separate power supplies, they can be completely powered down independently of each other without consuming any dynamic or static power. The processing system includes:

- Full Power Domain (FPD)
- Low Power Domain (LPD)
- Battery Powered Domain (BPD)

In addition to these three Processing System power domains, the PL can also be completely powered down if connected to separate power supplies.

The Full Power Domain (FPD) consists of the following major blocks:

- Application Processing Unit (APU)
- DMA (FP-DMA)
- Graphics Processing Unit (GPU)
- Dynamic Memory Controller (DDRC)
- High-Speed I/O Peripherals

The Low Power Domain (LPD) consists of the following major blocks:

- Real-Time Processing Unit (RPU)
- DMA (LP-DMA)
- Platform Management Unit (PMU)
- Configuration Security Unit (CSU)
- Low-Speed I/O Peripherals
- Static Memory Interfaces

The Battery Power Domain (BPD) is the lowest power domain of the Zynq UltraScale+ MPSoC processing system. In this mode, all the PS is powered off except the Real-Time Clock (RTC) and battery-backed RAM (BBRAM).

Power Examples

Power for the Zynq UltraScale+ MPSoCs varies depending on the utilization of the PL resources, and the frequency of the PS and PL. To estimate power, use the Xilinx Power Estimator (XPE) at:

http://www.xilinx.com/products/design_tools/logic_design/xpe.htm

Ordering Information

Table 12 shows the speed and temperature grades available in the different device families.

Table 12: **Speed Grade and Temperature Grade**

Device Family	Devices	Speed Grade and Temperature Grade			
		Commercial (C)	Extended (E)		Industrial (I)
		0°C to +85°C	0°C to +100°C	0°C to +110°C	–40°C to +100°C
Zynq UltraScale+	CG Devices		-2E (0.85V)		-2I (0.85V)
				-2LE(1)(2) (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI(2) (0.85V or 0.72V)
	ZU2EG ZU3EG		-2E (0.85V)		-2I (0.85V)
				-2LE(1)(2) (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI(2) (0.85V or 0.72V)
	ZU4EG ZU5EG ZU6EG ZU7EG ZU9EG ZU11EG ZU15EG ZU17EG ZU19EG		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE(1)(2) (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI(2) (0.85V or 0.72V)
	EV Devices		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE(1)(2) (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI(2) (0.85V or 0.72V)

Notes:

1. In -2LE speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal at 0.85V or low voltage at 0.72V). Operation at 110°C Tj is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of device lifetime.
2. In Zynq UltraScale+ MPSoCs, when operating the PL at low voltage (0.72V), the PS operates at nominal voltage (0.85V)

The ordering information shown in Figure 3 applies to all packages in the Zynq UltraScale+ MPSoCs.

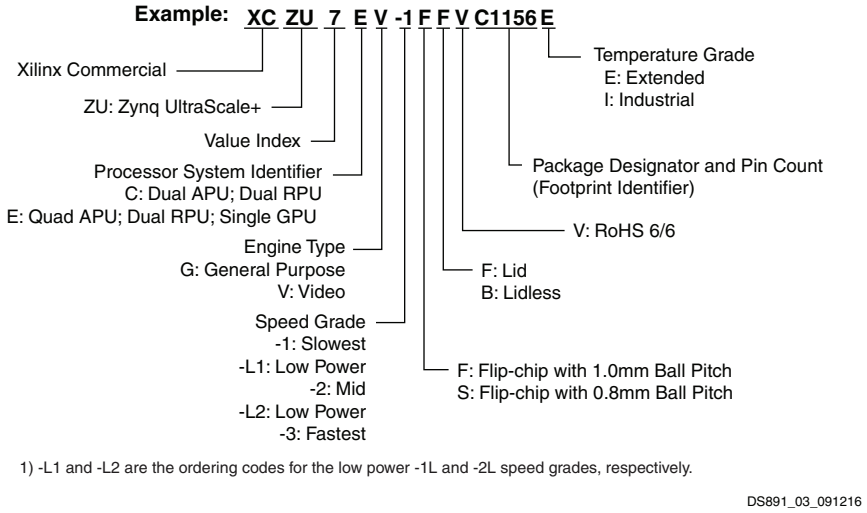

Figure 3: **Zynq UltraScale+ MPSoC Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/15/2017	1.4	Updated DSP count in Table 1, Table 3, and Table 5. Updated I/O Electrical Characteristics. Updated Table 12 with -2E speed grade.
09/23/2016	1.3	Updated Table 2; Table 3; Table 4; Table 6; Graphics Processing Unit (GPU); and NAND ONFI 3.1 Flash Controller.
06/03/2016	1.2	Added CG devices: Updated Table 1; Table 2; Table 3; Table 4; Table 5; Table 6; and Table 12. Added Video Encoder/Decoder (VCU); Table 7; and Power Examples (removed XPE Computed Range table). Updated: General Description; ARM Cortex-A53 Based Application Processing Unit (APU); Zynq UltraScale+ MPSoCs; Dynamic Memory Controller (DDRC); and Figure 3.
01/28/2016	1.1	Updated Table 1 and Table 2.
11/24/2015	1.0	Initial Xilinx release.

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