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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™ -400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq@UltraScale+™ FPGA, 599K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (Tj)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu9eg-2ffvb1156i

Table 4: Zynq UltraScale+ MPSoC: EG Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
		HD, HP GTH, GTY										
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0									
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0									
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0							
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0					
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0		48, 156 16, 0		
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0		120, 208 24, 0		
FFVC1156	35x35						48, 312 20, 0		48, 312 20, 0			
FFVB1517	40x40								72, 416 16, 0		72, 572 16, 0	72, 572 16, 0
FFVF1517	40x40						48, 416 24, 0		48, 416 32, 0			
FFVC1760	42.5x42.5								96, 416 32, 16		96, 416 32, 16	96, 416 32, 16
FFVD1760	42.5x42.5										48, 260 44, 28	48, 260 44, 28
FFVE1924	45x45										96, 572 44, 0	96, 572 44, 0

Notes:

1. Go to [Ordering Information](#) for package designation details.(5)
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CC0} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+ MPSoCs

A comprehensive device family, Zynq UltraScale+ MPSoCs offer single-chip, all programmable, heterogeneous multiprocessors that provide designers with software, hardware, interconnect, power, security, and I/O programmability. The range of devices in the Zynq UltraScale+ MPSoC family allows designers to target cost-sensitive as well as high-performance applications from a single platform using industry-standard tools. While each Zynq UltraScale+ MPSoC contains the same PS, the PL, Video hard blocks, and I/O resources vary between the devices.

Table 7: Zynq UltraScale+ MPSoC Device Features

	CG Devices	EG Devices	EV Devices
APU	Dual-core ARM Cortex-A53	Quad-core ARM Cortex-A53	Quad-core ARM Cortex-A53
RPU	Dual-core ARM Cortex-R5	Dual-core ARM Cortex-R5	Dual-core ARM Cortex-R5
GPU	–	Mali-400MP2	Mali-400MP2
VCU	–	–	H.264/H.265

The Zynq UltraScale+ MPSoCs are able to serve a wide range of applications including:

- Automotive: Driver assistance, driver information, and infotainment
- Wireless Communications: Support for multiple spectral bands and smart antennas
- Wired Communications: Multiple wired communications standards and context-aware network services
- Data Centers: Software Defined Networks (SDN), data pre-processing, and analytics
- Smarter Vision: Evolving video-processing algorithms, object detection, and analytics
- Connected Control/M2M: Flexible/adaptable manufacturing, factory throughput, quality, and safety

The UltraScale MPSoC architecture provides processor scalability from 32 to 64 bits with support for virtualization, the combination of soft and hard engines for real-time control, graphics/video processing, waveform and packet processing, next-generation interconnect and memory, advanced power management, and technology enhancements that deliver multi-level security, safety, and reliability. Xilinx offers a large number of soft IP for the Zynq UltraScale+ MPSoC family. Stand-alone and Linux device drivers are available for the peripherals in the PS and the PL. Xilinx's Vivado® Design Suite, SDK™, and PetaLinux development environments enable rapid product development for software, hardware, and systems engineers. The ARM-based PS also brings a broad range of third-party tools and IP providers in combination with Xilinx's existing PL ecosystem.

The Zynq UltraScale+ MPSoC family delivers unprecedented processing, I/O, and memory bandwidth in the form of an optimized mix of heterogeneous processing engines embedded in a next-generation, high-performance, on-chip interconnect with appropriate on-chip memory subsystems. The heterogeneous processing and programmable engines, which are optimized for different application tasks, enable the Zynq UltraScale+ MPSoCs to deliver the extensive performance and efficiency required to address next-generation smarter systems while retaining backwards compatibility with the original Zynq-7000 All Programmable SoC family. The UltraScale MPSoC architecture also incorporates multiple levels of security, increased safety, and advanced power management, which are critical requirements of next-generation smarter systems. Xilinx's embedded UltraFast™ design methodology fully exploits the

ASIC-class capabilities afforded by the UltraScale MPSoC architecture while supporting rapid system development.

The inclusion of an application processor enables high-level operating system support, e.g., Linux. Other standard operating systems used with the Cortex-A53 processor are also available for the Zynq UltraScale+ MPSoC family. The PS and the PL are on separate power domains, enabling users to power down the PL for power management if required. The processors in the PS always boot first, allowing a software centric approach for PL configuration. PL configuration is managed by software running on the CPU, so it boots similar to an ASSP.

Processing System

Application Processing Unit (APU)

The key features of the APU include:

- 64-bit quad-core ARM Cortex-A53 MPCores. Features associated with each core include:
 - ARM v8-A Architecture
 - Operating target frequency: up to 1.5GHz
 - Single and double precision floating point: 4 SP / 2 DP FLOPs
 - NEON Advanced SIMD support with single and double precision floating point instructions
 - A64 instruction set in 64-bit operating mode, A32/T32 instruction set in 32-bit operating mode
 - Level 1 cache (separate instruction and data, 32KB each for each Cortex-A53 CPU)
 - 2-way set-associative Instruction Cache with parity support
 - 4-way set-associative Data Cache with ECC support
 - Integrated memory management unit (MMU) per processor core
 - TrustZone for secure mode operation
 - Virtualization support
- Ability to operate in single processor, symmetric quad processor, and asymmetric quad-processor modes
- Integrated 16-way set-associative 1MB Unified Level 2 cache with ECC support
- Interrupts and Timers
 - Generic interrupt controller (GIC-400)
 - ARM generic timers (4 timers per CPU)
 - One watchdog timer (WDT)
 - One global timer
 - Two triple timers/counters (TTC)
- Little and big endian support
 - Big endian support in BE8 mode
- CoreSight debug and trace support
 - Embedded Trace Macrocell (ETM) for instruction trace
 - Cross trigger interface (CTI) enabling hardware breakpoints and triggers
- ACP interface to PL for I/O coherency and Level 2 cache allocation
- ACE interface to PL for full coherency
- Power island gating on each processor core
- Optional eFUSE disable per core

Xilinx Memory Protection Unit (XMPU)

- Region based memory protection unit
- Up to 16 regions
- Each region supports address alignment of 1MB or 4KB
- Regions can overlap; the higher region number has priority
- Each region can be independently enabled or disabled
- Each region has a start and end address

Graphics Processing Unit (GPU)

- Supports OpenGL ES 1.1 & 2.0
- Supports OpenVG 1.1
- Operating target frequency: up to 667MHz
- Single Geometry Processor and two Pixel processor
- Pixel Fill Rate: 2 Mpixel/sec/MHz
- Triangle Rate: 0.11 Mtriangles/sec/MHz
- 64KB Level 2 Cache (read-only)
- 4X and 16X Anti-aliasing Support
- ETC1 texture compression to reduce external memory bandwidth
- Extensive texture format support
 - RGBA 8888, 565, 1556
 - Mono 8, 16
 - YUV format support
- Automatic load balancing across different graphics shader engines
- 2D and 3D graphic acceleration
- Up to 4K texture input and 4K render output resolutions
- Each geometry processor and pixel processor supports 4KB page MMU
- Power island gating on each GPU engine and shared cache
- Optional eFUSE disable

Dynamic Memory Controller (DDRC)

- DDR3, DDR3L, DDR4, LPDDR3, LPDDR4
- Target data rate: Up to 2400Mb/s DDR4 operation in -1 speed grade
- 32-bit and 64-bit bus width support for DDR4, DDR3, DDR3L, or LPDDR3 memories, and 32-bit bus width support for LPDDR4 memory
- ECC support (using extra bits)
- Up to a total DRAM capacity of 32GB

SATA

- Compliant with SATA 3.1 Specification
- SATA host port supports up to 2 external devices
- Compliant with Advanced Host Controller Interface ('AHCI') ver. 1.3
- 1.5Gb/s, 3.0Gb/s, and 6.0Gb/s data rates
- Power management features: supports partial and slumber modes

USB 3.0

- Two USB controllers (configurable as USB 2.0 or USB 3.0)
- Up to 5.0Gb/s data rate
- Host and Device modes
 - Super Speed, High Speed, Full Speed, and Low Speed
 - Up to 12 endpoints
 - The USB host controller registers and data structures are compliant to Intel xHCI specifications
 - 64-bit AXI master port with built-in DMA
 - Power management features: Hibernation mode

DisplayPort Controller

- 4K Display Processing with DisplayPort output
 - Maximum resolution of 4K x 2K-30 (30Hz pixel rate)
 - DisplayPort AUX channel, and Hot Plug Detect (HPD) on the output
 - RGB YCbCr, 4:2:0; 4:2:2, 4:4:4 with 6, 8, 10, and 12b/c
 - Y-only, xvYCC, RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2, and YCbCr 4:2:0 video format with 6,8,10 and 12-bits per color component
 - 256-color palette
 - Multiple frame buffer formats
 - 1, 2, 4, 8 bits per pixel (bpp) via a palette
 - 16, 24, 32bpp
 - Graphics formats such as RGBA8888, RGB555, etc.
- Accepts streaming video from the PL or dedicated DMA controller
- Enables Alpha blending of graphics and Chroma keying

- Sleep Mode with automatic wake-up
- Snoop Mode
- 16-bit timestamping for receive messages
- Both internal generated reference clock and external reference clock input from MIO
- Guarantee clock sampling edge between 80 to 83% at 24MHz reference clock input
- Optional eFUSE disable per port

USB 2.0

- Two USB controllers (configurable as USB 2.0 or USB 3.0)
- Host, device and On-The-Go (OTG) modes
- High Speed, Full Speed, and Low Speed
- Up to 12 endpoints
- 8-bit ULPI External PHY Interface
- The USB host controller registers and data structures are compliant to Intel xHCI specifications.
- 64-bit AXI master port with built-in DMA
- Power management features: hibernation mode

Static Memory Interfaces

The static memory interfaces support external static memories.

- ONFI 3.1 NAND flash support with up to 24-bit ECC
- 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash
- 8-bit eMMC interface supporting managed NAND flash

NAND ONFI 3.1 Flash Controller

- ONFI 3.1 compliant
- Supports chip select reduction per ONFI 3.1 spec
- SLC NAND for boot/configuration and data storage
- ECC options based on SLC NAND
 - 1, 4, or 8 bits per 512+spare bytes
 - 24 bits per 1024+spare bytes
- Maximum throughput as follows
 - Asynchronous mode (SDR) 24.3MB/s
 - Synchronous mode (NV-DDR) 112MB/s (for 100MHz flash clock)
- 8-bit SDR NAND interface

- 2 chip selects
- Programmable access timing
- 1.8V and 3.3V I/O
- Built-in DMA for improved performance

Quad-SPI Controller

- 4 bytes (32-bit) and 3 bytes (24-bit) address width
- Maximum SPI Clock at Master Mode at 150MHz
- Single, Dual-Parallel, and Dual-Stacked mode
- 32-bit AXI Linear Address Mapping Interface for read operation
- Up to 2 chip select signals
- Write Protection Signal
- Hold signals
- 4-bit bidirectional I/O signals
- x1/x2/x4 Read speed required
- x1 write speed required only
- 64 byte Entry FIFO depth to improve QSPI read efficiency
- Built-in DMA for improved performance

Video Encoder/Decoder (VCU)

Zynq UltraScale+ MPSoCs include a Video codec (encoder/decoder) available in the devices designated with the EV suffix. The VCU is located in the PL and can be accessed from either the PL or PS.

- Simultaneous Encode and Decode through separate cores
- H.264 high profile level 5.2 (4Kx2K-60)
- H.265 (HEVC) main, main10 profile, level 5.1, high Tier, up to 4Kx2K-60 rate
- 8 and 10 bit encoding
- 4:2:0 and 4:2:2 chroma sampling
- 8Kx4K-15 rate
- Multi-stream up to total of 4Kx2K-60 rate
- Low Latency mode
- Can share the PS DRAM or use dedicated DRAM in the PL
- Clock/power management
- OpenMax Linux drivers

Interconnect

All the blocks are connected to each other and to the PL through a multi-layered ARM Advanced Microprocessor Bus Architecture (AMBA) AXI interconnect. The interconnect is non-blocking and supports multiple simultaneous master-slave transactions.

The interconnect is designed with latency sensitive masters, such as the ARM CPU, having the shortest paths to memory, and bandwidth critical masters, such as the potential PL masters, having high throughput connections to the slaves with which they need to communicate.

Traffic through the interconnect can be regulated through the Quality of Service (QoS) block in the interconnect. The QoS feature is used to regulate traffic generated by the CPU, DMA controller, and a combined entity representing the masters in the IOP.

PS Interfaces

PS interfaces include external interfaces going off-chip or signals going from PS to PL.

PS External Interfaces

The Zynq UltraScale+ MPSoC's external interfaces use dedicated pins that cannot be assigned as PL pins. These include:

- Clock, reset, boot mode, and voltage reference
- Up to 78 dedicated multiplexed I/O (MIO) pins, software-configurable to connect to any of the internal I/O peripherals and static memory controllers
- 32-bit or 64-bit DDR4/DDR3/DDR3L/LPDDR3 memories with optional ECC
- 32-bit LPDDR4 memory with optional ECC
- 4 channels (TX and RX pair) for transceivers

MIO Overview

The IOP peripherals communicate to external devices through a shared pool of up to 78 dedicated multiplexed I/O (MIO) pins. Each peripheral can be assigned one of several pre-defined groups of pins, enabling a flexible assignment of multiple devices simultaneously. Although 78 pins are not enough for simultaneous use of all the I/O peripherals, most IOP interface signals are available to the PL, allowing use of standard PL I/O pins when powered up and properly configured. Extended multiplexed I/O (EMIO) allows unmapped PS peripherals to access PL I/O.

Port mappings can appear in multiple locations. For example, there are up to 12 possible port mappings for CAN pins. The PS Configuration Wizard (PCW) tool aids in peripheral and static memory pin mapping.

Table 8: MIO Peripheral Interface Mapping

Peripheral Interface	MIO	EMIO
Quad-SPI NAND	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 78 bits	Yes CAN: External PHY GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: <ul style="list-style-type: none"> Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, <i>or</i> Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

Transceiver (PS-GTR)

The four PS-GTR transceivers, which reside in the full power domain (FPD), support data rates of up to 6.0Gb/s. All the protocols cannot be pinned out at the same time. At any given time, four differential pairs can be pinned out using the transceivers. This is user programmable via the high-speed I/O multiplexer (HS-MIO).

- A Quad transceiver PS-GTR (TX/RX pair) able to support following standards simultaneously
 - x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
 - 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
 - 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
 - 1 or 2 USB3.0 channels at 5.0Gb/s
 - 1-4 Ethernet SGMII channels at 1.25Gb/s
- Provides flexible host-programmable multiplexing function for connecting the transceiver resources to the PS masters (DisplayPort, PCIe, Serial-ATA, USB3.0, and GigE).

HS-MIO

The function of the HS-MIO is to multiplex access from the high-speed PS peripheral to the differential pair on the PS-GTR transceiver as defined in the configuration registers. Up to 4 channels of the transceiver are available for use by the high-speed interfaces in the PS.

Table 9: HS-MIO Peripheral Interface Mapping

Peripheral Interface	Lane0	Lane1	Lane2	Lane3
PCIe (x1, x2 or x4)	PCIe0	PCIe1	PCIe2	PCIe3
SATA (1 or 2 channels)	SATA0	SATA1	SATA0	SATA1
DisplayPort (TX only)	DP1	DPO	DP1	DPO
USB0	USB0	USB0	USB0	–
USB1	–	–	–	USB1
SGMII0	SGMII0	–	–	–
SGMII1	–	SGMII1	–	–
SGMII2	–	–	SGMII2	–
SGMII3	–	–	–	SGMII3

PS-PL Interface

The PS-PL interface includes:

- AMBA AXI4 interfaces for primary data communication
 - Six 128-bit/64-bit/32-bit High Performance (HP) Slave AXI interfaces from PL to PS.
 - Four 128-bit/64-bit/32-bit HP AXI interfaces from PL to PS DDR.
 - Two 128-bit/64-bit/32-bit high-performance coherent (HPC) ports from PL to cache coherent interconnect (CCI).
 - Two 128-bit/64-bit/32-bit HP Master AXI interfaces from PS to PL.
 - One 128-bit/64-bit/32-bit interface from PL to RPU in PS (PL_LPD) for low latency access to OCM.
 - One 128-bit/64-bit/32-bit AXI interface from RPU in PS to PL (LPD_PL) for low latency access to PL.
 - One 128-bit AXI interface (ACP port) for I/O coherent access from PL to Cortex-A53 cache memory. This interface provides coherency in hardware for Cortex-A53 cache memory.
 - One 128-bit AXI interface (ACE Port) for Fully coherent access from PL to Cortex-A53. This interface provides coherency in hardware for Cortex-A53 cache memory and the PL.
- Clocks and resets
 - Four PS clock outputs to the PL with start/stop control.
 - Four PS reset outputs to the PL.

High-Performance AXI Ports

The high-performance AXI4 ports provide access from the PL to DDR and high-speed interconnect in the PS. The six dedicated AXI memory ports from the PL to the PS are configurable as either 128-bit, 64-bit, or 32-bit interfaces. These interfaces connect the PL to the memory interconnect via a FIFO interface. Two of the AXI interfaces support I/O coherent access to the APU caches.

Each high-performance AXI port has these characteristics:

- Reduced latency between PL and processing system memory
- 1KB deep FIFO
- Configurable either as 128-bit, 64-bit, or 32-bit AXI interfaces
- Multiple AXI command issuing to DDR

Accelerator Coherency Port (ACP)

The Zynq UltraScale+ MPSoC accelerator coherency port (ACP) is a 64-bit AXI slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACP directly connects the PL to the snoop control unit (SCU) of the ARM Cortex-A53 processors, enabling cache-coherent access to CPU data in the L2 cache. The ACP provides a low latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme. The ACP only snoops access in the CPU L2 cache, providing coherency in hardware. It does not support coherency on the PL side. So this interface is ideal for a DMA or an accelerator in the PL that only requires coherency on the CPU cache memories. For example, if a MicroBlaze™ processor in the PL is attached to the ACP interface, the cache of MicroBlaze processor will not be coherent with Cortex-A53 caches.

AXI Coherency Extension (ACE)

The Zynq UltraScale+ MPSoC AXI coherency extension (ACE) is a 64-bit AXI4 slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACE directly connects the PL to the snoop control unit (SCU) of the ARM Cortex-A53 processors, enabling cache-coherent access to Cache Coherent Interconnect (CCI). The ACE provides a low-latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme. The ACE snoops accesses to the CCI and the PL side, thus, providing full coherency in hardware. This interface can be used to hook up a cached interface in the PL to the PS as caches on both the Cortex-A53 memories and the PL master are snooped thus providing full coherency. For example, if a MicroBlaze processor in the PL is hooked up using an ACE interface, then Cortex-A53 and MicroBlaze processor caches will be coherent with each other.

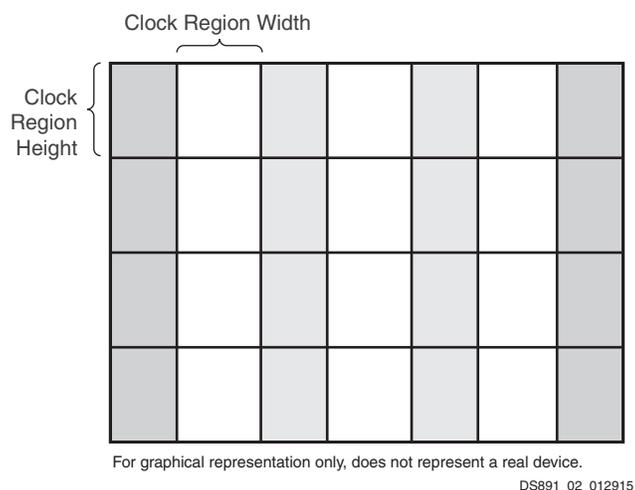


Figure 2: Column-Based Device Divided into Clock Regions

Input/Output

All Zynq UltraScale+ MPSoCs have I/O pins for communicating to external components. In addition, in the MPSoC's PS, there are another 78 I/Os that the I/O peripherals use to communicate to external components, referred to as multiplexed I/O (MIO). If more than 78 pins are required by the I/O peripherals, the I/O pins in the PL can be used to extend the MPSoC interfacing capability, referred to as extended MIO (EMIO).

The number of I/O pins in the PL of Zynq UltraScale+ MPSoCs varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-performance (HP), or high-density (HD). The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V. The HD I/Os are reduced-feature I/Os organized in banks of 24, providing voltage support from 1.2V to 3.3V.

All I/O pins are organized in banks, with 52 HP pins per bank or 24 HD pins per bank. Each bank has one common V_{CC0} output buffer power supply, which also powers certain input buffers. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CC0} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100 Ω internal resistor. All UltraScale architecture-based devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. The Zynq UltraScale+ family includes support for MIPI with a dedicated D-PHY in the I/O bank.

Programmable Data Width

Each port can be configured as $32K \times 1$; $16K \times 2$; $8K \times 4$; $4K \times 9$ (or 8); $2K \times 18$ (or 16); $1K \times 36$ (or 32); or 512×72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from $16K \times 1$ to 512×36 . Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

UltraRAM

UltraRAM is a high-density, dual-port, synchronous memory block used in some UltraScale+ families. Both of the ports share the same clock and can address all of the $4K \times 72$ bits. Each port can independently read from or write to the memory array. UltraRAM supports two types of write enable schemes. The first mode is consistent with the block RAM byte write enable mode. The second mode allows gating the data and parity byte writes separately. Multiple UltraRAM blocks can be cascaded together to create larger memory arrays. UltraRAM blocks can be connected together to create larger memory arrays. Dedicated routing in the UltraRAM column enables the entire column height to be connected together. This makes UltraRAM an ideal solution for replacing external memories such as SRAM. Cascadable anywhere from 288Kb to 36Mb, UltraRAM provides the flexibility to fulfill many different memory requirements.

Error Detection and Correction

Each 64-bit-wide UltraRAM can generate, store and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale architecture-based devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27×18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ devices is similar to the Kintex UltraScale and Virtex UltraScale devices but with the addition of a PMBus interface.

Zynq UltraScale+ MPSoCs contain one System Monitor in the PL and an additional block in the PS. The System Monitor in the PL has the same features as the block in UltraScale+ FPGAs. See [Table 11](#).

Table 11: Key System Monitor Features

	Zynq UltraScale+ MPSoC PL	Zynq UltraScale+ MPSoC PS
ADC	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP, PMBus	APB

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor inputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the PMU in the PS.

Packaging

The UltraScale architecture-based devices are available in a variety of organic flip-chip and lidless flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

System-Level Features

Several functions span both the PS and PL and include:

- Reset Management
- Clock Management
- Power Domains
- PS Boot and Device Configuration
- Hardware and Software Debug Support

Reset Management

The reset management function provides the ability to reset the entire device or individual units within it. The PS supports these reset functions and signals:

- External and internal power-on reset signal
- Warm reset
- Watchdog timer reset
- User resets to PL
- Software, watchdog timer, or JTAG provided resets
- Security violation reset (locked down reset)

Clock Management

The PS in Zynq UltraScale+ MPSoCs is equipped with five phase-locked loops (PLLs), providing flexibility in configuring the clock domains within the PS. There are four primary clock domains of interest within the PS. These include the APU, the RPU, the DDR controller, and the I/O peripherals (IOP). The frequencies of all of these domains can be configured independently under software control.

Power Domains

The Zynq UltraScale+ MPSoC contains four separate power domains. When they are connected to separate power supplies, they can be completely powered down independently of each other without consuming any dynamic or static power. The processing system includes:

- Full Power Domain (FPD)
- Low Power Domain (LPD)
- Battery Powered Domain (BPD)

In addition to these three Processing System power domains, the PL can also be completely powered down if connected to separate power supplies.

The Full Power Domain (FPD) consists of the following major blocks:

- Application Processing Unit (APU)
- DMA (FP-DMA)
- Graphics Processing Unit (GPU)
- Dynamic Memory Controller (DDRC)
- High-Speed I/O Peripherals

The Low Power Domain (LPD) consists of the following major blocks:

- Real-Time Processing Unit (RPU)
- DMA (LP-DMA)
- Platform Management Unit (PMU)
- Configuration Security Unit (CSU)
- Low-Speed I/O Peripherals
- Static Memory Interfaces

The Battery Power Domain (BPD) is the lowest power domain of the Zynq UltraScale+ MPSoC processing system. In this mode, all the PS is powered off except the Real-Time Clock (RTC) and battery-backed RAM (BBRAM).

Power Examples

Power for the Zynq UltraScale+ MPSoCs varies depending on the utilization of the PL resources, and the frequency of the PS and PL. To estimate power, use the Xilinx Power Estimator (XPE) at:

http://www.xilinx.com/products/design_tools/logic_design/xpe.htm

PS Boot and Device Configuration

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decrypts and authenticates the images while the 4096-bit RSA block authenticates the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. The CSU executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the OCM.

After copying the FSBL to OCM, one of the processors, either the Cortex-A53 or Cortex-R5, executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL), such as U-Boot. Users obtain example SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, eMMC, or Quad-SPI) is configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or callable after boot.

Hardware and Software Debug Support

The debug system used in Zynq UltraScale+ MPSoCs is based on the ARM CoreSight architecture. It uses ARM CoreSight components including an embedded trace controller (ETC), an embedded trace Macrocell (ETM) for each Cortex-A53 and Cortex-R5 processor, and a system trace Macrocell (STM). This enables advanced debug features like event trace, debug breakpoints and triggers, cross-trigger, and debug bus dump to memory. The programmable logic can be debugged with the Xilinx Vivado Logic Analyzer.

Debug Ports

Three JTAG ports are available and can be chained together or used separately. When chained together, a single port is used for chip-level JTAG functions, ARM processor code downloads and run-time control operations, PL configuration, and PL debug with the Vivado Logic Analyzer. This enables tools such as the Xilinx Software Development Kit (SDK) and Vivado Logic Analyzer to share a single download cable from Xilinx.

When the JTAG chain is split, one port is used to directly access the ARM DAP interface. This CoreSight interface enables the use of ARM-compliant debug and software development tools such as Development Studio 5 (DS-5™). The other JTAG port can then be used by the Xilinx FPGA tools for access to the PL, including configuration bitstream downloads and PL debug with the Vivado Logic Analyzer. In this mode, users can download to and debug the PL in the same manner as a stand-alone FPGA.

Ordering Information

Table 12 shows the speed and temperature grades available in the different device families.

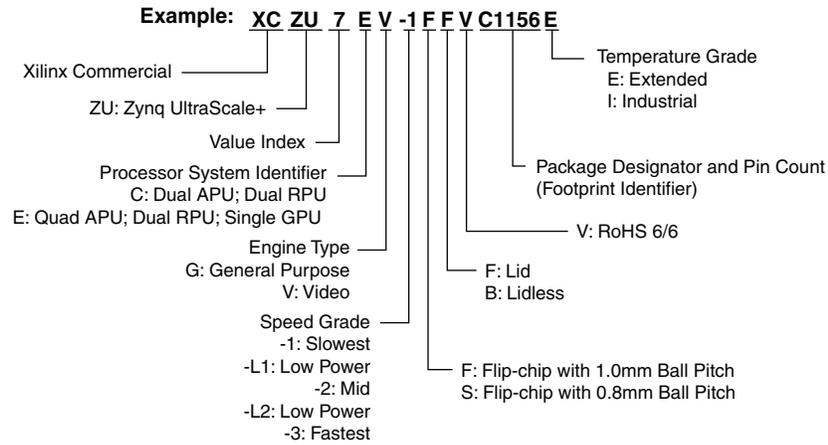
Table 12: Speed Grade and Temperature Grade

Device Family	Devices	Speed Grade and Temperature Grade			
		Commercial (C)	Extended (E)		Industrial (I)
		0°C to +85°C	0°C to +100°C	0°C to +110°C	-40°C to +100°C
Zynq UltraScale+	CG Devices		-2E (0.85V)		-2I (0.85V)
				-2LE ⁽¹⁾⁽²⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI ⁽²⁾ (0.85V or 0.72V)
	ZU2EG ZU3EG		-2E (0.85V)		-2I (0.85V)
				-2LE ⁽¹⁾⁽²⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI ⁽²⁾ (0.85V or 0.72V)
	ZU4EG ZU5EG ZU6EG ZU7EG ZU9EG ZU11EG ZU15EG ZU17EG ZU19EG		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE ⁽¹⁾⁽²⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI ⁽²⁾ (0.85V or 0.72V)
			-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
	EV Devices			-2LE ⁽¹⁾⁽²⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI ⁽²⁾ (0.85V or 0.72V)

Notes:

1. In -2LE speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal at 0.85V or low voltage at 0.72V). Operation at 110°C Tj is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of device lifetime.
2. In Zynq UltraScale+ MPSoCs, when operating the PL at low voltage (0.72V), the PS operates at nominal voltage (0.85V)

The ordering information shown in Figure 3 applies to all packages in the Zynq UltraScale+ MPSoCs.



1) -L1 and -L2 are the ordering codes for the low power -1L and -2L speed grades, respectively.

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Figure 3: Zynq UltraScale+ MPSoC Ordering Information