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[Embedded - System On Chip \(SoC\): The Heart of Modern Embedded Systems](#)

[Embedded - System On Chip \(SoC\)](#) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are [Embedded - System On Chip \(SoC\)](#)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™ -400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 599K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu9eg-l1ffvb1156i

ARM Mali-400 Based GPU

- Supports OpenGL ES 1.1 and 2.0
- Supports OpenVG 1.1
- GPU frequency: Up to 667MHz
- Single Geometry Processor, Two Pixel Processors
- Pixel Fill Rate: 2 Mpixels/sec/MHz
- Triangle Rate: 0.11 Mtriangles/sec/MHz
- 64KB L2 Cache
- Power island gating

External Memory Interfaces

- Multi-protocol dynamic memory controller
- 32-bit or 64-bit interfaces to DDR4, DDR3, DDR3L, or LPDDR3 memories, and 32-bit interface to LPDDR4 memory
- ECC support in 64-bit and 32-bit modes
- Up to 32GB of address space using single or dual rank of 8-, 16-, or 32-bit-wide memories
- Static memory interfaces
 - eMMC4.51 Managed NAND flash support
 - ONFI3.1 NAND flash with 24-bit ECC
 - 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash

8-Channel DMA Controller

- Two DMA controllers of 8-channels each
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

Serial Transceivers

- Four dedicated PS-GTR receivers and transmitters supports up to 6.0Gb/s data rates
 - Supports SGMII tri-speed Ethernet, PCI Express® Gen2, Serial-ATA (SATA), USB3.0, and DisplayPort

Dedicated I/O Peripherals and Interfaces

- PCI Express — Compliant with PCIe® 2.1 base specification
 - Root complex and End Point configurations
 - x1, x2, and x4 at Gen1 or Gen2 rates
- SATA Host
 - 1.5, 3.0, and 6.0Gb/s data rates as defined by SATA Specification, revision 3.1
 - Supports up to two channels
- DisplayPort Controller
 - Up to 5.4Gb/s rate
 - Up to two TX lanes (no RX support)

- Four 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
 - Scatter-gather DMA capability
 - Recognition of IEEE Std 1588 rev.2 PTP frames
 - GMII, RGMII, and SGMII interfaces
 - Jumbo frames
- Two USB 3.0/2.0 Device, Host, or OTG peripherals, each supporting up to 12 endpoints
 - USB 3.0/2.0 compliant device IP core
 - Super-speed, high-speed, full-speed, and low-speed modes
 - Intel XHCI- compliant USB host
- Two full CAN 2.0B-compliant CAN bus interfaces
 - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
- Two SD/SDIO 2.0/eMMC4.51 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1Mb/s)
- Two master and slave I2C interfaces
- Up to 78 flexible multiplexed I/O (MIO) (up to three banks of 26 I/Os) for peripheral pin assignment
- Up to 96 EMIOs (up to three banks of 32 I/Os) connected to the PL

Interconnect

- High-bandwidth connectivity within PS and between PS and PL
- ARM AMBA® AXI4-based
- QoS support for latency and bandwidth control
- Cache Coherent Interconnect (CCI)

System Memory Management

- System Memory Management Unit (SMMU)
- Xilinx Memory Protection Unit (XMPU)

Platform Management Unit

- Power gates PS peripherals, power islands, and power domains
- Clock gates PS peripheral user firmware option

Configuration and Security Unit

- Boots PS and configures PL
- Supports secure and non-secure boot modes

System Monitor in PS

- On-chip voltage and temperature sensing

Programmable Logic (PL)

Configurable Logic Blocks (CLB)

- Look-up tables (LUT)
- Flip-flops
- Cascadable adders

36Kb Block RAM

- True dual-port
- Up to 72 bits wide
- Configurable as dual 18Kb

UltraRAM

- 288Kb dual-port
- 72 bits wide
- Error checking and correction

DSP Blocks

- 27 x 18 signed multiply
- 48-bit adder/accumulator
- 27-bit pre-adder

Programmable I/O Blocks

- Supports LVCMOS, LVDS, and SSTL
- 1.0V to 3.3V I/O
- Programmable I/O delay and SerDes

JTAG Boundary-Scan

- IEEE Std 1149.1 Compatible Test Interface

PCI Express

- Supports Root complex and End Point configurations
- Supports up to Gen4 speeds
- Up to five integrated blocks in select devices

100G Ethernet MAC/PCS

- IEEE Std 802.3 compliant
- CAUI-10 (10x 10.3125Gb/s) or CAUI-4 (4x 25.78125Gb/s)
- RSFEC (IEEE Std 802.3bj) in CAUI-4 configuration
- Up to four integrated blocks in select devices

Interlaken

- Interlaken spec 1.2 compliant
- 64/67 encoding
- 12 x 12.5Gb/s or 6 x 25Gb/s
- Up to four integrated blocks in select devices

Video Encoder/Decoder (VCU)

- Available in EV devices
- Accessible from either PS or PL
- Simultaneous encode and decode
- H.264 and H.265 support

System Monitor in PL

- On-chip voltage and temperature sensing
- 10-bit 200KSPS ADC with up to 17 external inputs

Table 3: Zynq UltraScale+ MPSoC: EG Device Feature Summary

	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache										
Real-Time Processing Unit	Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM										
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC										
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters										
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII										
Graphic Processing Unit	ARM Mali™-400 MP2; 64KB L2 Cache										
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550	653,100	746,550	926,194	1,143,450
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160	597,120	682,560	846,806	1,045,440
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080	298,560	341,280	423,403	522,720
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
Block RAM Blocks	150	216	128	144	714	312	912	600	744	796	984
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
UltraRAM Blocks	0	0	48	64	0	96	0	80	112	102	128
UltraRAM (Mb)	0	0	14.0	18.0	0	27.0	0	22.5	31.5	28.7	36.0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
CMTs	3	3	4	4	4	8	4	8	4	11	11
Max. HP I/O ⁽¹⁾	156	156	156	156	208	416	208	416	208	572	572
Max. HD I/O ⁽²⁾	96	96	96	96	120	48	120	96	120	96	96
System Monitor	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s ⁽³⁾	0	0	16	16	24	24	24	32	24	44	44
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0	16	0	28	28
Transceiver Fractional PLLs	0	0	8	8	12	12	12	24	12	36	36
PCIe Gen3 x16 and Gen4 x8	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	1	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	2	0	2	4

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 4](#).

Table 6: Zynq UltraScale+ MPSoC: EV Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)(4)	Package Dimensions (mm)	ZU4EV	ZU5EV	ZU7EV
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SFVC784 ⁽⁵⁾	23x23	96, 156 4, 0	96, 156 4, 0	
FBVB900	31x31	48, 156 16, 0	48, 156 16, 0	48, 156 16, 0
FFVC1156	35x35			48, 312 20, 0
FFVF1517	40x40			48, 416 24, 0

Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. Packages with the same last letter and number sequence, e.g., C784, are footprint compatible with all other UltraScale devices with the same sequence. The footprint compatible devices within this family are outlined.
5. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+ MPSoCs

A comprehensive device family, Zynq UltraScale+ MPSoCs offer single-chip, all programmable, heterogeneous multiprocessors that provide designers with software, hardware, interconnect, power, security, and I/O programmability. The range of devices in the Zynq UltraScale+ MPSoC family allows designers to target cost-sensitive as well as high-performance applications from a single platform using industry-standard tools. While each Zynq UltraScale+ MPSoC contains the same PS, the PL, Video hard blocks, and I/O resources vary between the devices.

Table 7: Zynq UltraScale+ MPSoC Device Features

	CG Devices	EG Devices	EV Devices
APU	Dual-core ARM Cortex-A53	Quad-core ARM Cortex-A53	Quad-core ARM Cortex-A53
RPU	Dual-core ARM Cortex-R5	Dual-core ARM Cortex-R5	Dual-core ARM Cortex-R5
GPU	–	Mali-400MP2	Mali-400MP2
VCU	–	–	H.264/H.265

The Zynq UltraScale+ MPSoCs are able to serve a wide range of applications including:

- Automotive: Driver assistance, driver information, and infotainment
- Wireless Communications: Support for multiple spectral bands and smart antennas
- Wired Communications: Multiple wired communications standards and context-aware network services
- Data Centers: Software Defined Networks (SDN), data pre-processing, and analytics
- Smarter Vision: Evolving video-processing algorithms, object detection, and analytics
- Connected Control/M2M: Flexible/adaptable manufacturing, factory throughput, quality, and safety

The UltraScale MPSoC architecture provides processor scalability from 32 to 64 bits with support for virtualization, the combination of soft and hard engines for real-time control, graphics/video processing, waveform and packet processing, next-generation interconnect and memory, advanced power management, and technology enhancements that deliver multi-level security, safety, and reliability. Xilinx offers a large number of soft IP for the Zynq UltraScale+ MPSoC family. Stand-alone and Linux device drivers are available for the peripherals in the PS and the PL. Xilinx's Vivado® Design Suite, SDK™, and PetaLinux development environments enable rapid product development for software, hardware, and systems engineers. The ARM-based PS also brings a broad range of third-party tools and IP providers in combination with Xilinx's existing PL ecosystem.

The Zynq UltraScale+ MPSoC family delivers unprecedented processing, I/O, and memory bandwidth in the form of an optimized mix of heterogeneous processing engines embedded in a next-generation, high-performance, on-chip interconnect with appropriate on-chip memory subsystems. The heterogeneous processing and programmable engines, which are optimized for different application tasks, enable the Zynq UltraScale+ MPSoCs to deliver the extensive performance and efficiency required to address next-generation smarter systems while retaining backwards compatibility with the original Zynq-7000 All Programmable SoC family. The UltraScale MPSoC architecture also incorporates multiple levels of security, increased safety, and advanced power management, which are critical requirements of next-generation smarter systems. Xilinx's embedded UltraFast™ design methodology fully exploits the

Processing System

Application Processing Unit (APU)

The key features of the APU include:

- 64-bit quad-core ARM Cortex-A53 MPCores. Features associated with each core include:
 - ARM v8-A Architecture
 - Operating target frequency: up to 1.5GHz
 - Single and double precision floating point: 4 SP / 2 DP FLOPs
 - NEON Advanced SIMD support with single and double precision floating point instructions
 - A64 instruction set in 64-bit operating mode, A32/T32 instruction set in 32-bit operating mode
 - Level 1 cache (separate instruction and data, 32KB each for each Cortex-A53 CPU)
 - 2-way set-associative Instruction Cache with parity support
 - 4-way set-associative Data Cache with ECC support
 - Integrated memory management unit (MMU) per processor core
 - TrustZone for secure mode operation
 - Virtualization support
- Ability to operate in single processor, symmetric quad processor, and asymmetric quad-processor modes
- Integrated 16-way set-associative 1MB Unified Level 2 cache with ECC support
- Interrupts and Timers
 - Generic interrupt controller (GIC-400)
 - ARM generic timers (4 timers per CPU)
 - One watchdog timer (WDT)
 - One global timer
 - Two triple timers/counters (TTC)
- Little and big endian support
 - Big endian support in BE8 mode
- CoreSight debug and trace support
 - Embedded Trace Macrocell (ETM) for instruction trace
 - Cross trigger interface (CTI) enabling hardware breakpoints and triggers
- ACP interface to PL for I/O coherency and Level 2 cache allocation
- ACE interface to PL for full coherency
- Power island gating on each processor core
- Optional eFUSE disable per core

Real-Time Processing Unit (RPU)

- Dual-core ARM Cortex-R5 MPCores. Features associated with each core include:
 - ARM v7-R Architecture (32-bit)
 - Operating target frequency: Up to 600MHz
 - A32/T32 instruction set support
 - 4-way set-associative Level 1 caches (separate instruction and data, 32KB each) with ECC support
 - Integrated Memory Protection Unit (MPU) per processor
 - 128KB Tightly Coupled Memory (TCM) with ECC support
 - TCMs can be combined to become 256KB in lockstep mode
- Ability to operate in single-processor or dual-processor modes (split and lock-step)
- Little and big endian support
- Dedicated SWDT and two Triple Timer Counters (TTC)
- CoreSight debug and trace support
 - Embedded Trace Macrocell (ETM) for instruction and trace
 - Cross trigger interface (CTI) enabling hardware breakpoints and triggers
- Optional eFUSE disable

Full-Power Domain DMA (FPD-DMA) and Low-Power Domain DMA (LPD-DMA)

- Two general-purpose DMA controllers one in the full-power domain (FPD-DMA) and one in the low-power domain (LPD-DMA)
- Eight independent channels per DMA
- Multiple transfer types:
 - Memory-to-memory
 - Memory-to-peripheral
 - Peripheral-to-memory and
 - Scatter-gather
- 8 peripheral interfaces per DMA
- TrustZone per DMA for optional secure operation

Xilinx Memory Protection Unit (XMPU)

- Region based memory protection unit
- Up to 16 regions
- Each region supports address alignment of 1MB or 4KB
- Regions can overlap; the higher region number has priority
- Each region can be independently enabled or disabled
- Each region has a start and end address

Graphics Processing Unit (GPU)

- Supports OpenGL ES 1.1 & 2.0
- Supports OpenVG 1.1
- Operating target frequency: up to 667MHz
- Single Geometry Processor and two Pixel processor
- Pixel Fill Rate: 2 Mpixel/sec/MHz
- Triangle Rate: 0.11 Mtriangles/sec/MHz
- 64KB Level 2 Cache (read-only)
- 4X and 16X Anti-aliasing Support
- ETC1 texture compression to reduce external memory bandwidth
- Extensive texture format support
 - RGBA 8888, 565, 1556
 - Mono 8, 16
 - YUV format support
- Automatic load balancing across different graphics shader engines
- 2D and 3D graphic acceleration
- Up to 4K texture input and 4K render output resolutions
- Each geometry processor and pixel processor supports 4KB page MMU
- Power island gating on each GPU engine and shared cache
- Optional eFUSE disable

Dynamic Memory Controller (DDRC)

- DDR3, DDR3L, DDR4, LPDDR3, LPDDR4
- Target data rate: Up to 2400Mb/s DDR4 operation in -1 speed grade
- 32-bit and 64-bit bus width support for DDR4, DDR3, DDR3L, or LPDDR3 memories, and 32-bit bus width support for LPDDR4 memory
- ECC support (using extra bits)
- Up to a total DRAM capacity of 32GB

SPI

- Full-duplex operation offers simultaneous receive and transmit
- 128B deep read and write FIFO
- Master or slave SPI mode
- Up to 3 chip select lines
- Multi-master environment
- Identifies an error condition if more than one master detected
- Selectable master clock reference
- Software can poll for status or be interrupt driven

I2C

- 128-bit buffer size
- Both normal (100kHz) and fast bus data rates (400kHz)
- Master or slave mode
- Normal or extended addressing
- I2C bus hold for slow host service

GPIO

- Up to 128 GPIO bits
 - Up to 78-bits from MIO and 96-bits from EMIO
- Each GPIO bit can be dynamically programmed as input or output
- Independent reset values for each bit of all registers
- Interrupt request generation for each GPIO signals
- Single Channel (Bit) write capability for all control registers include data output register, direction control register, and interrupt clear register
- Read back in output mode

CAN

- Conforms to the ISO 11898 -1, CAN2.0A, and CAN 2.0B standards
- Both standard (11-bit identifier) and extended (29-bit identifier) frames
- Bit rates up to 1Mb/s
- Transmit and Receive message FIFO with a depth of 64 messages
- Watermark interrupts for TXFIFO and RXFIFO
- Automatic re-transmission on errors or arbitration loss in normal mode
- Acceptance filtering of 4 acceptance filters

- Sleep Mode with automatic wake-up
- Snoop Mode
- 16-bit timestamping for receive messages
- Both internal generated reference clock and external reference clock input from MIO
- Guarantee clock sampling edge between 80 to 83% at 24MHz reference clock input
- Optional eFUSE disable per port

USB 2.0

- Two USB controllers (configurable as USB 2.0 or USB 3.0)
- Host, device and On-The-Go (OTG) modes
- High Speed, Full Speed, and Low Speed
- Up to 12 endpoints
- 8-bit ULPI External PHY Interface
- The USB host controller registers and data structures are compliant to Intel xHCI specifications.
- 64-bit AXI master port with built-in DMA
- Power management features: hibernation mode

Static Memory Interfaces

The static memory interfaces support external static memories.

- ONFI 3.1 NAND flash support with up to 24-bit ECC
- 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash
- 8-bit eMMC interface supporting managed NAND flash

NAND ONFI 3.1 Flash Controller

- ONFI 3.1 compliant
- Supports chip select reduction per ONFI 3.1 spec
- SLC NAND for boot/configuration and data storage
- ECC options based on SLC NAND
 - 1, 4, or 8 bits per 512+spare bytes
 - 24 bits per 1024+spare bytes
- Maximum throughput as follows
 - Asynchronous mode (SDR) 24.3MB/s
 - Synchronous mode (NV-DDR) 112MB/s (for 100MHz flash clock)
- 8-bit SDR NAND interface

- 2 chip selects
- Programmable access timing
- 1.8V and 3.3V I/O
- Built-in DMA for improved performance

Quad-SPI Controller

- 4 bytes (32-bit) and 3 bytes (24-bit) address width
- Maximum SPI Clock at Master Mode at 150MHz
- Single, Dual-Parallel, and Dual-Stacked mode
- 32-bit AXI Linear Address Mapping Interface for read operation
- Up to 2 chip select signals
- Write Protection Signal
- Hold signals
- 4-bit bidirectional I/O signals
- x1/x2/x4 Read speed required
- x1 write speed required only
- 64 byte Entry FIFO depth to improve QSPI read efficiency
- Built-in DMA for improved performance

Video Encoder/Decoder (VCU)

Zynq UltraScale+ MPSoCs include a Video codec (encoder/decoder) available in the devices designated with the EV suffix. The VCU is located in the PL and can be accessed from either the PL or PS.

- Simultaneous Encode and Decode through separate cores
- H.264 high profile level 5.2 (4Kx2K-60)
- H.265 (HEVC) main, main10 profile, level 5.1, high Tier, up to 4Kx2K-60 rate
- 8 and 10 bit encoding
- 4:2:0 and 4:2:2 chroma sampling
- 8Kx4K-15 rate
- Multi-stream up to total of 4Kx2K-60 rate
- Low Latency mode
- Can share the PS DRAM or use dedicated DRAM in the PL
- Clock/power management
- OpenMax Linux drivers

Table 8: MIO Peripheral Interface Mapping

Peripheral Interface	MIO	EMIO
Quad-SPI NAND	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 78 bits	Yes CAN: External PHY GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: <ul style="list-style-type: none"> Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, <i>or</i> Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

Transceiver (PS-GTR)

The four PS-GTR transceivers, which reside in the full power domain (FPD), support data rates of up to 6.0Gb/s. All the protocols cannot be pinned out at the same time. At any given time, four differential pairs can be pinned out using the transceivers. This is user programmable via the high-speed I/O multiplexer (HS-MIO).

- A Quad transceiver PS-GTR (TX/RX pair) able to support following standards simultaneously
 - x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
 - 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
 - 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
 - 1 or 2 USB3.0 channels at 5.0Gb/s
 - 1-4 Ethernet SGMII channels at 1.25Gb/s
- Provides flexible host-programmable multiplexing function for connecting the transceiver resources to the PS masters (DisplayPort, PCIe, Serial-ATA, USB3.0, and GigE).

HS-MIO

The function of the HS-MIO is to multiplex access from the high-speed PS peripheral to the differential pair on the PS-GTR transceiver as defined in the configuration registers. Up to 4 channels of the transceiver are available for use by the high-speed interfaces in the PS.

Table 9: HS-MIO Peripheral Interface Mapping

Peripheral Interface	Lane0	Lane1	Lane2	Lane3
PCIe (x1, x2 or x4)	PCIe0	PCIe1	PCIe2	PCIe3
SATA (1 or 2 channels)	SATA0	SATA1	SATA0	SATA1
DisplayPort (TX only)	DP1	DP0	DP1	DP0
USB0	USB0	USB0	USB0	–
USB1	–	–	–	USB1
SGMII0	SGMII0	–	–	–
SGMII1	–	SGMII1	–	–
SGMII2	–	–	SGMII2	–
SGMII3	–	–	–	SGMII3

PS-PL Interface

The PS-PL interface includes:

- AMBA AXI4 interfaces for primary data communication
 - Six 128-bit/64-bit/32-bit High Performance (HP) Slave AXI interfaces from PL to PS.
 - Four 128-bit/64-bit/32-bit HP AXI interfaces from PL to PS DDR.
 - Two 128-bit/64-bit/32-bit high-performance coherent (HPC) ports from PL to cache coherent interconnect (CCI).
 - Two 128-bit/64-bit/32-bit HP Master AXI interfaces from PS to PL.
 - One 128-bit/64-bit/32-bit interface from PL to RPU in PS (PL_LPD) for low latency access to OCM.
 - One 128-bit/64-bit/32-bit AXI interface from RPU in PS to PL (LPD_PL) for low latency access to PL.
 - One 128-bit AXI interface (ACP port) for I/O coherent access from PL to Cortex-A53 cache memory. This interface provides coherency in hardware for Cortex-A53 cache memory.
 - One 128-bit AXI interface (ACE Port) for Fully coherent access from PL to Cortex-A53. This interface provides coherency in hardware for Cortex-A53 cache memory and the PL.
- Clocks and resets
 - Four PS clock outputs to the PL with start/stop control.
 - Four PS reset outputs to the PL.

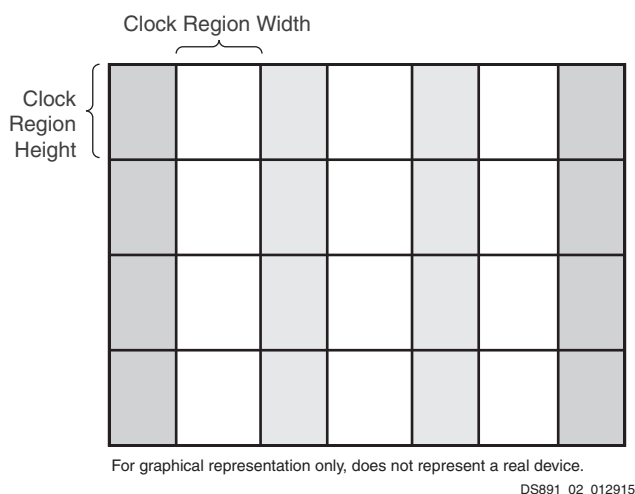


Figure 2: Column-Based Device Divided into Clock Regions

Input/Output

All Zynq UltraScale+ MPSoCs have I/O pins for communicating to external components. In addition, in the MPSoC's PS, there are another 78 I/Os that the I/O peripherals use to communicate to external components, referred to as multiplexed I/O (MIO). If more than 78 pins are required by the I/O peripherals, the I/O pins in the PL can be used to extend the MPSoC interfacing capability, referred to as extended MIO (EMIO).

The number of I/O pins in the PL of Zynq UltraScale+ MPSoCs varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-performance (HP), or high-density (HD). The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V. The HD I/Os are reduced-feature I/Os organized in banks of 24, providing voltage support from 1.2V to 3.3V.

All I/O pins are organized in banks, with 52 HP pins per bank or 24 HD pins per bank. Each bank has one common V_{CCO} output buffer power supply, which also powers certain input buffers. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100 Ω internal resistor. All UltraScale architecture-based devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. The Zynq UltraScale+ family includes support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Ultra-fast serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100 Gb/s and 400 Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Three types of transceivers are used in Zynq UltraScale+ MPSoCs: GTH, GTY, and PS-GTR. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. [Table 10](#) compares the available transceivers.

Table 10: Transceiver Information

	Zynq UltraScale+ MPSoCs		
Type	PS-GTR	GTH	GTY
Qty	4	0–44	0–28
Max. Data Rate	6.0Gb/s	16.3Gb/s	32.75Gb/s
Min. Data Rate	1.25Gb/s	0.5Gb/s	0.5Gb/s
Applications	<ul style="list-style-type: none"> • PCIe Gen2 • USB • Ethernet 	<ul style="list-style-type: none"> • Backplane • PCIe Gen4 • HMC 	<ul style="list-style-type: none"> • 100G+ Optics • Chip-to-Chip • 25G+ Backplane • HMC

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for tough 10G+ and 25G+ backplanes.

Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

Block RAM

Every UltraScale architecture-based device contains a number of 36Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale architecture-based devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27×18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ devices is similar to the Kintex UltraScale and Virtex UltraScale devices but with the addition of a PMBus interface.

Zynq UltraScale+ MPSoCs contain one System Monitor in the PL and an additional block in the PS. The System Monitor in the PL has the same features as the block in UltraScale+ FPGAs. See [Table 11](#).

Table 11: Key System Monitor Features

	Zynq UltraScale+ MPSoC PL	Zynq UltraScale+ MPSoC PS
ADC	10-bit 200KSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP, PMBus	APB

Clock Management

The PS in Zynq UltraScale+ MPSoCs is equipped with five phase-locked loops (PLLs), providing flexibility in configuring the clock domains within the PS. There are four primary clock domains of interest within the PS. These include the APU, the RPU, the DDR controller, and the I/O peripherals (IOP). The frequencies of all of these domains can be configured independently under software control.

Power Domains

The Zynq UltraScale+ MPSoC contains four separate power domains. When they are connected to separate power supplies, they can be completely powered down independently of each other without consuming any dynamic or static power. The processing system includes:

- Full Power Domain (FPD)
- Low Power Domain (LPD)
- Battery Powered Domain (BPD)

In addition to these three Processing System power domains, the PL can also be completely powered down if connected to separate power supplies.

The Full Power Domain (FPD) consists of the following major blocks:

- Application Processing Unit (APU)
- DMA (FP-DMA)
- Graphics Processing Unit (GPU)
- Dynamic Memory Controller (DDRC)
- High-Speed I/O Peripherals

The Low Power Domain (LPD) consists of the following major blocks:

- Real-Time Processing Unit (RPU)
- DMA (LP-DMA)
- Platform Management Unit (PMU)
- Configuration Security Unit (CSU)
- Low-Speed I/O Peripherals
- Static Memory Interfaces

The Battery Power Domain (BPD) is the lowest power domain of the Zynq UltraScale+ MPSoC processing system. In this mode, all the PS is powered off except the Real-Time Clock (RTC) and battery-backed RAM (BBRAM).

Power Examples

Power for the Zynq UltraScale+ MPSoCs varies depending on the utilization of the PL resources, and the frequency of the PS and PL. To estimate power, use the Xilinx Power Estimator (XPE) at:

http://www.xilinx.com/products/design_tools/logic_design/xpe.htm

PS Boot and Device Configuration

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decrypts and authenticates the images while the 4096-bit RSA block authenticates the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. The CSU executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the OCM.

After copying the FSBL to OCM, one of the processors, either the Cortex-A53 or Cortex-R5, executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL), such as U-Boot. Users obtain example SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, eMMC, or Quad-SPI) is configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or callable after boot.

Hardware and Software Debug Support

The debug system used in Zynq UltraScale+ MPSoCs is based on the ARM CoreSight architecture. It uses ARM CoreSight components including an embedded trace controller (ETC), an embedded trace Macrocell (ETM) for each Cortex-A53 and Cortex-R5 processor, and a system trace Macrocell (STM). This enables advanced debug features like event trace, debug breakpoints and triggers, cross-trigger, and debug bus dump to memory. The programmable logic can be debugged with the Xilinx Vivado Logic Analyzer.

Debug Ports

Three JTAG ports are available and can be chained together or used separately. When chained together, a single port is used for chip-level JTAG functions, ARM processor code downloads and run-time control operations, PL configuration, and PL debug with the Vivado Logic Analyzer. This enables tools such as the Xilinx Software Development Kit (SDK) and Vivado Logic Analyzer to share a single download cable from Xilinx.

When the JTAG chain is split, one port is used to directly access the ARM DAP interface. This CoreSight interface enables the use of ARM-compliant debug and software development tools such as Development Studio 5 (DS-5™). The other JTAG port can then be used by the Xilinx FPGA tools for access to the PL, including configuration bitstream downloads and PL debug with the Vivado Logic Analyzer. In this mode, users can download to and debug the PL in the same manner as a stand-alone FPGA.