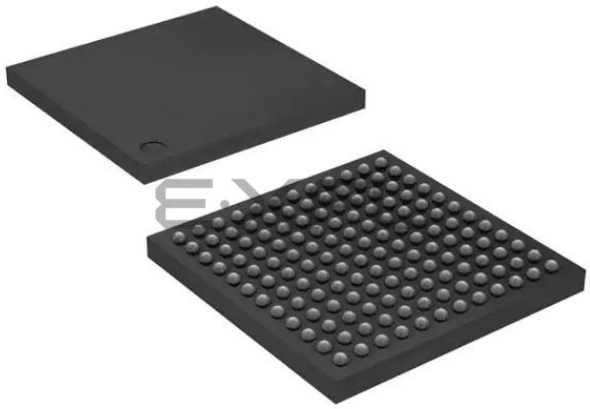

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	240MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	AC'97, POR, PWM, WDT
Number of I/O	49
Program Memory Size	32KB (32K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9r64-cu-999

Table 1-1. Unavailable or Partially Available Features and Signals in AT91SAM9R64

Feature	Full/Partial	Signal	Peripheral A	Peripheral B
PWM	Partial	PWM2	PD5 and PD12	-
SPI	Partial	NPCS2 NPCS3	PD8	 PD9 and PD13
SSC1	Full	RF1 RK1 TD1 RD1 TK1 TF1	-	PA8 PA9 PA13 PA14 PA29 PA30
Touchscreen ADC	Partial	AD3YM GPAD4 GPAD5	PA20 PD6 PD7	-
TC	Partial	TIOA1 TIOB1 TCLK1 TIOA2 TIOB2	-	PC29 PC30 PC31 PD10 PD11
TWI	Full	TWD1 TWCK1	PD10 PD11	-
USART0	Partial	SCK0 RTS0 CTS0 DSR0 DTR0 DCD0 RI0	PA8 PA9 PA10 PD14 PD15 PD16 PD17	-
USART1	Partial	SCK1	-	PD2
USART2	Partial	SCK2 RTS2 CTS2	PD9 PA29 PA30	-
USART3	Partial	SCK3 RTS3 CTS3	-	PA20 PD3 PD4

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
USB High Speed Device				
DFSDM	USB Device Full Speed Data -	Analog		
DFSDP	USB Device Full Speed Data +	Analog		
DHSDM	USB Device High Speed Data -	Analog		
DHSDP	USB Device High Speed Data +	Analog		

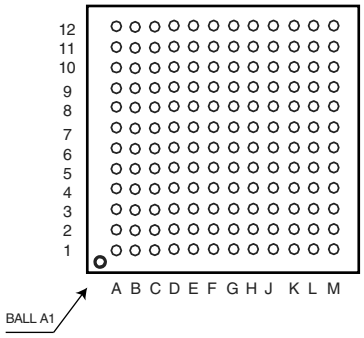
4. Package and Pinout

The AT91SAM9R64 is available in a 144-ball BGA package. The AT91SAM9RL64 is available in a 217-ball LFBGA package.

4.1 144-ball BGA Package Outline

Figure 4-1 shows the orientation of the 144-ball BGA package.

Figure 4-1. 144-ball BGA Pinout (Top View)



4.2 Pinout

Table 4-1. AT91SAM9R64 Pinout for 144-ball BGA Package

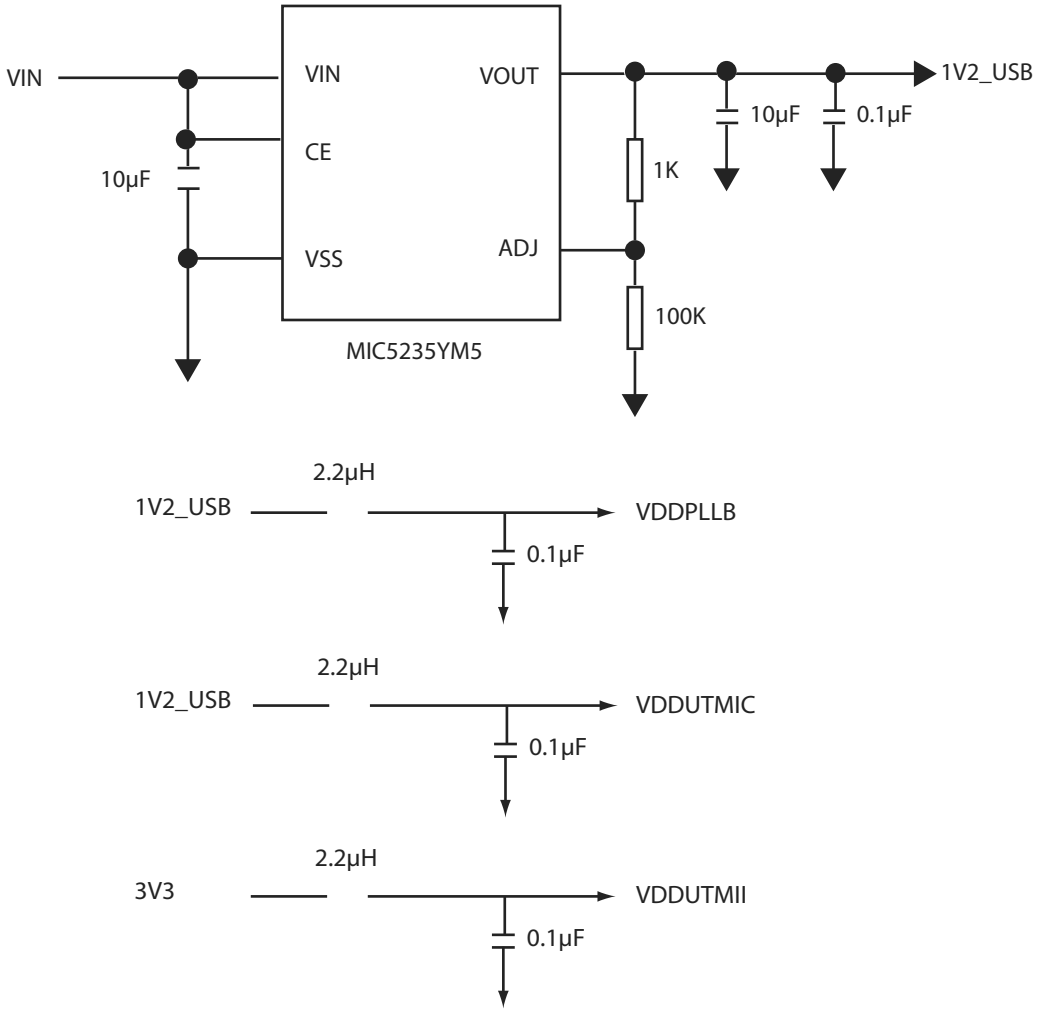
Pin	Signal Name
A1	DFSDM
A2	DHSDM
A3	XIN
A4	XOUT
A5	XIN32
A6	XOUT32
A7	TDO
A8	PA[31]
A9	PA[22]
A10	PA[16]
A11	PA[14]
A12	PA[11]
B1	DFSDP
B2	DHSDP
B3	NC
B4	VDDPLLB
B5	GNDPLLB
B6	TMS
B7	RTCK
B8	PA[27]
B9	PA[21]
B10	PA[12]
B11	PD[21]
B12	PA[10]
C1	VDDPLLA
C2	VBG
C3	VDDBU
C4	SHDN
C5	WKUP
C6	NTRST
C7	TDI
C8	PA[28]
C9	PA[23]
C10	PA[7]
C11	PD[19]
C12	PD[18]

Pin	Signal Name
D1	PLLRCA
D2	VDDUTMII
D3	NWR3/NBS3/CFIOW
D4	NWR1/NBS1/CFIOR
D5	JTAGSEL
D6	GNDBU
D7	TCK
D8	PA[26]
D9	PA[24]
D10	PA[13]
D11	PA[6]
D12	PD[20]
E1	GNDPLLA
E2	NWR0/NWE/CFWE
E3	NRD/CFOE
E4	NCS0
E5	NCS1/SDCS
E6	PB[2]
E7	NRST
E8	BMS
E9	PA[25]
E10	PA[15]
E11	PA[5]
E12	PA[4]
F1	PB[5]
F2	PB[6]
F3	PB[7]
F4	PB[8]
F5	PB[3]
F6	PB[4]
F7	TST
F8	VDDUTMIC
F9	PA[3]
F10	PA[2]
F11	PA[0]
F12	PA[1]

Pin	Signal Name
G1	PB[10]
G2	PB[11]
G3	PB[12]
G4	PB[9]
G5	PB[13]
G6	GND
G7	GND
G8	GND
G9	GNDUTMI
G10	VDDCORE
G11	VDDIOP
G12	VDDIOP
H1	PB[14]
H2	PB[15]
H3	A[0]
H4	A[2]
H5	SDA10
H6	D[1]
H7	GND
H8	GND
H9	VDDIOM
H10	SDCKE
H11	VDDCORE
H12	VDDIOP
J1	A[4]
J2	A[1]
J3	A[3]
J4	A[14]
J5	CAS
J6	D[2]
J7	D[5]
J8	D[12]
J9	D[14]
J10	VDDIOM
J11	D[10]
J12	D[9]

Pin	Signal Name
K1	A[5]
K2	A[6]
K3	A[13]
K4	A[15]
K5	RAS
K6	D[3]
K7	D[6]
K8	D[13]
K9	VDDIOM
K10	VDDIOM
K11	D[11]
K12	PB[1]
L1	A[7]
L2	A[8]
L3	A[11]
L4	A[16]
L5	SDWE
L6	D[4]
L7	D[7]
L8	D[15]
L9	PC[1]
L10	PC[0]
L11	PB[0]
L12	GNDANA
M1	A[9]
M2	A[10]
M3	A[12]
M4	A[17]
M5	D[0]
M6	SDCK
M7	D[8]
M8	ADVREF
M9	VDDANA
M10	PA[17]
M11	PA[18]
M12	PA[19]

Figure 5-1. Example of PLL and USB Power Supplies



5.2 Programmable I/O Lines Power Supplies

The power supplies pins VDDIOM support two voltage ranges. This allows the device to reach its maximum speed either out of 1.8V or 3.3V external memories.

The maximum speed is MCK on the pin SDCK (SDRAM Clock) loaded with 30pF for power supply at 1.8V and 50 pF for power supply at 3.3V.

The maximum speed on the other signals of the External Bus Interface (control, address and data signals) is 50 MHz.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal and power supply pins can accept either 1.8V or 3.3V. The user must make sure to program the EBI voltage range before getting the device out of its Slow Clock Mode.

The PIO lines are supplied through VDDIOP and the speed of the signal that can be driven on them can reach 50 MHz with 50 pF load.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs and have no pull-up resistors.

TDO is an output, driven at up to VDDIOP, and have no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

All the JTAG signals are supplied with VDDIOP except JTAGSEL supplied by VDDBU.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP.

As the product integrates power-on reset cells, which manages the processor and the JTAG reset, the NRST and NTRST pin can be left unconnected.

The NRST and NTRST pins integrates a permanent pull-up resistor of 100 kΩ typical to VDDIOP.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines which are managed by the PIO Controllers integrate a programmable pull-up resistor. Refer to the section “AT91SAM9R64/RL64 Electrical Characteristics” in the product datasheet for more details.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables.

6.5 Shutdown Logic Pins

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets

  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 4-Kbyte Data Cache, 4-Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Matrix Masters

The Bus Matrix of the AT91SAM9R64/RL64 product manages 6 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	DMA Controller
Master 1	USB Device High Speed DMA
Master 2	LCD Controller DMA

Table 7-1. List of Bus Matrix Masters

Master 3	Peripheral DMA Controller
Master 4	ARM926™ Instruction
Master 5	ARM926 Data

7.3 Matrix Slaves

The Bus Matrix of the AT91SAM9R64/RL64 product manages 6 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal ROM
Slave 1	Internal SRAM
Slave 2	LCD Controller User Interface
Slave 3	UDP High Speed RAM
Slave 4	External Bus Interface (EBI)
Slave 5	Peripheral Bridge

7.4 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the USB Device High speed DMA to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown as "-" in the following table.

Table 7-3. AT91SAM9R64/RL64 Master to Slave Access

Masters		0	1	2	3	4	5
Slaves		DMA Controller	USB HS Device DMA	LCD Controller DMA	Peripheral DMA	ARM926 Instruction	ARM926 Data
0	Internal ROM	X	X		X	X	X
1	Internal SRAM	X	X	X	X	X	X
2	LCD Controller User Interface	-	-	-	-	X	X
3	UDP High Speed RAM	-	-	-	-	X	X
4	External Bus Interface	X	X	X	X	X	X
5	Peripheral Bridge	X	X	X	-	-	-

7.5 Peripheral DMA Controller (PDC)

- Acting as one AHB Bus Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer support, prevents strong real-time constraints on buffer management.

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

a. TWI0 Transmit Channel
b. DBGU Transmit Channel
c. USART3 Transmit Channel
d. USART2 Transmit Channel
e. USART1 Transmit Channel
f. USART0 Transmit Channel
g. AC97 Transmit Channel
h. SPI Transmit Channel
i. SSC1 Transmit Channel
j. SSC0 Transmit Channel
k. TWI0 Receive Channel
l. DBGU Receive Channel
m. ADC Receive Channel
n. USART3 Receive Channel
o. USART2 Receive Channel
p. USART1 Receive Channel
q. USART0 Receive Channel
r. AC97 Receive Channel
s. SPI Receive Channel
t. SSC1 Receive Channel
u. SSC0 Transmit Channel
v. MCI Receive/Transmit Channel

7.6 DMA Controller

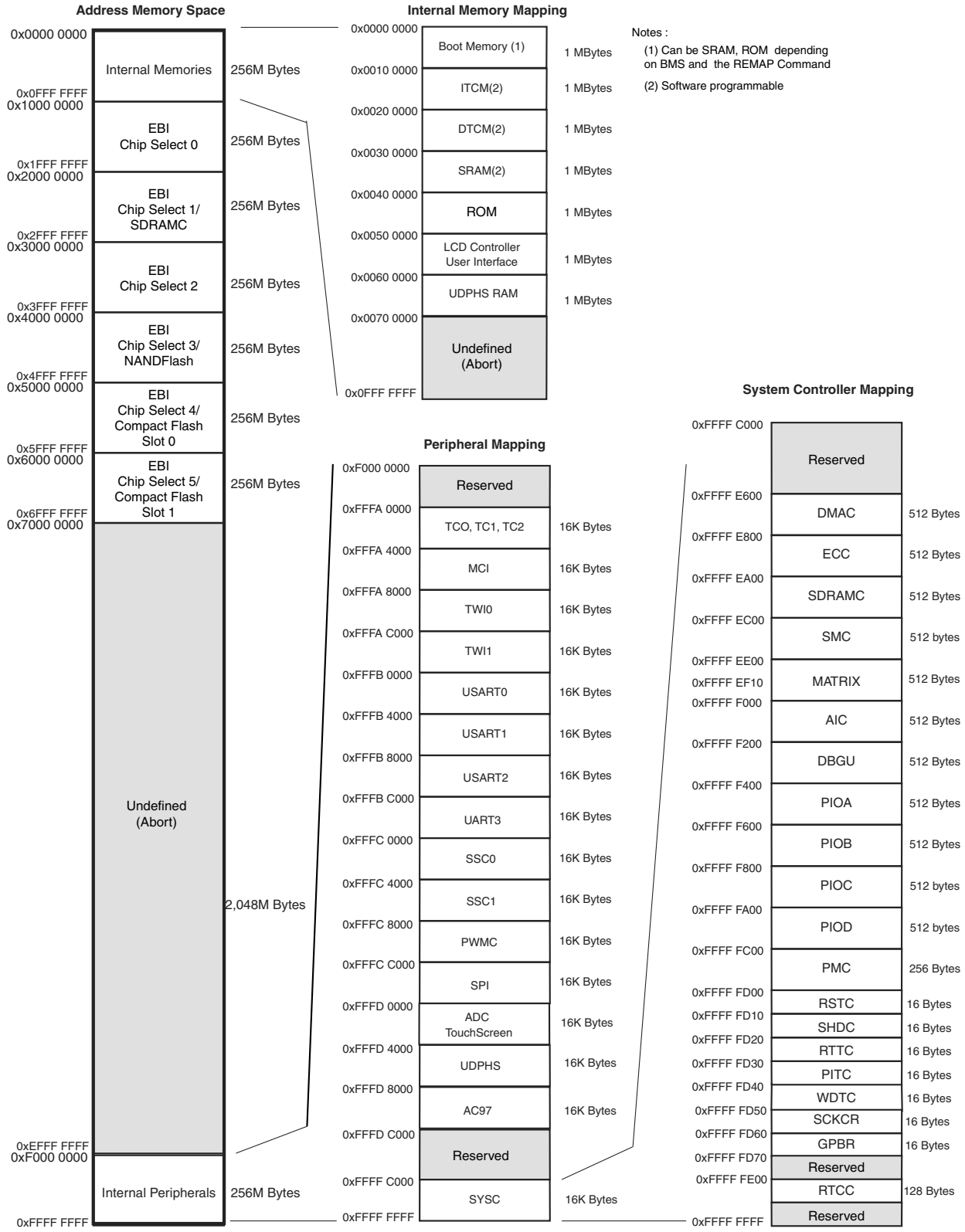
- Acting as one Matrix Master
- Embeds 2 channels
- 16 bytes/FIFO for Channel Buffering
- Linked List support with Status Write Back operation at End of Transfer
- Word, Half-word, Byte transfer support

7.7 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

8. Memories

Figure 8-1. AT91SAM9R64/RL64 Memory Mapping



- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0020 0000.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64Kbyte SRAM size available, the amount of memory assigned to each block is software programmable as a multiple of 16K Bytes according to Table 8-2. This Table provides the size of the Internal SRAM C according to the size of the Internal SRAM A and the Internal SRAM B.

Table 8-2. Internal SRAM Block Size

Remaining Internal SRAM C		Internal SRAM A (ITCM) Size		
		0	16K Bytes	32K Bytes
Internal SRAM B (DTCM) size	0	64K Bytes	48K Bytes	32K Bytes
	16K Bytes	48K Bytes	32K Bytes	16K Bytes
	32K Bytes	32K Bytes	16K Bytes	0K Bytes

At reset, the whole memory is assigned to Internal SRAM C.

The memory blocks assigned to SRAM A, SRAM B and SRAM C areas are not contiguous and when the user dynamically changes the Internal SRAM configuration, the new 16-Kbyte block organization may affect the previous configuration from a software point of view.

Table 8-3 illustrates different configurations and the related 16-Kbyte blocks (RB0 to RB3) assignments.

Table 8-3. 16-Kbyte Block Allocation example

Decoded Area	Address	Configuration examples and related 16-Kbyte block assignments								
		I = 0K D = 0K A = 64K(1)	I = 16K D = 0K A = 48K	I =32K D = 0K A = 32K	I = 0K D = 16K A = 48K	I = 16K D = 16K A = 32K	I = 32K D = 16K A = 16K	I = 0K D = 32K A = 32K	I = 16K D = 32K A = 16K	I = 32K D = 32K A = 0K
Internal SRAM A (ITCM)	0x0010 0000		RB1	RB1		RB1	RB1		RB1	RB1
	0x0010 4000			RB0			RB0			RB0
Internal SRAM B (DTCM)	0x0020 0000				RB3	RB3	RB3	RB3	RB3	RB3
	0x0020 4000							RB2	RB2	RB2
Internal SRAM C (AHB)	0x0030 0000	RB3	RB3	RB3	RB2	RB2	RB2	RB1	RB0	
	0x0030 4000	RB2	RB2	RB2	RB1	RB0		RB0		
	0x0030 8000	RB1	RB0		RB0					
	0x0030 C000	RB0								

Note: 1. Configuration after reset.

When accessed from the AHB, the internal Fast SRAM is single cycle accessible at full matrix speed (MCK). When accessed from the processor's TCM Interface, they are also single cycle accessible at full processor speed.

8.1.1.2 Internal ROM

The AT91SAM9R64/RL64 embeds an Internal ROM, which contains the SAM-BA program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

8.1.2 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0 to ease the development. This is done by software once the system has boot. Refer to the Bus Matrix Section for more details.

When REMAP = 0 BMS allows the user to lay out to 0x0, at his convenience, the ROM or an external memory. This is done by a hardware way at reset.

Note: All the memory blocks can always be seen at their specified base addresses that are not concerned by these parameters.

The AT91SAM9R64/RL64 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

8.1.2.1 BMS = 1, boot on embedded ROM

The system boots on Boot Program.

- Boot on on-chip RC
- Enable the 32768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SDCard (boot ROM does not support high-capacity SDCards)
  - NAND Flash
  - SPI DataFlash® connected on NPCS0 of the SPI0
- SAM-BA Boot in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device HS Port

8.1.2.2 BMS = 0, boot on external memory

- Boot on on-chip RC

8.2.3 SDRAM Controller

- Supported devices:
  - Standard and Low Power SDRAM (Mobile SDRAM)
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with two or four Internal Banks
  - SDRAM with 16- or 32-bit Data Path
- Programming facilities
  - Word, half-word, byte access
  - Automatic page break when Memory Boundary has been reached
  - Multibank Ping-pong Access
  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
- Energy-saving capabilities
  - Self-refresh, power down and deep power down modes supported
- Error detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- SDRAM CAS Latency of 1, 2 and 3 supported
- Auto Precharge Command not used

8.2.4 NAND Flash Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by trigging on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-bytes pages

9. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface embeds also the registers allowing to configure the Matrix and a set of registers configuring the EBI chip select assignment and the voltage range for external memories.

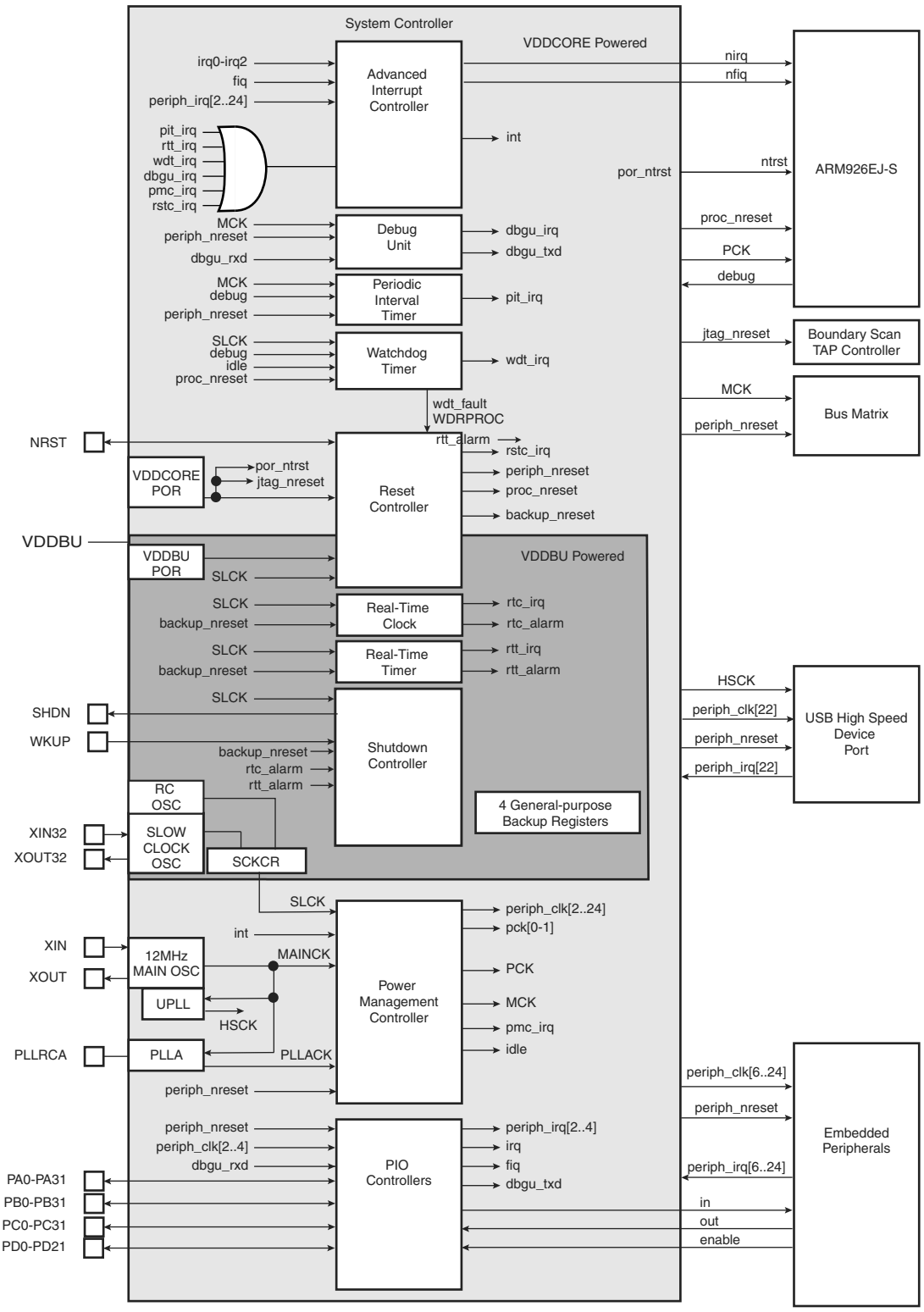
9.1 System Controller Mapping

As shown in Figure 8-1, the System Controller's peripherals are all mapped within the highest 16K bytes of the 4 Gbyte address space, between addresses 0xFFFF C000 and 0xFFFF FFFF.

However, all the registers of System Controller are mapped on the top of the address space. This allows addressing all the registers of the System Controller from a single pointer by using the standard ARM instruction set, as the Load/Store instruction have an indexing mode of +/- 4kbytes.

9.2 Block Diagram

Figure 9-1. System Controller Block Diagram



10.3 Peripheral Interrupts and Clock Control

10.3.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the SDRAM Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-time Timer
- the Real-time Clock
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

10.3.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signal IRQ, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

10.4 Peripherals Signals Multiplexing on I/O Lines

The AT91SAM9R64/RL64 features 4 PIO controllers, PIOA, PIOB, PIOC and PIOD, which multiplexes the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns “Function” and “Comments” have been inserted in this table for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the both tables.

The column “Reset State” indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O is mentioned, the PIO Line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case for pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

The AT91SAM9RL64 and AT91SAM9R64 do not have the same peripheral signal multiplexing, each one follows.

10.4.1.3 AT91SAM9RL64 PIO Controller C Multiplexing

Table 10-4. AT91SAM9RL64 Multiplexing on PIO Controller C

PIO Controller C					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PC0	TF0		I/O	VDDIOP		
PC1	TK0	LCDPWR	I/O	VDDIOP		
PC2	LCDMOD	PWM0	I/O	VDDIOP		
PC3	LCDCC	PWM1	I/O	VDDIOP		
PC4	LCDVSYNC		I/O	VDDIOP		
PC5	LCDHSYNC		I/O	VDDIOP		
PC6	LCDDOTCK		I/O	VDDIOP		
PC7	LCDDEN		I/O	VDDIOP		
PC8	LCDD0	LCDD2	I/O	VDDIOP		
PC9	LCDD1	LCDD3	I/O	VDDIOP		
PC10	LCDD2	LCDD4	I/O	VDDIOP		
PC11	LCDD3	LCDD5	I/O	VDDIOP		
PC12	LCDD4	LCDD6	I/O	VDDIOP		
PC13	LCDD5	LCDD7	I/O	VDDIOP		
PC14	LCDD6	LCDD10	I/O	VDDIOP		
PC15	LCDD7	LCDD11	I/O	VDDIOP		
PC16	LCDD8	LCDD12	I/O	VDDIOP		
PC17	LCDD9	LCDD13	I/O	VDDIOP		
PC18	LCDD10	LCDD14	I/O	VDDIOP		
PC19	LCDD11	LCDD15	I/O	VDDIOP		
PC20	LCDD12	LCDD18	I/O	VDDIOP		
PC21	LCDD13	LCDD19	I/O	VDDIOP		
PC22	LCDD14	LCDD20	I/O	VDDIOP		
PC23	LCDD15	LCDD21	I/O	VDDIOP		
PC24	LCDD16	LCDD22	I/O	VDDIOP		
PC25	LCDD17	LCDD23	I/O	VDDIOP		
PC26	LCDD18		I/O	VDDIOP		
PC27	LCDD19		I/O	VDDIOP		
PC28	LCDD20		I/O	VDDIOP		
PC29	LCDD21	TIOA1	I/O	VDDIOP		
PC30	LCDD22	TIOB1	I/O	VDDIOP		
PC31	LCDD23	TCLK1	I/O	VDDIOP		

10.4.2 AT91SAM9R64 PIO Multiplexing

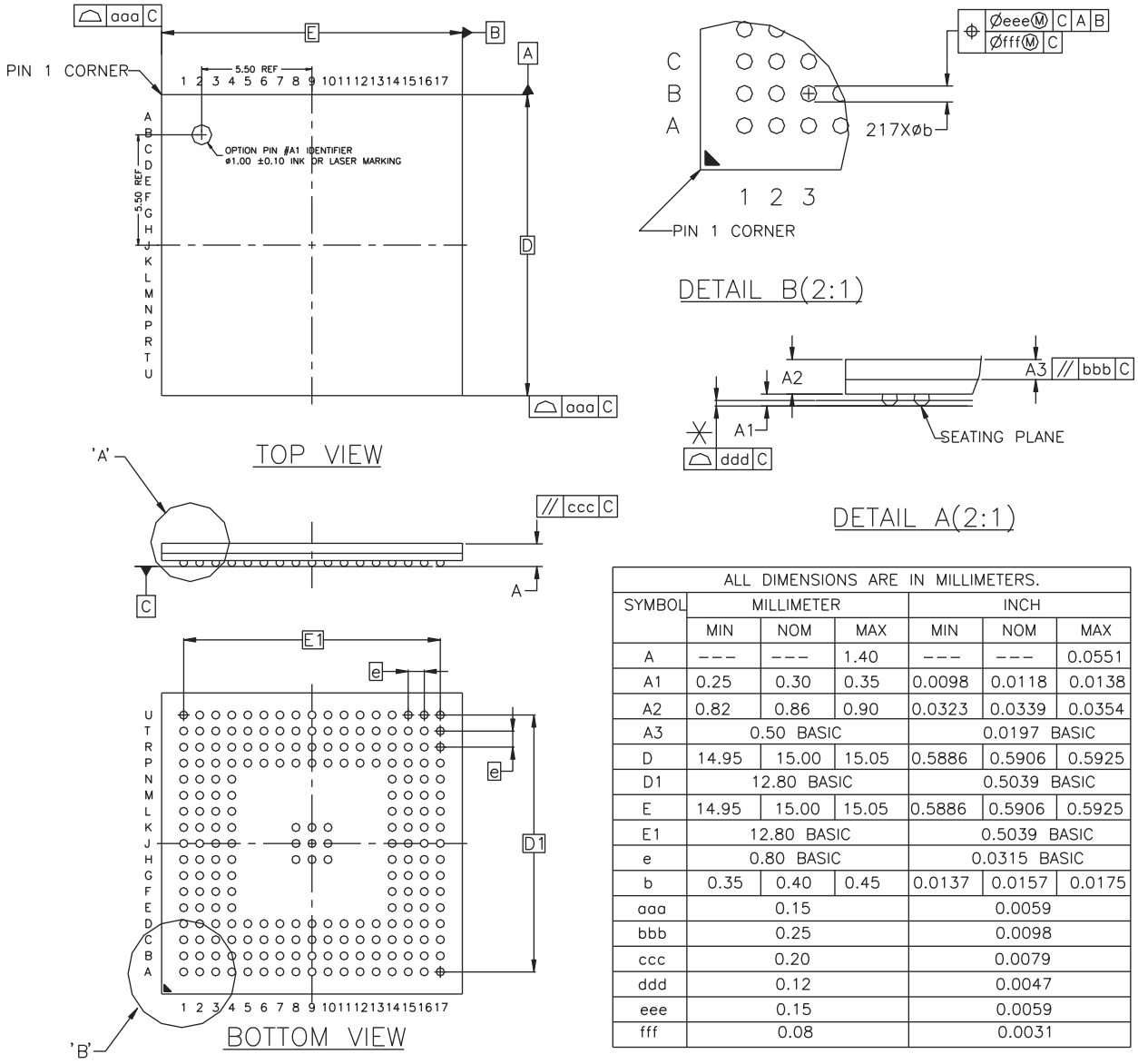
Note: In Table 10-6, Table 10-7, Table 10-8 and Table 10-9, shaded cells indicate I/O lines that are NOT available on the AT91SAM9R64.

10.4.2.1 AT91SAM9R64 PIO Controller A Multiplexing

Table 10-6. AT91SAM9R64 Multiplexing on PIO Controller A

PIO Controller A					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PA0	MC_DA0		I/O	VDDIOP		
PA1	MC_CDA		I/O	VDDIOP		
PA2	MC_CK		I/O	VDDIOP		
PA3	MC_DA1	TCLK0	I/O	VDDIOP		
PA4	MC_DA2	TIOA0	I/O	VDDIOP		
PA5	MC_DA3	TIOB0	I/O	VDDIOP		
PA6	TXD0		I/O	VDDIOP		
PA7	RXD0		I/O	VDDIOP		
PA8	NA	NA				Reserved
PA9	NA	NA				Reserved
PA10	CTS0	RK0	I/O	VDDIOP		
PA11	TXD1		I/O	VDDIOP		
PA12	RXD1		I/O	VDDIOP		
PA13	TXD2		I/O	VDDIOP		
PA14	RXD2		I/O	VDDIOP		
PA15	TD0		I/O	VDDIOP		
PA16	RD0		I/O	VDDIOP		
PA17	AD0		I/O	VDDIOP		
PA18	AD1	RTS1	I/O	VDDIOP		
PA19	AD2	CTS1	I/O	VDDIOP		
PA20	NA	NA				Reserved
PA21	DRXD		I/O	VDDIOP		
PA22	DTXD	RF0	I/O	VDDIOP		
PA23	TWD0		I/O	VDDIOP		
PA24	TWCK0		I/O	VDDIOP		
PA25	MISO		I/O	VDDIOP		
PA26	MOSI		I/O	VDDIOP		
PA27	SPCK		I/O	VDDIOP		
PA28	NPCS0		I/O	VDDIOP		
PA29	NA	NA				Reserved
PA30	NA	NA				Reserved
PA31	NWAIT	IRQ	I/O	VDDIOP		

Figure 12-2. 217-ball LFBGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.82	0.86	0.90	0.0323	0.0339	0.0354
A3	0.50 BASIC			0.0197 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5925
D1	12.80 BASIC			0.5039 BASIC		
E	14.95	15.00	15.05	0.5886	0.5906	0.5925
E1	12.80 BASIC			0.5039 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0137	0.0157	0.0175
aaa	0.15			0.0059		
bbb	0.25			0.0098		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

14. Revision History

Doc. Rev	Comments	Change Request Ref.
6289CS	**Product Overview:** "Features" on page 1, removed mid-level Embedded Trace Macrocell feature "Features" on page 1, updated figures on CPU speed "Features" on page 1, updated SDIO and MMC version Removed paragraph Section 5.2 "Power Consumption". Section 6.5 "Shutdown Logic Pins", removed information on the shutdown pin Section 8.1.2.1 "BMS = 1, boot on embedded ROM", – SDCard, (boot ROM does not support high capacity SDCards) clarification added.	 6142 RFO 6345 6345 6345 5935
6289BS	"Features" "Debug Unit (DBGU)" on page 2, updated Figure 8-1 "AT91SAM9R64/RL64 Memory Mapping", Internal Memory Mapping updated. Table 7-2, "List of Bus Matrix Slaves", Table 7-3, "AT91SAM9R64/RL64 Master to Slave Access", Slave 3 updated. Section 5.1 "Power Supplies", updated with caution on VDDCORE and VDDIO constraints Section 5.1.1 "USB Power Supply Considerations" and Figure 5-1 added to datasheet. Section 5.2 "Power Consumption", first two sentences updated. Table 3-1, "Signal Description List", additional comments on BMS. SHDN comments updated. Table 10-3 and Table 10-7 PB8, PB9 Peripheral A column: typos corrected, "CFCE1", "CFCE2".	5846 5276 5291 5420 5388 5423 rfo 5788
6289AS	First issue	