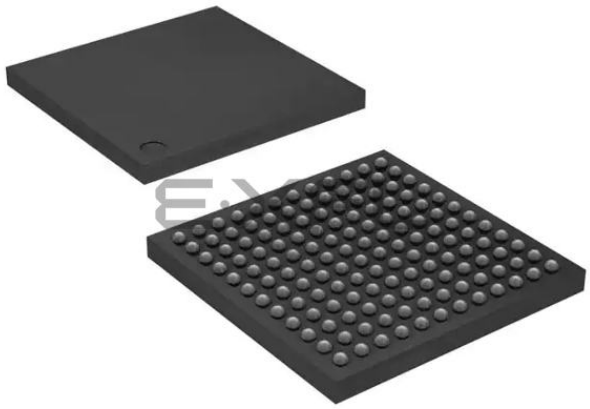

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	240MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	AC'97, POR, PWM, WDT
Number of I/O	49
Program Memory Size	32KB (32K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9r64-cu

Table 1-1. Unavailable or Partially Available Features and Signals in AT91SAM9R64

Feature	Full/Partial	Signal	Peripheral A	Peripheral B
PWM	Partial	PWM2	PD5 and PD12	-
SPI	Partial	NPCS2 NPCS3	PD8	 PD9 and PD13
SSC1	Full	RF1 RK1 TD1 RD1 TK1 TF1	-	PA8 PA9 PA13 PA14 PA29 PA30
Touchscreen ADC	Partial	AD3YM GPAD4 GPAD5	PA20 PD6 PD7	-
TC	Partial	TIOA1 TIOB1 TCLK1 TIOA2 TIOB2	-	PC29 PC30 PC31 PD10 PD11
TWI	Full	TWD1 TWCK1	PD10 PD11	-
USART0	Partial	SCK0 RTS0 CTS0 DSR0 DTR0 DCD0 RI0	PA8 PA9 PA10 PD14 PD15 PD16 PD17	-
USART1	Partial	SCK1	-	PD2
USART2	Partial	SCK2 RTS2 CTS2	PD9 PA29 PA30	-
USART3	Partial	SCK3 RTS3 CTS3	-	PA20 PD3 PD4

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
NTRST	Test Reset Signal	Input	Low	Pull-up resistor.
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor
BMS	Boot Mode Select	Input		Must be connected to GND or VDDIOP. No pullup resistor BMS = 0 when tied to GND BMS = 1 when tied to VDDIOP
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
Advanced Interrupt Controller - AIC				
IRQ	External Interrupt Input	Input		
FIQ	Fast Interrupt Input	Input		
PIO Controller - PIOA - PIOB - PIOC-PIOD				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD21	Parallel IO Controller D	I/O		Pulled-up input at reset
External Bus Interface - EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset. D16-D31 not present on AT91SAM9R64.
A0 - A25	Address Bus	Output		0 at reset
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
NCS0 - NCS5	Chip Select Lines	Output	Low	NCS2, NCS5 not present on AT91SAM9R64.
NWR0 - NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	CFCS1 not present on AT91SAM9R64.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
NAND Flash Support				
NANDCS	NAND Flash Chip Select	Output	Low	
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Multimedia Card Interface MCI				
CK	Multimedia Card Clock	I/O		
CDA	Multimedia Card Slot A Command	I/O		
DA0 - DA3	Multimedia Card Slot A Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter USARTx				
SCKx	USARTx Serial Clock	I/O		SCKx not present on AT91SAM9R64.
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		RTS0, RTS2, RTS3 not present on AT91SAM9R64.
CTSx	USARTx Clear To Send	Input		CTS0, CTS2, CTS3 not present on AT91SAM9R64.
DTR0	USART0 Data Terminal Ready	I/O		Not present on AT91SAM9R64.
DSR0	USART0 Data Set Ready	Input		Not present on AT91SAM9R64.
DCD0	USART0 Data Carrier Detect	Output		Not present on AT91SAM9R64.
RI0	USART0 Ring Indicator	Input		Not present on AT91SAM9R64.
Synchronous Serial Controller - SSCx				
TD0 - TD1	SSC Transmit Data	Output		TD1 not present on AT91SAM9R64.
RD0 - RD1	SSC Receive Data	Input		RD1 not present on AT91SAM9R64.
TK0 - TK1	SSC Transmit Clock	I/O		TK1 not present on AT91SAM9R64.
RK0 - RK1	SSC Receive Clock	I/O		RK1 not present on AT91SAM9R64.
TF0 - TF1	SSC Transmit Frame Sync	I/O		TF1 not present on AT91SAM9R64.
RF0 - RF1	SSC Receive Frame Sync	I/O		RF1 not present on AT91SAM9R64.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
USB High Speed Device				
DFSDM	USB Device Full Speed Data -	Analog		
DFSDP	USB Device Full Speed Data +	Analog		
DHSDM	USB Device High Speed Data -	Analog		
DHSDP	USB Device High Speed Data +	Analog		

4.4 Pinout

Table 4-2. AT91SAM9RL64 Pinout for 217-ball LFBGA Package [1]

Pin	Signal Name
A1	DFSDM
A2	DHSDP
A3	VDDPLLB
A4	XIN
A5	XOUT
A6	GNDPLLB
A7	XOUT32
A8	GND
A9	NRST
A10	RTCK
A11	PA[29]
A12	PA[26]
A13	PA[22]
A14	PA[14]
A15	PA[10]
A16	PD[20]
A17	PD[17]
B1	DFSDP
B2	DHSDM
B3	VBG
B4	NC
B5	NC
B6	XIN32
B7	TST
B8	GND
B9	TMS
B10	VDDCORE
B11	PA[28]
B12	PA[25]
B13	PA[21]
B14	PA[13]
B15	PD[21]
B16	PD[19]
B17	PA[9]
C1	VDDPLLA
C2	VDDUTMII
C3	GND
C4	GNDUTMI
C5	VDDBU
C6	WKUP
C7	GNDBU
C8	TCK
C9	TDI
C10	PA[31]
C11	PA[27]
C12	PA[24]
C13	PA[16]
C14	PA[11]
C15	PD[18]
C16	PA[7]
C17	PA[6]
D1	PLLRCA
D2	NWR1/NBS1/CFIOR
D3	GND
D4	GND
D5	SHDN
D6	JTAGSEL
D7	NTRST
D8	BMS
D9	TDO
D10	PA[30]
D11	GND
D12	PA[23]
D13	PA[15]
D14	PA[12]
D15	PA[8]
D16	PD[13]
D17	PD[16]
E1	GNDPLLA
E2	NCS1/SDCS
E3	NCS0
E4	NWR3/NBS3/CFIOW
E14	PD[15]
E15	PD[14]
E16	PA[5]
E17	PA[4]
F1	NRD/CFOE
F2	PB[2]
F3	NWR0/NWE/CFWE
F4	PB[3]
F14	PA[1]
F15	PA[0]
F16	PA[2]
F17	PA[3]
G1	GND
G2	VDDIOM
G3	PB[5]
G4	PB[4]
G14	PD[12]
G15	PD[11]
G16	PD[10]
G17	PD[9]
H1	PB[8]
H2	PB[9]
H3	PB[7]
H4	PB[6]
H8	VDDCORE
H9	VDDIOP
H10	PD[4]
H14	PD[8]
H15	PD[5]
H16	PD[2]
H17	PD[3]
J1	PB[12]
J2	PB[13]
J3	PB[11]
J4	PB[10]
J8	VDDCORE
J9	VDDIOP
J10	PC[29]
J14	PD[1]
J15	PD[0]
J16	PC[30]
J17	PC[31]
K1	PB[14]
K2	PB[15]
K3	PB[17]
K4	PB[16]
K8	VDDUTMIC
K9	VDDIOP
K10	PC[28]
K14	PC[25]
K15	PC[24]
K16	PC[26]
K17	PC[27]
L1	PB[18]
L2	PB[19]
L3	PB[21]
L4	PB[20]
L14	PC[21]
L15	PC[20]
L16	PC[22]
L17	PC[23]
M1	PB[22]
M2	PB[23]
M3	PB[25]
M4	PB[24]
M14	PC[17]
M15	PC[16]
M16	PC[18]
M17	PC[19]
N1	PB[26]
N2	PB[27]
N3	PB[29]
N4	PB[28]
N14	PC[13]
N15	PC[12]
N16	PC[14]
N17	PC[15]
P1	PB[30]
P2	PB[31]
P3	A[1]
P4	A[11]
P5	A[15]
P6	CAS
P7	D[1]
P8	SDCKE
P9	D[5]
P10	D[8]
P11	D[15]
P12	PC[0]
P13	PB[0]
P14	PC[8]
P15	PC[9]
P16	PC[10]
P17	PC[11]
R1	A[0]
R2	A[2]
R3	A[7]
R4	A[10]
R5	A[14]
R6	SDA10
R7	D[0]
R8	VDDIOM
R9	D[6]
R10	D[9]
R11	NC
R12	VDDIOM
R13	PC[1]
R14	PB[1]
R15	PC[5]
R16	PC[6]
R17	PC[7]
T1	A[3]
T2	A[5]
T3	A[8]
T4	A[12]
T5	A[16]
T6	RAS
T7	D[2]
T8	D[4]
T9	D[7]
T10	D[10]
T11	D[14]
T12	VDDANA
T13	PA[17]
T14	PA[19]
T15	PC[2]
T16	PC[3]
T17	PC[4]
U1	A[4]
U2	A[6]
U3	A[9]
U4	A[13]
U5	A[17]
U6	SDWE
U7	D[3]
U8	SDCK
U9	D[11]
U10	D[12]
U11	D[13]
U12	TSADVREF
U13	PA[18]
U14	PA[20]
U15	PD[6]
U16	PD[7]
U17	GNDANA

Note: 1. Shaded cells define the pins powered by VDDIOM.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs and have no pull-up resistors.

TDO is an output, driven at up to VDDIOP, and have no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

All the JTAG signals are supplied with VDDIOP except JTAGSEL supplied by VDDBU.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP.

As the product integrates power-on reset cells, which manages the processor and the JTAG reset, the NRST and NTRST pin can be left unconnected.

The NRST and NTRST pins integrates a permanent pull-up resistor of 100 kΩ typical to VDDIOP.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines which are managed by the PIO Controllers integrate a programmable pull-up resistor. Refer to the section “AT91SAM9R64/RL64 Electrical Characteristics” in the product datasheet for more details.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables.

6.5 Shutdown Logic Pins

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

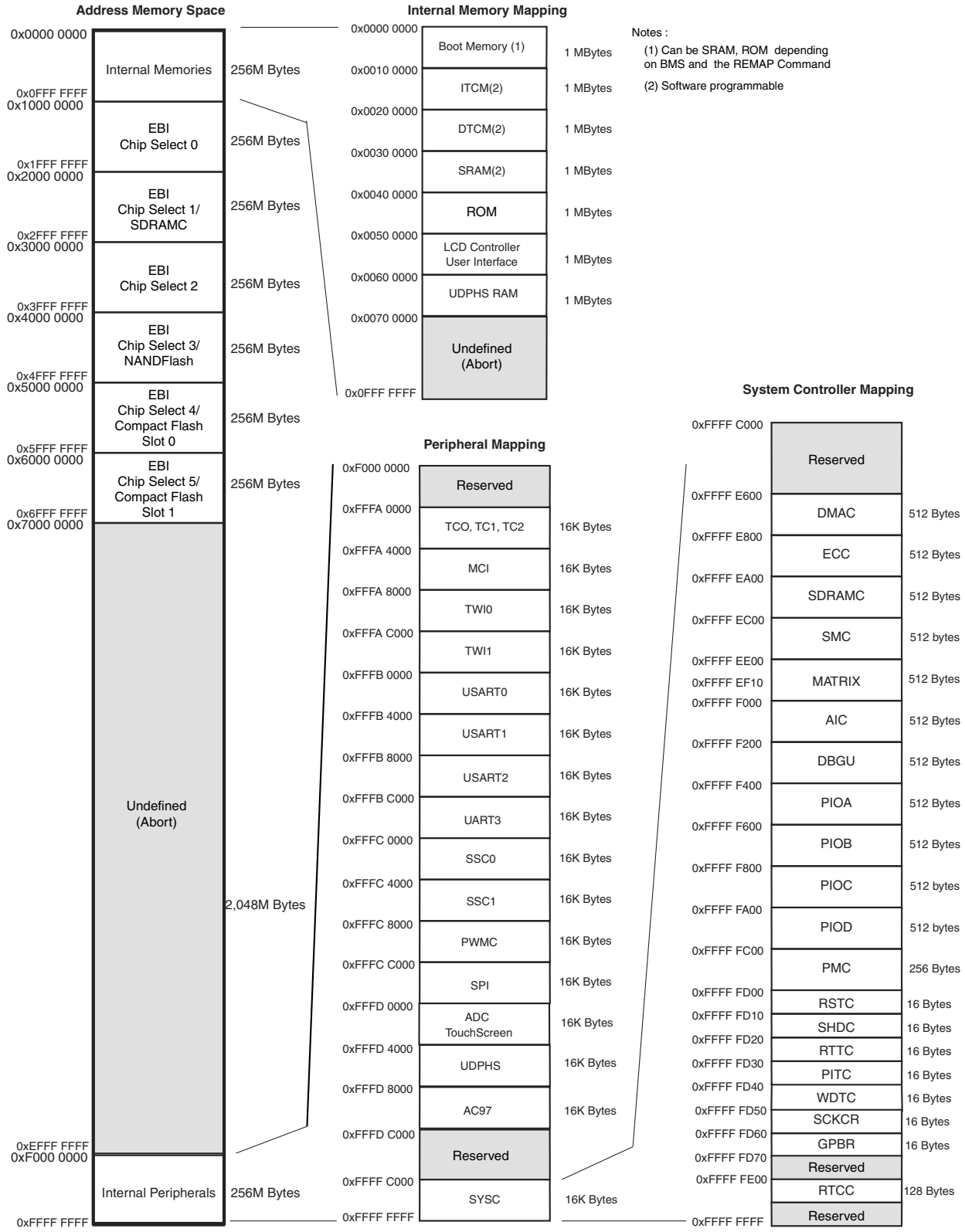
7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets

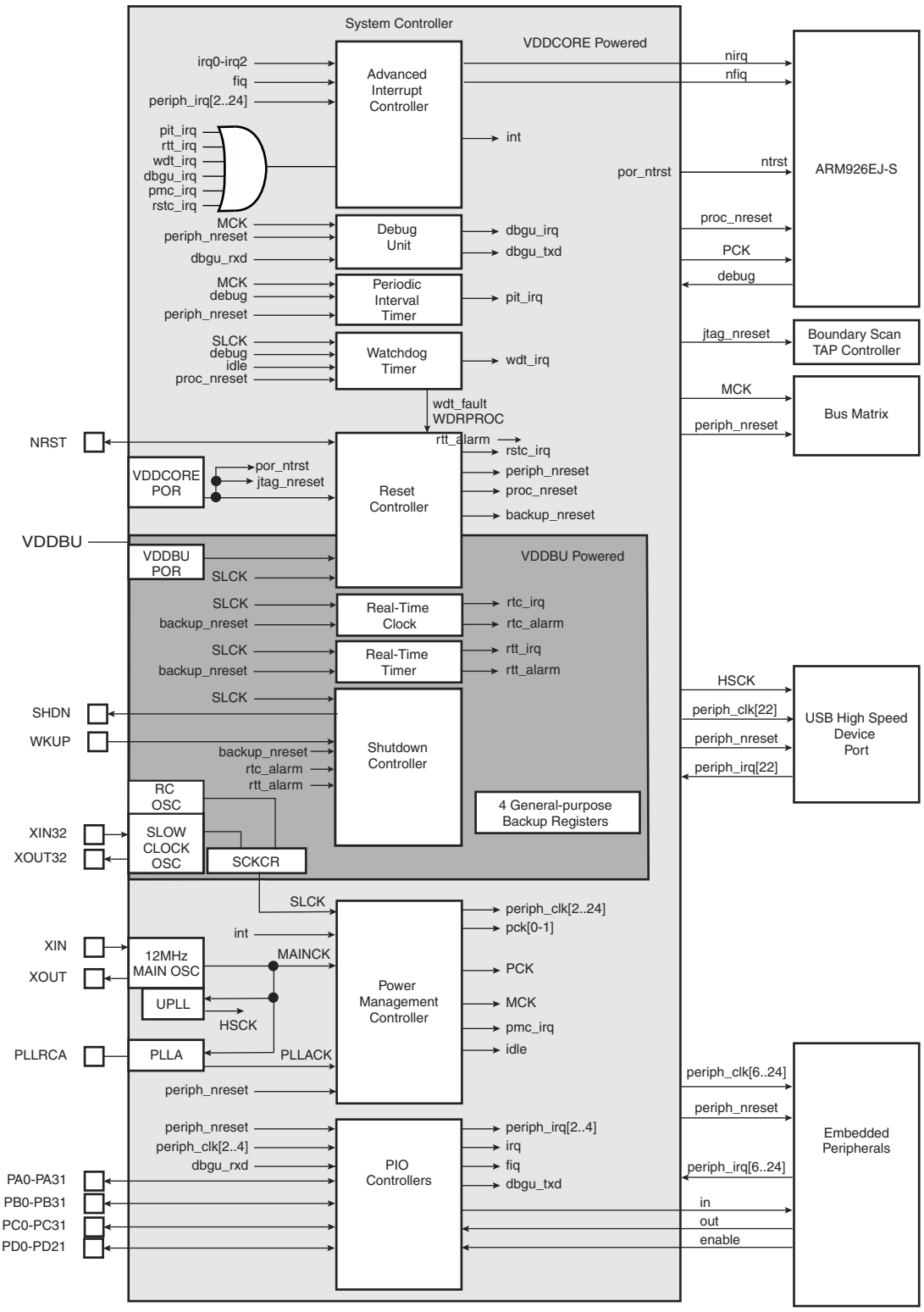
8. Memories

Figure 8-1. AT91SAM9R64/RL64 Memory Mapping



9.2 Block Diagram

Figure 9-1. System Controller Block Diagram



9.3 Reset Controller

The Reset Controller is based on two Power-on-Reset cells, one on VDDBU and one on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset (VDDBU rising), a wake-up reset (VDDCORE rising), a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDBU.

9.4 Shutdown Controller

The Shutdown Controller is supplied on VDDBU and allows a software-controllable shut down of the system through the pin SHDN. An input change of the WKUP pin or an alarm releases the SHDN pin, and thus wakes up the system power supply.

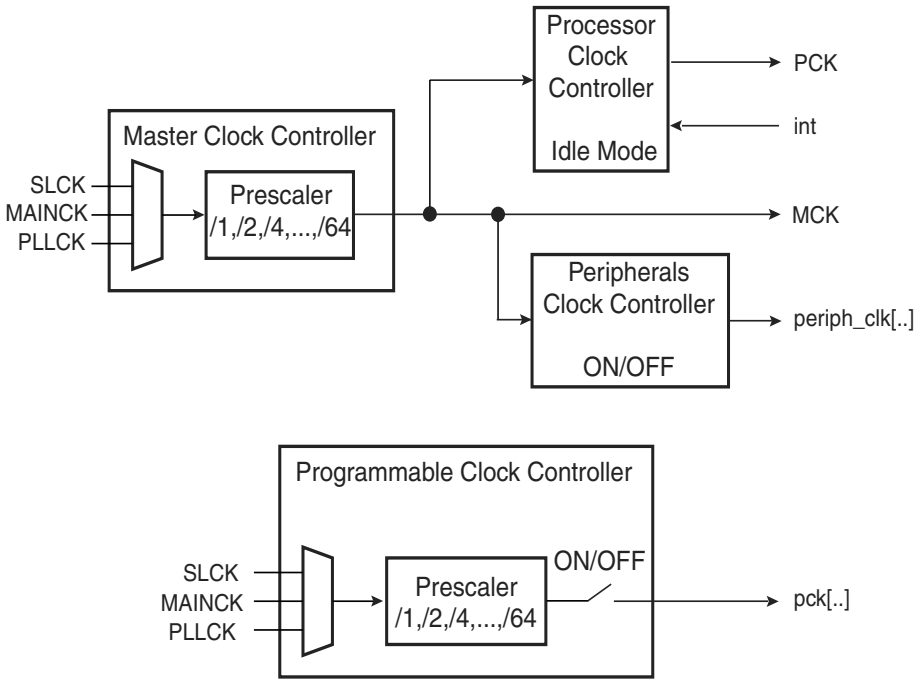
9.5 Clock Generator

The Clock Generator is made up of:

- One low-power 32768 Hz Slow Clock Oscillator with bypass mode
- One low-power RC oscillator
- One 12 MHz Main Oscillator, which can be bypassed
- One 480 MHz PLL (UPLL or PLLB) providing a clock for the USB High Speed Device Controller
- One 80 to 240 MHz programmable PLL, providing the PLL Clock (PLLCK). This PLL has an input divider to offer a wider range of output frequencies from the 12 MHz input, the only limitation being the lowest input frequency shall be higher or equal to 1 MHz.

- Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
- Backup Mode, Main Power Supplies off, VDDBU powered by a battery

Figure 9-3. AT91SAM9R64/RL64 Power Management Controller Block Diagram



9.8 Periodic Interval Timer

- Includes a 20-bit Periodic Counter, with less than 1 µs accuracy
- Includes a 12-bit Interval Overlay Counter
- Real Time OS or Linux®/WindowsCE® compliant tick generator

9.9 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

9.10 Real-Time Timer

- Real-Time Timer, allowing backup of time with different accuracies
  - 32-bit Free-running back-up Counter
  - Integrates a 16-bit programmable prescaler running on slow clock
  - Alarm Register capable to generate a wake-up of the system through the Shut Down Controller

9.11 Real-Time Clock

- Low power consumption
- Full asynchronous design

  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support
  - Offers visibility of and interrupt trigger from COMMRX and COMMTX signals from the ARM Processor's ICE Interface

9.15 Chip Identification

- Chip ID: 0x019B03A0
- JTAG ID: 0x05B2003F
- ARM926 TAP ID: 0x0792603F

9.16 PIO Controllers

- 4 PIO Controllers, PIOA, PIOB, PIOC and PIOD, controlling a maximum of 118 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
  - PIOA has 32 I/O Lines
  - PIOB has 32 I/O Lines
  - PIOC has 32 I/O Lines
  - PIOD has 22 I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change interrupt
  - Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

10. Peripherals

10.1 Peripheral Mapping

As shown in Figure 8-1, the Peripherals are mapped in the upper 256M bytes of the address space between the addresses 0xFFFA 0000 and 0xFFFC FFFF.

Each User Peripheral is allocated 16K bytes of address space.

10.2 Peripheral Identifiers

The Table 10-1 defines the Peripheral Identifiers of the AT91SAM9R64/RL64. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. AT91SAM9R64/RL64 Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	**AIC**	Advanced Interrupt Controller	FIQ
1	**SYSC**	System Controller Interrupt	
2	**PIOA**	Parallel I/O Controller A,	
3	**PIOB**	Parallel I/O Controller B	
4	**PIOC**	Parallel I/O Controller C	
5	**PIOD**	Parallel I/O Controller D	
6	**US0**	USART 0	
7	**US1**	USART 1	
8	**US2**	USART 2	
9	**US3**	USART 3	
10	**MCI**	Multimedia Card Interface	
11	**TWI0**	Two-Wire Interface 0	
12	**TWI1**	Two-Wire Interface 1	
13	**SPI**	Serial Peripheral Interface	
14	**SSC0**	Synchronous Serial Controller 0	
15	**SSC1**	Synchronous Serial Controller 1	
16	**TC0**	Timer Counter 0	
17	**TC1**	Timer Counter 1	
18	**TC2**	Timer Counter 2	
19	**PWMC**	Pulse Width Modulation Controller	
20	**TSADCC**	Touch Screen ADC Controller	
21	**DMAC**	DMA Controller	
22	**UDPHS**	USB Device High Speed	
23	**LCDC**	LCD Controller (AT91SAM9RL64 only)	
24	**AC97**	AC97 Controller	
25-30	**-**	Reserved	
31	**AIC**	Advanced Interrupt Controller	IRQ

Note: Setting AIC, SYSIRQ, LCDC and IRQ bits in the clock set/clear registers of the PMC has no effect.

10.4.1.2 AT91SAM9RL64 PIO Controller B Multiplexing

Table 10-3. AT91SAM9RL64 Multiplexing on PIO Controller B

PIO Controller B					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PB0	TXD3		I/O	VDDIOP		
PB1	RXD3		I/O	VDDIOP		
PB2	A21/NANDALE		A21	VDDIOM		
PB3	A22/NANDCLE		A22	VDDIOM		
PB4	NANDOE		I/O	VDDIOM		
PB5	NANDWE		I/O	VDDIOM		
PB6	NCS3/NANDCS		I/O	VDDIOM		
PB7	NCS4/CFCS0	NPCS1	I/O	VDDIOM		
PB8	CFCE1	PWM0	I/O	VDDIOM		
PB9	CFCE2	PWM1	I/O	VDDIOM		
PB10	A25/CFRNW	FIQ	A25	VDDIOM		
PB11	A18		A18	VDDIOM		
PB12	A19		A19	VDDIOM		
PB13	A20		A20	VDDIOM		
PB14	A23	PCK0	A23	VDDIOM		
PB15	A24	ADTRG	A24	VDDIOM		
PB16	D16		I/O	VDDIOM		
PB17	D17		I/O	VDDIOM		
PB18	D18		I/O	VDDIOM		
PB19	D19		I/O	VDDIOM		
PB20	D20		I/O	VDDIOM		
PB21	D21		I/O	VDDIOM		
PB22	D22		I/O	VDDIOM		
PB23	D23		I/O	VDDIOM		
PB24	D24		I/O	VDDIOM		
PB25	D25		I/O	VDDIOM		
PB26	D26		I/O	VDDIOM		
PB27	D27		I/O	VDDIOM		
PB28	D28		I/O	VDDIOM		
PB29	D29		I/O	VDDIOM		
PB30	D30		I/O	VDDIOM		
PB31	D31		I/O	VDDIOM		

10.4.1.4 AT91SAM9RL64 PIO Controller D Multiplexing

Table 10-5. AT91SAM9RL64 Multiplexing on PIO Controller D

PIO Controller D						Application Usage	
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Reset State**	**Power Supply**	**Function**	**Comments**
PD0	NCS2			I/O	VDDIOP		
PD1	AC97_FS			I/O	VDDIOP		
PD2	AC97_CK	SCK1		I/O	VDDIOP		
PD3	AC97_TX	CTS3		I/O	VDDIOP		
PD4	AC97_RX	RTS3		I/O	VDDIOP		
PD5	DTXD	PWM2		I/O	VDDIOP		
PD6	AD4			I/O	VDDANA		
PD7	AD5			I/O	VDDANA		
PD8	NPCS2	PWM3		I/O	VDDIOP		
PD9	SCK2	NPCS3		I/O	VDDIOP		
PD10	TWD1	TIOA2		I/O	VDDIOP		
PD11	TWCK1	TIOB2		I/O	VDDIOP		
PD12	PWM2	PCK1		I/O	VDDIOP		
PD13	NCS5/CFCS1	NPCS3		I/O	VDDIOP		
PD14	DSR0	PWM0		I/O	VDDIOP		
PD15	DTR0	PWM1		I/O	VDDIOP		
PD16	DCD0	PWM2		I/O	VDDIOP		
PD17	RI0			I/O	VDDIOP		
PD18	PWM3			I/O	VDDIOP		
PD19	PCK0			I/O	VDDIOP		
PD20	PCK1			I/O	VDDIOP		
PD21	TCLK2			I/O	VDDIOP		

10.4.2 AT91SAM9R64 PIO Multiplexing

Note: In Table 10-6, Table 10-7, Table 10-8 and Table 10-9, shaded cells indicate I/O lines that are NOT available on the AT91SAM9R64.

10.4.2.1 AT91SAM9R64 PIO Controller A Multiplexing

Table 10-6. AT91SAM9R64 Multiplexing on PIO Controller A

PIO Controller A					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PA0	MC_DA0		I/O	VDDIOP		
PA1	MC_CDA		I/O	VDDIOP		
PA2	MC_CK		I/O	VDDIOP		
PA3	MC_DA1	TCLK0	I/O	VDDIOP		
PA4	MC_DA2	TIOA0	I/O	VDDIOP		
PA5	MC_DA3	TIOB0	I/O	VDDIOP		
PA6	TXD0		I/O	VDDIOP		
PA7	RXD0		I/O	VDDIOP		
PA8	NA	NA				Reserved
PA9	NA	NA				Reserved
PA10	CTS0	RK0	I/O	VDDIOP		
PA11	TXD1		I/O	VDDIOP		
PA12	RXD1		I/O	VDDIOP		
PA13	TXD2		I/O	VDDIOP		
PA14	RXD2		I/O	VDDIOP		
PA15	TD0		I/O	VDDIOP		
PA16	RD0		I/O	VDDIOP		
PA17	AD0		I/O	VDDIOP		
PA18	AD1	RTS1	I/O	VDDIOP		
PA19	AD2	CTS1	I/O	VDDIOP		
PA20	NA	NA				Reserved
PA21	DRXD		I/O	VDDIOP		
PA22	DTXD	RF0	I/O	VDDIOP		
PA23	TWD0		I/O	VDDIOP		
PA24	TWCK0		I/O	VDDIOP		
PA25	MISO		I/O	VDDIOP		
PA26	MOSI		I/O	VDDIOP		
PA27	SPCK		I/O	VDDIOP		
PA28	NPCS0		I/O	VDDIOP		
PA29	NA	NA				Reserved
PA30	NA	NA				Reserved
PA31	NWAIT	IRQ	I/O	VDDIOP		

10.4.2.3 AT91SAM9R64 PIO Controller C Multiplexing

Table 10-8. AT91SAM9R64 Multiplexing on PIO Controller C

PIO Controller C					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PC0	TF0		I/O	VDDIOP		
PC1	TK0		I/O	VDDIOP		
PC2-PC31	NA	NA				Reserved

10.4.2.4 AT91SAM9R64 PIO Controller D Multiplexing

Table 10-9. AT91SAM9R64 Multiplexing on PIO Controller D

PIO Controller D						Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PD0-PD17	NA	NA					Reserved
PD18	PWM3			I/O	VDDIOP		
PD19	PCK0			I/O	VDDIOP		
PD20	PCK1			I/O	VDDIOP		
PD21	TCLK2			I/O	VDDIOP		

11. Embedded Peripherals Overview

11.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

11.2 Two-wire Interface (TWI)

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations
- Supports either master or slave modes
- Compatible with Standard Two-wire Serial Memories
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbits
- General Call Supported in Slave mode
- Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode Only
  - One Channel for the Receiver, One Channel for the Transmitter
  - Next Buffer Support

11.3 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first

  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

11.4 Serial Synchronous Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

11.5 AC97 Controller

- Compatible with AC97 Component Specification V2.2
- Capable to Interface with a Single Analog Front end
- Three independent RX Channels and three independent TX Channels
  - One RX and one TX channel dedicated to the AC97 Analog Front end control
  - One RX and one TX channel for data transfers, associated with a PDC
  - One RX and one TX channel for data transfers with no PDC
- Time Slot Assigner allowing to assign up to 12 time slots to a channel
- Channels support mono or stereo up to 20 bit sample length
  - Variable sampling rate AC97 Codec Interface (48KHz and below)

11.6 Timer Counter (TC)

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation

- Endpoint 0: 64 bytes, 1 bank mode
- Endpoint 1 & 2: 1024 bytes, 2 banks mode, HS isochronous capable, DMA
- Endpoint 3 & 4: 1024bytes, 3 banks mode, DMA
- Endpoint 5 & 6: 1024 bytes, 3 banks mode, HS isochronous capable, DMA

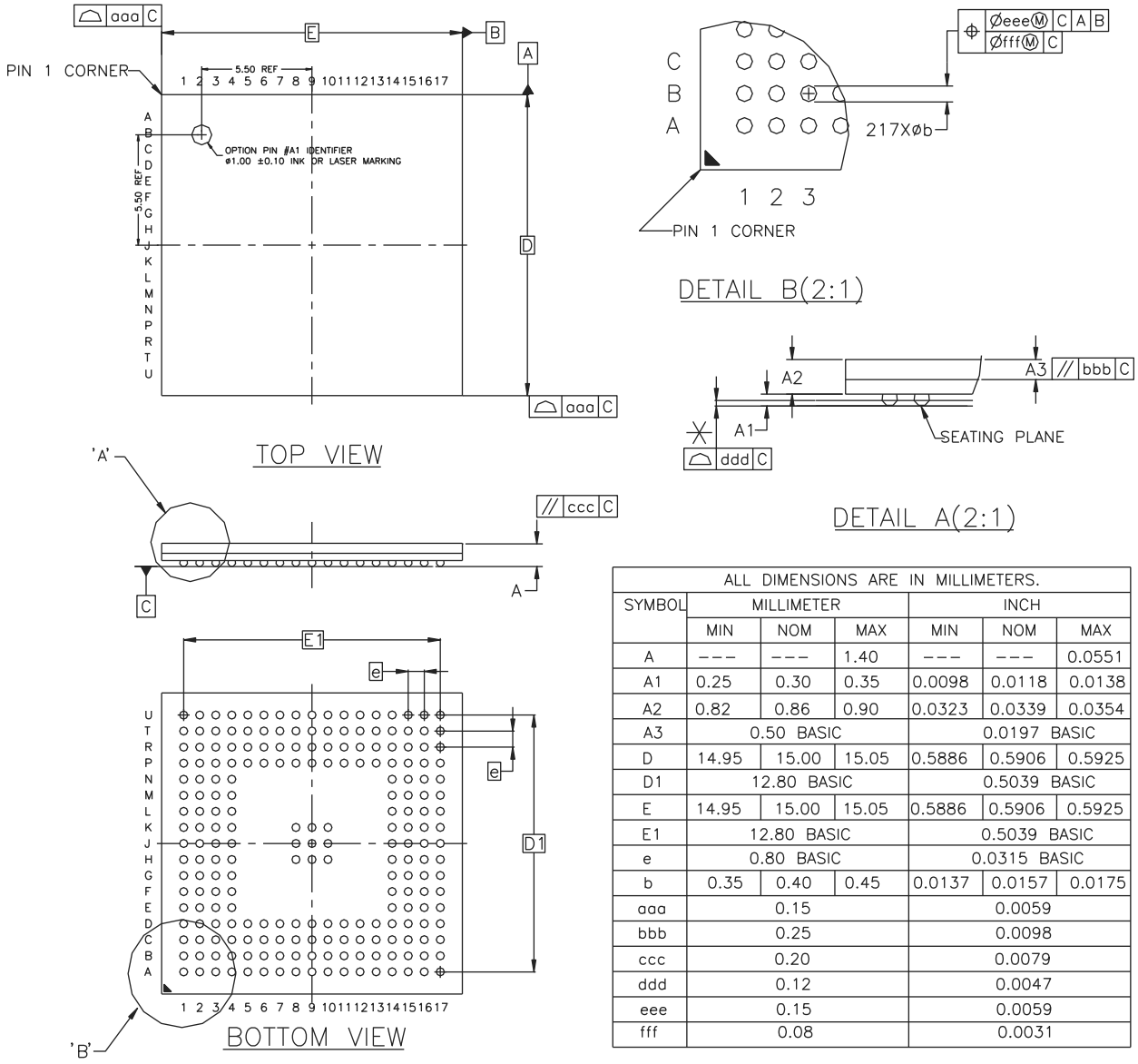
11.10 LCD Controller (LCDC)

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported.
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048x2048

11.11 Touch Screen Analog-to-digital Converter (TSADCC)

- 6-channel ADC
- Support 4-wire resistive Touch Screen
- 10-bit 384 Ksamples/sec. Successive Approximation Register ADC
- -3/+3 LSB Integral Non Linearity, -2/+2 LSB Differential Non Linearity
- Integrated 6-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

Figure 12-2. 217-ball LFBGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.82	0.86	0.90	0.0323	0.0339	0.0354
A3	0.50 BASIC			0.0197 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5925
D1	12.80 BASIC			0.5039 BASIC		
E	14.95	15.00	15.05	0.5886	0.5906	0.5925
E1	12.80 BASIC			0.5039 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0137	0.0157	0.0175
aaa	0.15			0.0059		
bbb	0.25			0.0098		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		