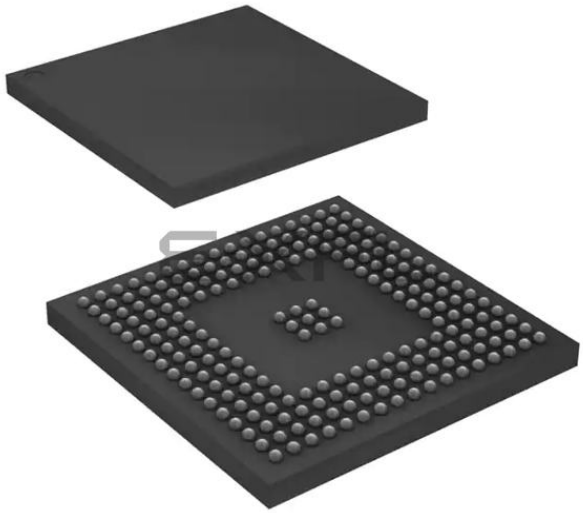

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	240MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	AC'97, LCD, POR, PWM, WDT
Number of I/O	118
Program Memory Size	32KB (32K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	217-LFBGA
Supplier Device Package	217-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9rl64-cu

- **Master, Multi-master and Slave Mode Operation**
- **Bit Rate: Up to 400 Kbits**
- **General Call Supported in Slave Mode**
- **Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode Only (TWI0 only)**

- **SAM-BA® Boot Assistant**
  - **Default Boot Program**
  - **Interface with SAM-BA Graphic User Interface**
- **IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins**
- **Required Power Supplies:**
  - **1.08 to 1.32V for VDDCORE, VDDUTMIC, VDDPLLB and VDDBU**
  - **3.0V to 3.6V for VDDPLLA, VDDANA, VDDUTMII and VDDIOP**
  - **Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM**
- **Available in a 144-ball BGA (AT91SAM9R64) and a 217-ball LFBGA (AT91SAM9RL64) Package**

1. Description

The AT91SAM9R64/RL64 device is based on the integration of an ARM926EJ-S processor with a large fast SRAM and a wide range of peripherals.

The AT91SAM9R64/RL64 embeds one USB Device High Speed Controller, one LCD Controller (for AT91SAM9RL64 only), one AC97 controller, a 2-channel DMA Controller, four USARTs, two SSCs, one SPI, two TWIs, three Timer Counter channels, a 4-channel PWM generator, one Multimedia Card interface and a 6-channel Analog-to-digital converter that also provides resistive touch screen management.

The AT91SAM9R64/RL64 is architectured on a 6-layer bus matrix. It also features an External Bus Interface capable of interfacing with a wide range of memory and peripheral devices.

Some features are not available for AT91SAM9R64 in the 144-ball BGA package.

Separate block diagrams and PIO multiplexing are provided in this document. Table 1-1 lists the features and signals of AT91SAM9RL64 that are not available or partially available for AT91SAM9R64. When the signal is multiplexed on a PIO, the PIO line is specified.

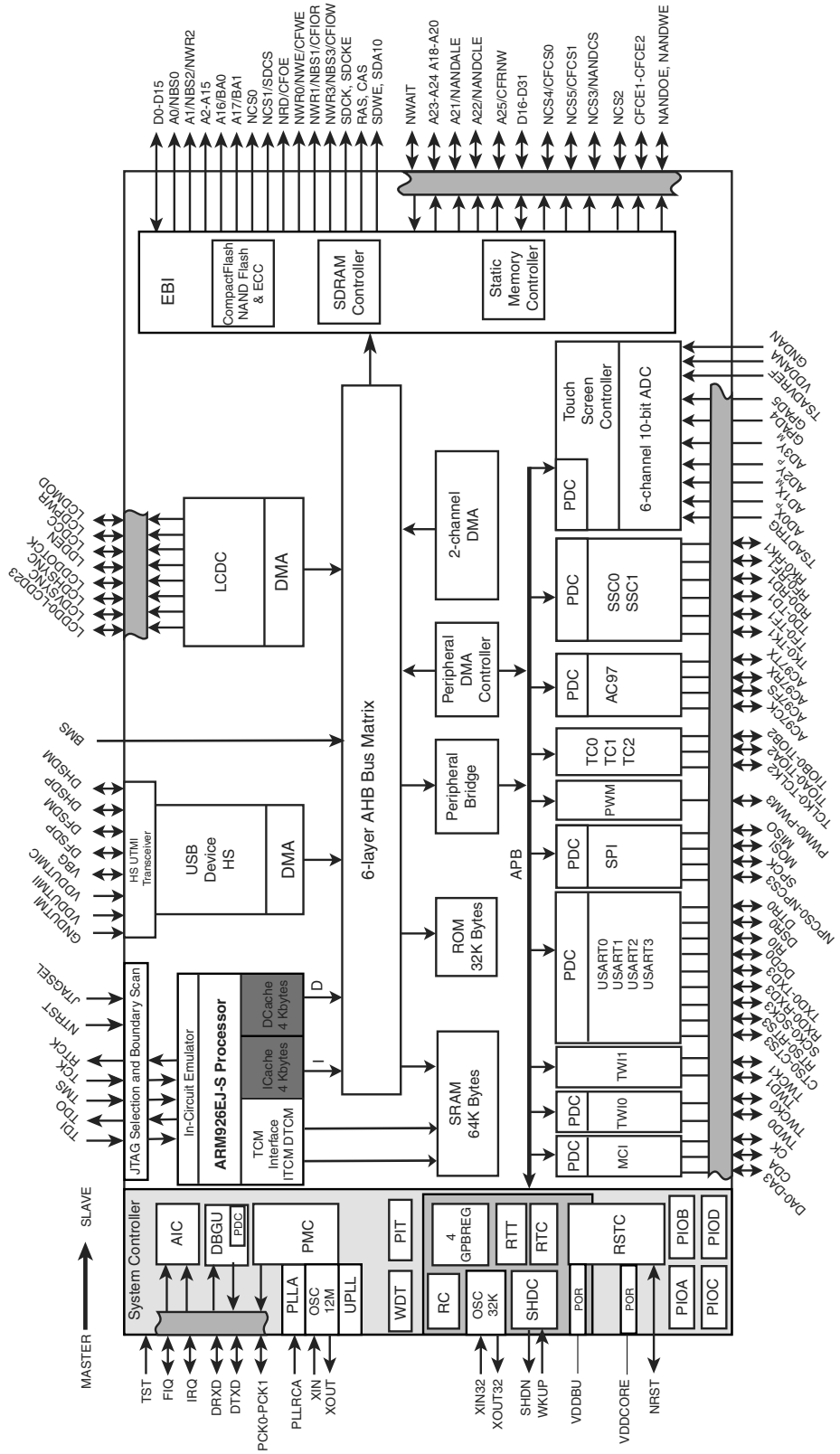
Table 1-1. Unavailable or Partially Available Features and Signals in AT91SAM9R64

Feature	Full/Partial	Signal	Peripheral A	Peripheral B
AC97	Full	AC97FS AC97CK AC97TX AC97RX	PD1 PD2 PD3 PD4	-
EBI	Partial	D16-D31 NCS2 NCS5/CFCS1	PB16-PB31 PD0 PD13	-
LCDC	Full	LCDMOD LCDCC LCDVSYNC LCDHSYNC LCDDOTCK LCDDEN LCDD0-LCDD23	PC2 PC3 PC4 PC5 PC6 PC7 PC8-PC31	-

Table 1-1. Unavailable or Partially Available Features and Signals in AT91SAM9R64

Feature	Full/Partial	Signal	Peripheral A	Peripheral B
PWM	Partial	PWM2	PD5 and PD12	-
SPI	Partial	NPCS2 NPCS3	PD8	 PD9 and PD13
SSC1	Full	RF1 RK1 TD1 RD1 TK1 TF1	-	PA8 PA9 PA13 PA14 PA29 PA30
Touchscreen ADC	Partial	AD3YM GPAD4 GPAD5	PA20 PD6 PD7	-
TC	Partial	TIOA1 TIOB1 TCLK1 TIOA2 TIOB2	-	PC29 PC30 PC31 PD10 PD11
TWI	Full	TWD1 TWCK1	PD10 PD11	-
USART0	Partial	SCK0 RTS0 CTS0 DSR0 DTR0 DCD0 RI0	PA8 PA9 PA10 PD14 PD15 PD16 PD17	-
USART1	Partial	SCK1	-	PD2
USART2	Partial	SCK2 RTS2 CTS2	PD9 PA29 PA30	-
USART3	Partial	SCK3 RTS3 CTS3	-	PA20 PD3 PD4

Figure 2-2. AT91SAM9RL64 Block Diagram



3. Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM	EBI I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOP	Peripherals I/O Lines Power Supply	Power		3.0V to 3.6V
VDDUTMII	USB UTMI+ Interface Power Supply	Power		3.0V to 3.6V
VDDUTMIC	USB UTMI+ Core Power Supply	Power		1.08V to 1.32V
GNDUTMI	USB UTMI Ground	Ground		
VDDBU	Backup I/O Lines Power Supply	Power		1.08V to 1.32V
GNDBU	Backup Ground	Ground		
VDDPLLA	PLL Power Supply	Power		3.0V to 3.6V
GNDPLLA	PLL Ground	Ground		
VDDPLLB	UTMI PLL and OSC 12M Power Supply	Power		1.08 V to 1.32V
GNDPLLB	UTMI PLL and OSC 12M Ground	Ground		
VDDANA	ADC Analog Power Supply	Power		3.0V to 3.6V
GNDANA	ADC Analog Ground	Ground		
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
GNDCORE	Ground	Ground		
GND	Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
VBG	Bias Voltage Reference	Analog		
PLLRCA	PLL A Filter	Input		
PCK0 - PCK1	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Driven at 0V only. 0: The device is in backup mode. 1: The device is running (not in backup mode.)
WKUP	Wake-Up Input	Input		Accept between 0V and VDDBU
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
NTRST	Test Reset Signal	Input	Low	Pull-up resistor.
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor
BMS	Boot Mode Select	Input		Must be connected to GND or VDDIOP. No pullup resistor BMS = 0 when tied to GND BMS = 1 when tied to VDDIOP
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
Advanced Interrupt Controller - AIC				
IRQ	External Interrupt Input	Input		
FIQ	Fast Interrupt Input	Input		
PIO Controller - PIOA - PIOB - PIOC-PIOD				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD21	Parallel IO Controller D	I/O		Pulled-up input at reset
External Bus Interface - EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset. D16-D31 not present on AT91SAM9R64.
A0 - A25	Address Bus	Output		0 at reset
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
NCS0 - NCS5	Chip Select Lines	Output	Low	NCS2, NCS5 not present on AT91SAM9R64.
NWR0 - NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	CFCS1 not present on AT91SAM9R64.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
AC97 Controller - AC97C				
AC97RX	AC97 Receive Signal	Input		Not present on AT91SAM9R64.
AC97TX	AC97 Transmit Signal	Output		Not present on AT91SAM9R64.
AC97FS	AC97 Frame Synchronization Signal	Output		Not present on AT91SAM9R64.
AC97CK	AC97 Clock signal	Input		Not present on AT91SAM9R64.
Timer/Counter - TC				
TCLKx	TC Channel x External Clock Input	Input		TCLK1 not present on AT91SAM9R64.
TIOAx	TC Channel x I/O Line A	I/O		TIOA1, TIOA2 not present on AT91SAM9R64.
TIOBx	TC Channel x I/O Line B	I/O		TIOB1, TIOB2 not present on AT91SAM9R64.
Pulse Width Modulation Controller- PWMC				
PMWx	Pulse Width Modulation Output	Output		PWM2 not present on AT91SAM9R64.
Serial Peripheral Interface - SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1 - NPCS3	SPI Peripheral Chip Select	Output	Low	NPCS2, NPCS3 not present on AT91SAM9R64.
Two-Wire Interface - TWIx				
TWDx	TWIx Two-wire Serial Data	I/O		TWD1 not present on AT91SAM9R64.
TWCKx	TWIx Two-wire Serial Clock	I/O		TWCK1 not present on AT91SAM9R64.
Touch Screen Analog-to-Digital Converter				
GPAD0-GPAD5	Analog Inputs	Analog		GPAD4, GPAD5 not present on AT91SAM9R64.
$AD0X_P$	Touch Panel Right side	Analog		Multiplexed with AD0
$AD1X_M$	Touch Panel Left side	Analog		Multiplexed with AD1
$AD2Y_P$	Touch Panel Top side	Analog		Multiplexed with AD2
$AD3Y_M$	Touch Panel Bottom side	Analog		Multiplexed with AD3. Not present on AT91SAM9R64.
TSADTRG	ADC Trigger	Input		
TSADVREF	ADC Reference	Analog		
LCD Controller - LCDC				
LCDD0 - LCDD23	LCD Data Bus	Output		Not present on AT91SAM9R64.
LCDVSYNC	LCD Vertical Synchronization	Output		Not present on AT91SAM9R64.
LCDHSYNC	LCD Horizontal Synchronization	Output		Not present on AT91SAM9R64.
LCDDOTCK	LCD Dot Clock	Output		Not present on AT91SAM9R64.
LCDDEN	LCD Data Enable	Output		Not present on AT91SAM9R64.
LCDCC	LCD Contrast Control	Output		Not present on AT91SAM9R64.
LCDPWR	LCD panel Power enable control	Output		Not present on AT91SAM9R64.
LCDMOD	LCD Modulation signal	Output		Not present on AT91SAM9R64.

4.2 Pinout

Table 4-1. AT91SAM9R64 Pinout for 144-ball BGA Package

Pin	Signal Name
A1	DFSDM
A2	DHSDM
A3	XIN
A4	XOUT
A5	XIN32
A6	XOUT32
A7	TDO
A8	PA[31]
A9	PA[22]
A10	PA[16]
A11	PA[14]
A12	PA[11]
B1	DFSDP
B2	DHSDP
B3	NC
B4	VDDPLLB
B5	GNDPLLB
B6	TMS
B7	RTCK
B8	PA[27]
B9	PA[21]
B10	PA[12]
B11	PD[21]
B12	PA[10]
C1	VDDPLLA
C2	VBG
C3	VDDBU
C4	SHDN
C5	WKUP
C6	NTRST
C7	TDI
C8	PA[28]
C9	PA[23]
C10	PA[7]
C11	PD[19]
C12	PD[18]

Pin	Signal Name
D1	PLLRCA
D2	VDDUTMII
D3	NWR3/NBS3/CFIOW
D4	NWR1/NBS1/CFIOR
D5	JTAGSEL
D6	GNDBU
D7	TCK
D8	PA[26]
D9	PA[24]
D10	PA[13]
D11	PA[6]
D12	PD[20]
E1	GNDPLLA
E2	NWR0/NWE/CFWE
E3	NRD/CFOE
E4	NCS0
E5	NCS1/SDCS
E6	PB[2]
E7	NRST
E8	BMS
E9	PA[25]
E10	PA[15]
E11	PA[5]
E12	PA[4]
F1	PB[5]
F2	PB[6]
F3	PB[7]
F4	PB[8]
F5	PB[3]
F6	PB[4]
F7	TST
F8	VDDUTMIC
F9	PA[3]
F10	PA[2]
F11	PA[0]
F12	PA[1]

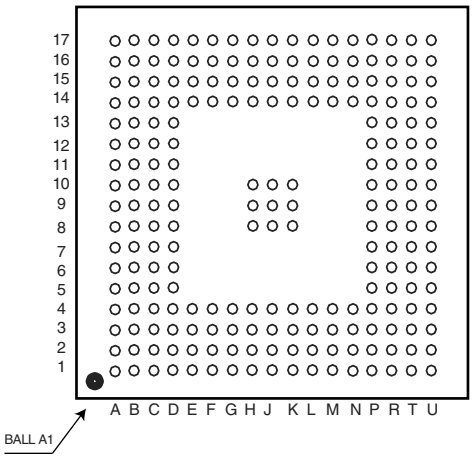
Pin	Signal Name
G1	PB[10]
G2	PB[11]
G3	PB[12]
G4	PB[9]
G5	PB[13]
G6	GND
G7	GND
G8	GND
G9	GNDUTMI
G10	VDDCORE
G11	VDDIOP
G12	VDDIOP
H1	PB[14]
H2	PB[15]
H3	A[0]
H4	A[2]
H5	SDA10
H6	D[1]
H7	GND
H8	GND
H9	VDDIOM
H10	SDCKE
H11	VDDCORE
H12	VDDIOP
J1	A[4]
J2	A[1]
J3	A[3]
J4	A[14]
J5	CAS
J6	D[2]
J7	D[5]
J8	D[12]
J9	D[14]
J10	VDDIOM
J11	D[10]
J12	D[9]

Pin	Signal Name
K1	A[5]
K2	A[6]
K3	A[13]
K4	A[15]
K5	RAS
K6	D[3]
K7	D[6]
K8	D[13]
K9	VDDIOM
K10	VDDIOM
K11	D[11]
K12	PB[1]
L1	A[7]
L2	A[8]
L3	A[11]
L4	A[16]
L5	SDWE
L6	D[4]
L7	D[7]
L8	D[15]
L9	PC[1]
L10	PC[0]
L11	PB[0]
L12	GNDANA
M1	A[9]
M2	A[10]
M3	A[12]
M4	A[17]
M5	D[0]
M6	SDCK
M7	D[8]
M8	ADVREF
M9	VDDANA
M10	PA[17]
M11	PA[18]
M12	PA[19]

4.3 217-ball LFBGA Package Outline

Figure 4-2 shows the orientation of the 217-ball LFBGA package.

Figure 4-2. 217-ball LFBGA Pinout (Top View)



  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 4-Kbyte Data Cache, 4-Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Matrix Masters

The Bus Matrix of the AT91SAM9R64/RL64 product manages 6 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	DMA Controller
Master 1	USB Device High Speed DMA
Master 2	LCD Controller DMA

Table 7-1. List of Bus Matrix Masters

Master 3	Peripheral DMA Controller
Master 4	ARM926™ Instruction
Master 5	ARM926 Data

7.3 Matrix Slaves

The Bus Matrix of the AT91SAM9R64/RL64 product manages 6 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal ROM
Slave 1	Internal SRAM
Slave 2	LCD Controller User Interface
Slave 3	UDP High Speed RAM
Slave 4	External Bus Interface (EBI)
Slave 5	Peripheral Bridge

7.4 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the USB Device High speed DMA to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown as "-" in the following table.

Table 7-3. AT91SAM9R64/RL64 Master to Slave Access

Masters		0	1	2	3	4	5
Slaves		DMA Controller	USB HS Device DMA	LCD Controller DMA	Peripheral DMA	ARM926 Instruction	ARM926 Data
0	Internal ROM	X	X		X	X	X
1	Internal SRAM	X	X	X	X	X	X
2	LCD Controller User Interface	-	-	-	-	X	X
3	UDP High Speed RAM	-	-	-	-	X	X
4	External Bus Interface	X	X	X	X	X	X
5	Peripheral Bridge	X	X	X	-	-	-

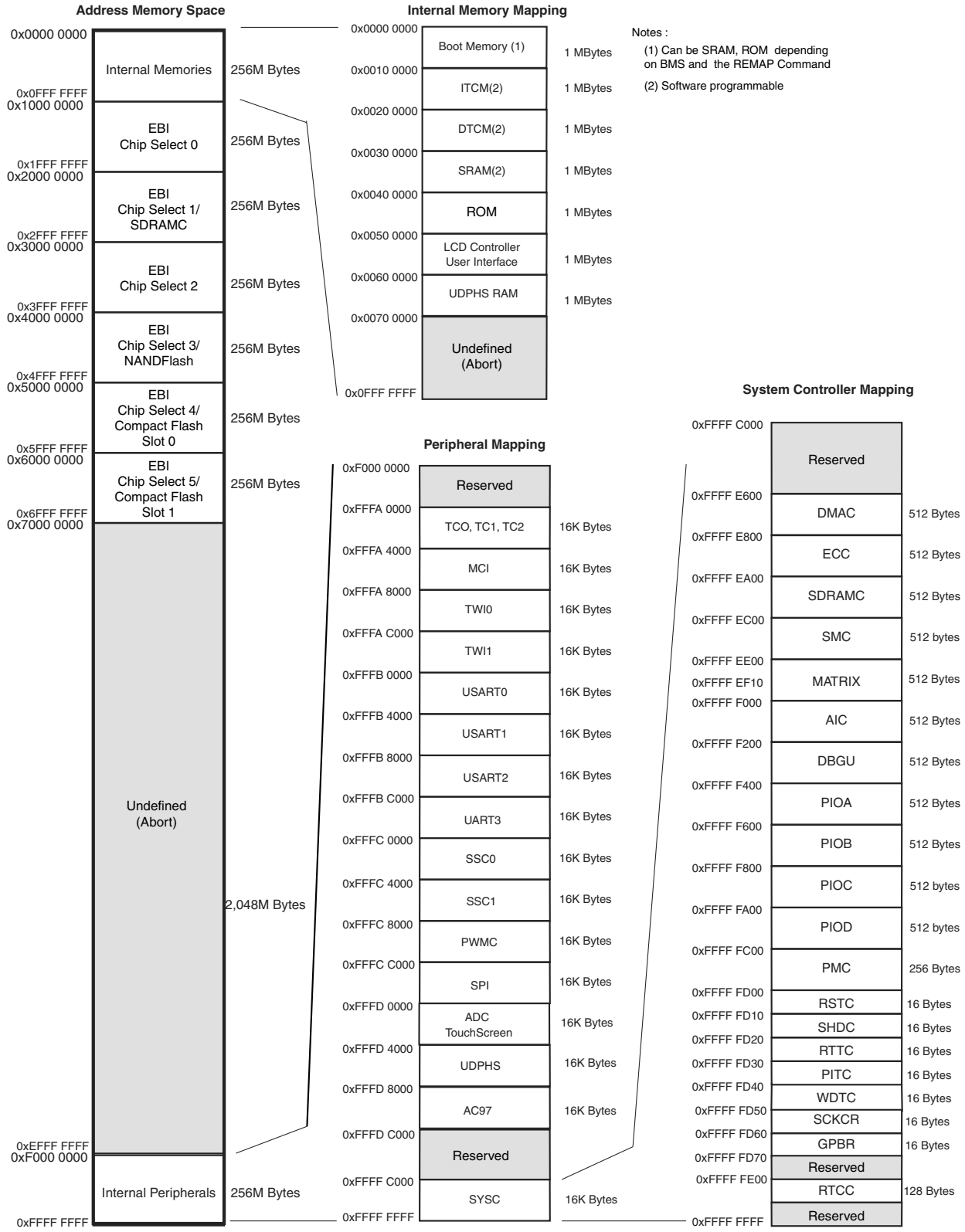
7.5 Peripheral DMA Controller (PDC)

- Acting as one AHB Bus Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer support, prevents strong real-time constraints on buffer management.

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

8. Memories

Figure 8-1. AT91SAM9R64/RL64 Memory Mapping



- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

For optimization purposes, nothing else is done. To speed up the boot sequence user programmed software should perform a complete configuration:

- Enable the 32768 Hz oscillator if best accuracy needed
- Program the PMC (main oscillator enable or bypass mode)
- Program and Start the PLL
- Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock
- Switch the main clock to the new value

8.2 External Memories

The AT91SAM9R64/RL64 features one External Bus Interface to offer interface to a wide range of external memories and to any parallel peripheral.

8.2.1 External Bus Interface

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - SLC Nand Flash ECC Controller
- Additional logic for NAND Flash and CompactFlash™
- Optional Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64MBytes linear per chip select)
- Up to 6 chips selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller (SDCS) or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash™ support

8.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

9.2 Block Diagram

Figure 9-1. System Controller Block Diagram

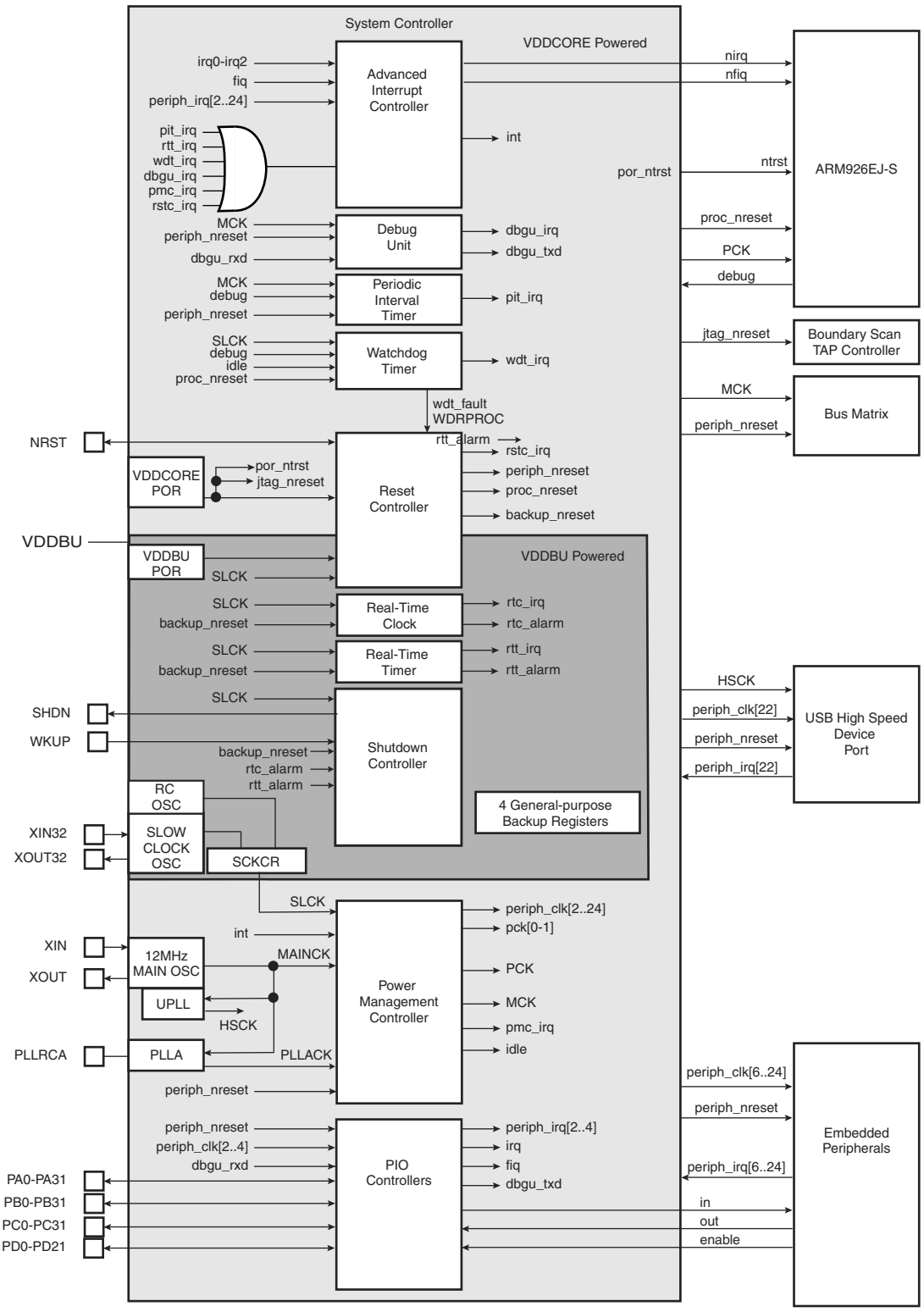
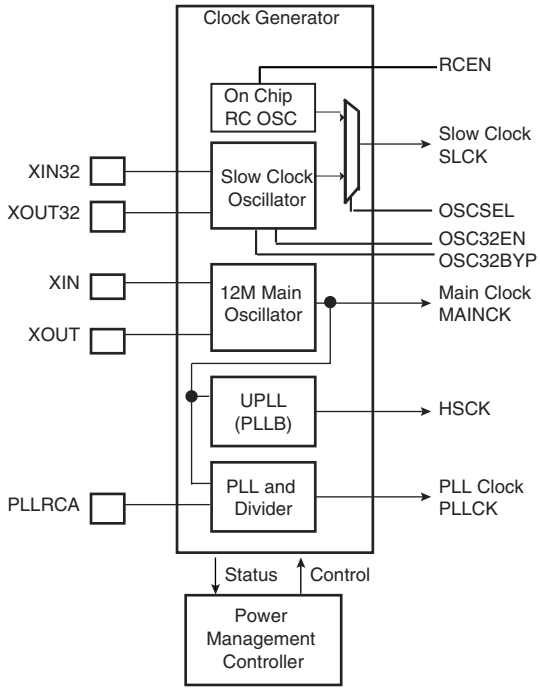


Figure 9-2. Clock Generator Block Diagram



9.6 Slow Clock Selection

9.6.1 Description

The AT91SAM9R64/RL64 slow clock can be generated either by an external 32768Hz crystal or the on-chip RC oscillator. The 32768Hz crystal oscillator can be bypassed to accept an external slow clock on XIN32.

Configuration is located in the slow clock control register (SCKCR) located at address 0xFFFFFD50 in the backed up part of the system controller and so is preserved while VDDBU is present.

Refer to the “Clock Generator” section for more details.

9.7 Power Management Controller

The Power Management Controller provides all the clock signals to the system. It provides:

- the Processor Clock PCK
- the Master Clock MCK, in particular to the Matrix and the memory interfaces
- the USB Device HS Clock HSCK
- independent peripheral clocks, typically at the frequency of MCK
- two programmable clock outputs: PCK0 and PCK1

This allows the software control of five flexible operating modes:

- Normal Mode, processor and peripherals running at a programmable frequency
- Idle Mode, processor stopped waiting for an interrupt
- Slow Clock Mode, processor and peripherals running at low frequency

- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

9.12 General-Purpose Backed-up Registers

- Four 32-bit backup general-purpose registers

9.13 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- One External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect modeIs are enabled
- Fast Forcing
  - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor

9.14 Debug Unit

- Composed of two functions
  - Two-pin UART
  - Debug Communication Channel (DCC) support
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes

10.4.1.4 AT91SAM9RL64 PIO Controller D Multiplexing

Table 10-5. AT91SAM9RL64 Multiplexing on PIO Controller D

PIO Controller D						Application Usage	
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Reset State**	**Power Supply**	**Function**	**Comments**
PD0	NCS2			I/O	VDDIOP		
PD1	AC97_FS			I/O	VDDIOP		
PD2	AC97_CK	SCK1		I/O	VDDIOP		
PD3	AC97_TX	CTS3		I/O	VDDIOP		
PD4	AC97_RX	RTS3		I/O	VDDIOP		
PD5	DTXD	PWM2		I/O	VDDIOP		
PD6	AD4			I/O	VDDANA		
PD7	AD5			I/O	VDDANA		
PD8	NPCS2	PWM3		I/O	VDDIOP		
PD9	SCK2	NPCS3		I/O	VDDIOP		
PD10	TWD1	TIOA2		I/O	VDDIOP		
PD11	TWCK1	TIOB2		I/O	VDDIOP		
PD12	PWM2	PCK1		I/O	VDDIOP		
PD13	NCS5/CFCS1	NPCS3		I/O	VDDIOP		
PD14	DSR0	PWM0		I/O	VDDIOP		
PD15	DTR0	PWM1		I/O	VDDIOP		
PD16	DCD0	PWM2		I/O	VDDIOP		
PD17	RI0			I/O	VDDIOP		
PD18	PWM3			I/O	VDDIOP		
PD19	PCK0			I/O	VDDIOP		
PD20	PCK1			I/O	VDDIOP		
PD21	TCLK2			I/O	VDDIOP		

10.4.2 AT91SAM9R64 PIO Multiplexing

Note: In Table 10-6, Table 10-7, Table 10-8 and Table 10-9, shaded cells indicate I/O lines that are NOT available on the AT91SAM9R64.

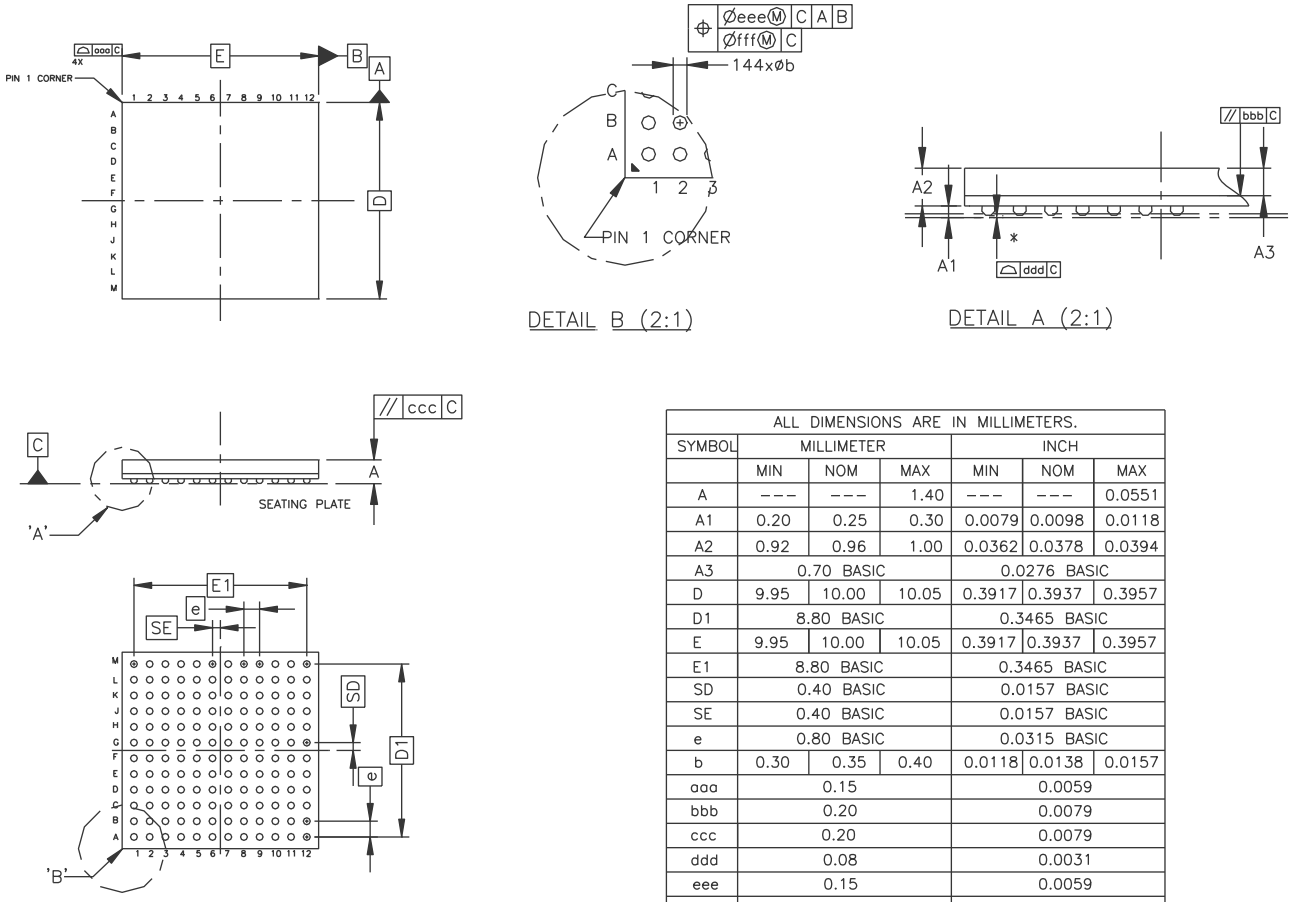
10.4.2.1 AT91SAM9R64 PIO Controller A Multiplexing

Table 10-6. AT91SAM9R64 Multiplexing on PIO Controller A

PIO Controller A					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PA0	MC_DA0		I/O	VDDIOP		
PA1	MC_CDA		I/O	VDDIOP		
PA2	MC_CK		I/O	VDDIOP		
PA3	MC_DA1	TCLK0	I/O	VDDIOP		
PA4	MC_DA2	TIOA0	I/O	VDDIOP		
PA5	MC_DA3	TIOB0	I/O	VDDIOP		
PA6	TXD0		I/O	VDDIOP		
PA7	RXD0		I/O	VDDIOP		
PA8	NA	NA				Reserved
PA9	NA	NA				Reserved
PA10	CTS0	RK0	I/O	VDDIOP		
PA11	TXD1		I/O	VDDIOP		
PA12	RXD1		I/O	VDDIOP		
PA13	TXD2		I/O	VDDIOP		
PA14	RXD2		I/O	VDDIOP		
PA15	TD0		I/O	VDDIOP		
PA16	RD0		I/O	VDDIOP		
PA17	AD0		I/O	VDDIOP		
PA18	AD1	RTS1	I/O	VDDIOP		
PA19	AD2	CTS1	I/O	VDDIOP		
PA20	NA	NA				Reserved
PA21	DRXD		I/O	VDDIOP		
PA22	DTXD	RF0	I/O	VDDIOP		
PA23	TWD0		I/O	VDDIOP		
PA24	TWCK0		I/O	VDDIOP		
PA25	MISO		I/O	VDDIOP		
PA26	MOSI		I/O	VDDIOP		
PA27	SPCK		I/O	VDDIOP		
PA28	NPCS0		I/O	VDDIOP		
PA29	NA	NA				Reserved
PA30	NA	NA				Reserved
PA31	NWAIT	IRQ	I/O	VDDIOP		

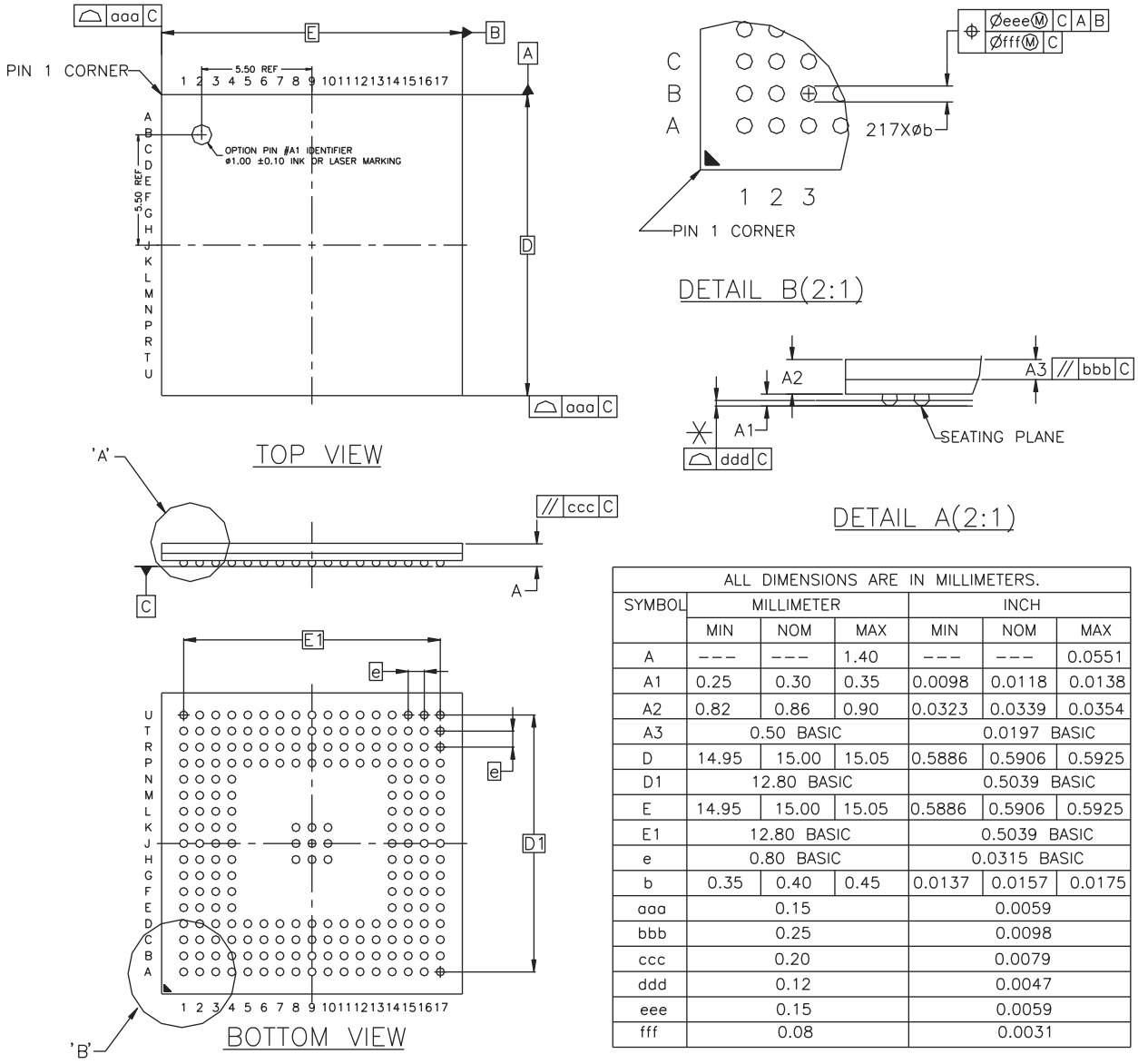
12. Package Drawings

Figure 12-1. 144-ball BGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.20	0.25	0.30	0.0079	0.0098	0.0118
A2	0.92	0.96	1.00	0.0362	0.0378	0.0394
A3	0.70 BASIC			0.0276 BASIC		
D	9.95	10.00	10.05	0.3917	0.3937	0.3957
D1	8.80 BASIC			0.3465 BASIC		
E	9.95	10.00	10.05	0.3917	0.3937	0.3957
E1	8.80 BASIC			0.3465 BASIC		
SD	0.40 BASIC			0.0157 BASIC		
SE	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.30	0.35	0.40	0.0118	0.0138	0.0157
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.08			0.0031		

Figure 12-2. 217-ball LFBGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.82	0.86	0.90	0.0323	0.0339	0.0354
A3	0.50 BASIC			0.0197 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5925
D1	12.80 BASIC			0.5039 BASIC		
E	14.95	15.00	15.05	0.5886	0.5906	0.5925
E1	12.80 BASIC			0.5039 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0137	0.0157	0.0175
aaa	0.15			0.0059		
bbb	0.25			0.0098		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

14. Revision History

Doc. Rev	Comments	Change Request Ref.
6289CS	**Product Overview:** "Features" on page 1, removed mid-level Embedded Trace Macrocell feature "Features" on page 1, updated figures on CPU speed "Features" on page 1, updated SDIO and MMC version Removed paragraph Section 5.2 "Power Consumption". Section 6.5 "Shutdown Logic Pins", removed information on the shutdown pin Section 8.1.2.1 "BMS = 1, boot on embedded ROM", – SDCard, (boot ROM does not support high capacity SDCards) clarification added.	 6142 RFO 6345 6345 6345 5935
6289BS	"Features" "Debug Unit (DBGU)" on page 2, updated Figure 8-1 "AT91SAM9R64/RL64 Memory Mapping", Internal Memory Mapping updated. Table 7-2, "List of Bus Matrix Slaves", Table 7-3, "AT91SAM9R64/RL64 Master to Slave Access", Slave 3 updated. Section 5.1 "Power Supplies", updated with caution on VDDCORE and VDDIO constraints Section 5.1.1 "USB Power Supply Considerations" and Figure 5-1 added to datasheet. Section 5.2 "Power Consumption", first two sentences updated. Table 3-1, "Signal Description List", additional comments on BMS. SHDN comments updated. Table 10-3 and Table 10-7 PB8, PB9 Peripheral A column: typos corrected, "CFCE1", "CFCE2".	5846 5276 5291 5420 5388 5423 rfo 5788
6289AS	First issue	