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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA, USB Core
Core Processor	Spartan-6 LX-45
Co-Processor	Cypress EZ-USB FX2LP
Speed	100MHz
Flash Size	8MB
RAM Size	128MB
Connector Type	B2B
Size / Dimension	1.6" x 1.9" (40.5mm x 47.5mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0630-01i

Table of Contents

1 Technical Specifications

1.1 Module options

FPGA options

Module can be ordered with Spartan-6 XC6SLX45, XC6SLX75, XC6SLX100, XC6SLX150 chip[1].

Temperature grade options

Module can be ordered in commercial or in extended (from -25 C° to +85 C°) temperature grade.

1.2 Dimensions

Figure 1 shows main module dimensions from top view.

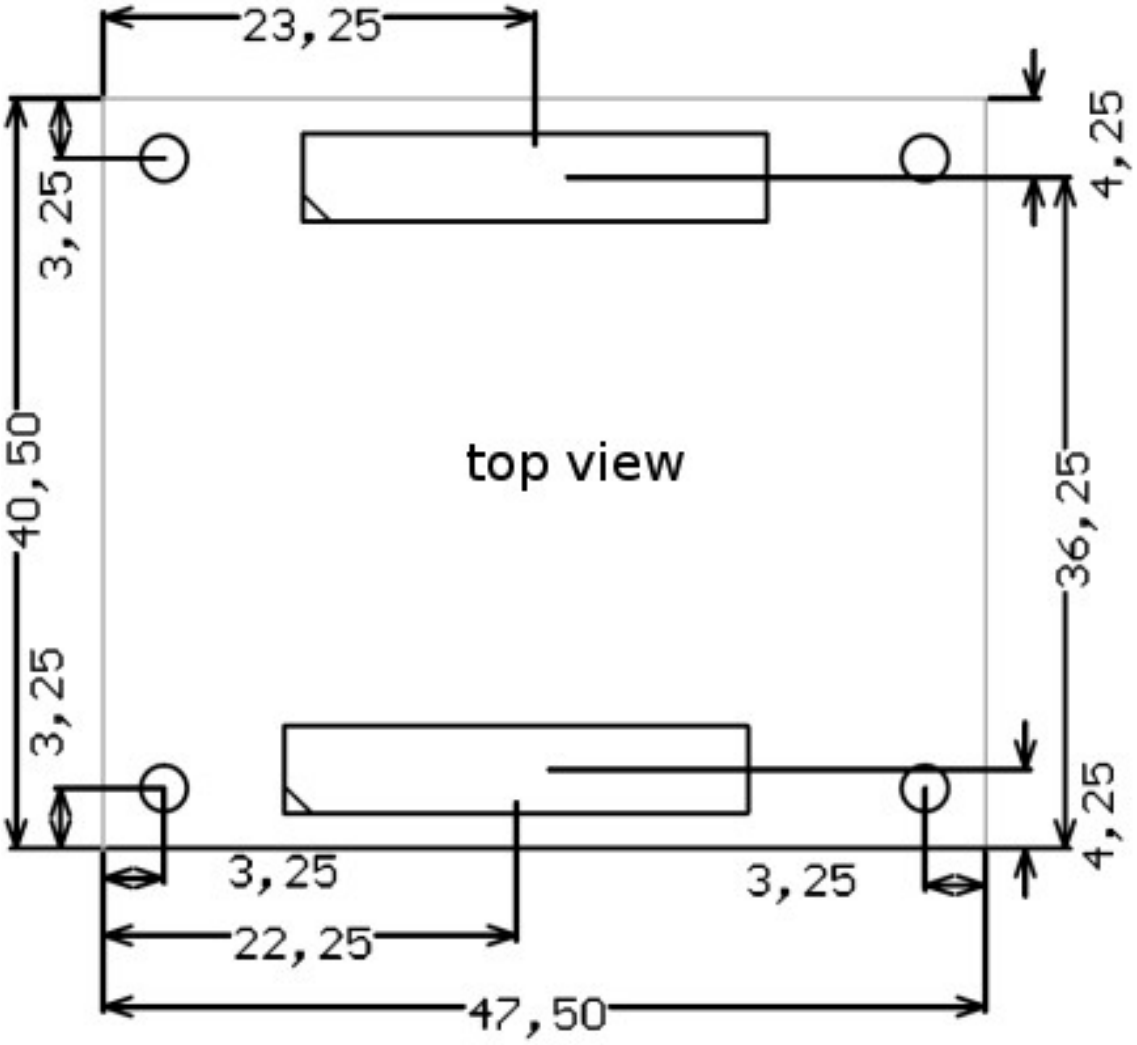


Figure 1: Module dimensions in mm

Mounting hole diameter is 3.2 mm.

1 Contact Trenz Electronic support for availability

2 Detailed Description

2.1 Block Diagram

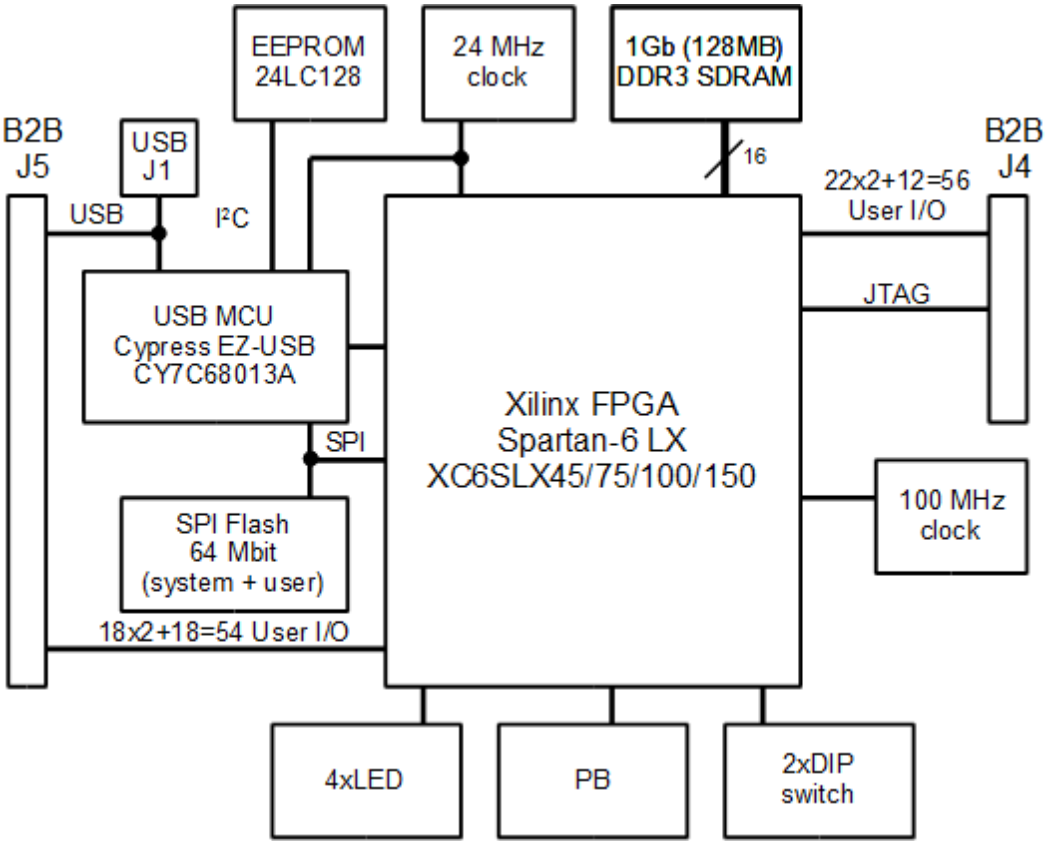


Figure 2: TE0630 block diagram

2.2 Power Supply

The module can be powered by B2B connector J5 or the USB connector. If both power supplies are available, the B2B connector power supply takes precedence, disabling the USB power supply automatically.

2.2.1 Supply from B2B Connector

The B2B connector power supply requires a single nominal 5 V DC power supply. The power is usually supplied to the module through the 5 V contacts (5Vb2b) of B2B connector J5 (see chapter 6.4 J5 Pin-out). The recommended minimum supply voltage is 4 V. The maximum supply voltage is 5.5 V. The recommended maximum continuous supply current is 1.5 A.

2.2.2 Supply from USB Connector

The module is powered by the USB connector if the following conditions are met:

- the module is equipped with an USB connector,
- the module is connected to a USB bus,

- no power supply is provided by B2B connectors.

In this case, other components (e.g. extension or carrier boards) may also be powered by the corresponding 5 volt line (5V) of B2B connector J5.

2.2.3 On-board Power Rails

Three on-board voltage regulators provide the following power supply rails needed by the components on the module:

- 1.2V, 3.0 A max
- 2.5V, 0.8 A max
- 3.3V, 3.0 A max
- 1.5V, 1.0 A max

Figure 3 show power supply diagram.

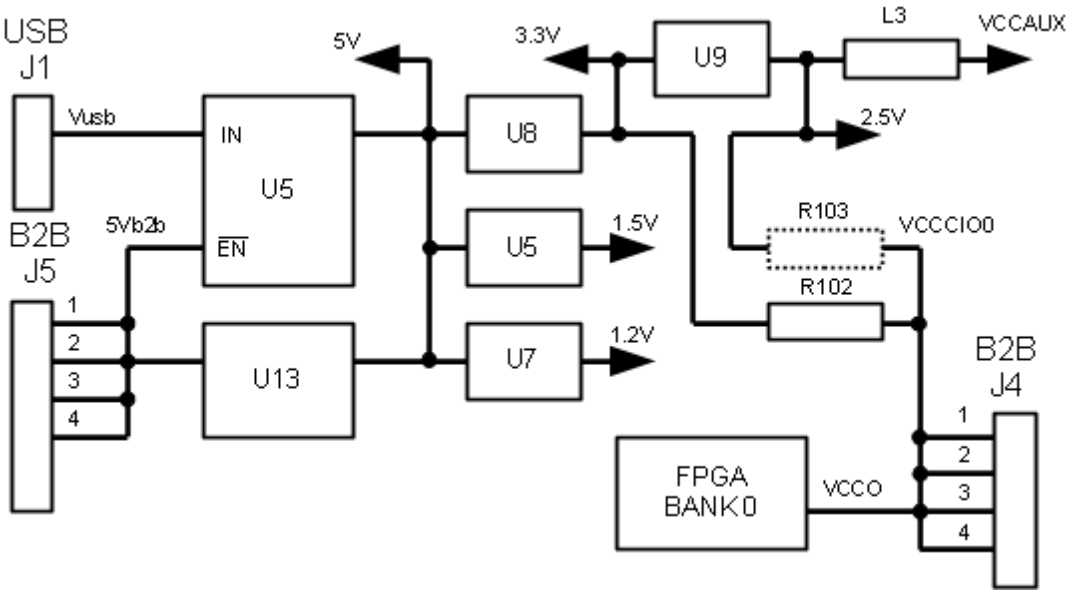


Figure 3: TE0630 Power diagram

The power rails are available for the FPGA and can be shared with a carrier board by the **corresponding** lines of the B2B connectors J4 and J5. Please note that the **power consumption of the FPGA is highly dependent on the design actually loaded.** So please use a tool like Xilinx Xpower to estimate the expected power consumption of your design.

Even if the provided voltages of the module are not used on the carrier board, it is recommended to bypass them to ground with 10 nF - 100 nF capacitors.

FPGA I/O banks power supply

Spartan-6 architecture organizes I/Os into four I/O banks, see Table 1 for supply voltage used for each bank.

VCCIO0 voltage can be configured in 3 ways:

- **2.5V** - When resistor **R103 is populated** and resistor **R102 is not populated**.
- **3.3V** - When **R103 is not populated** and resistor **R102 is populated**.

- **External supply** - When **R103 is not populated** and **R102 is not populated**. In this case external supply source have to be connected to pins 1, 2, 3, 4 of J4 B2B connector[2].

Others options of VCCIO0 power supply are not supported and can damage the FPGA!

See Figure 4 to locate R102 and R103 on PCB.

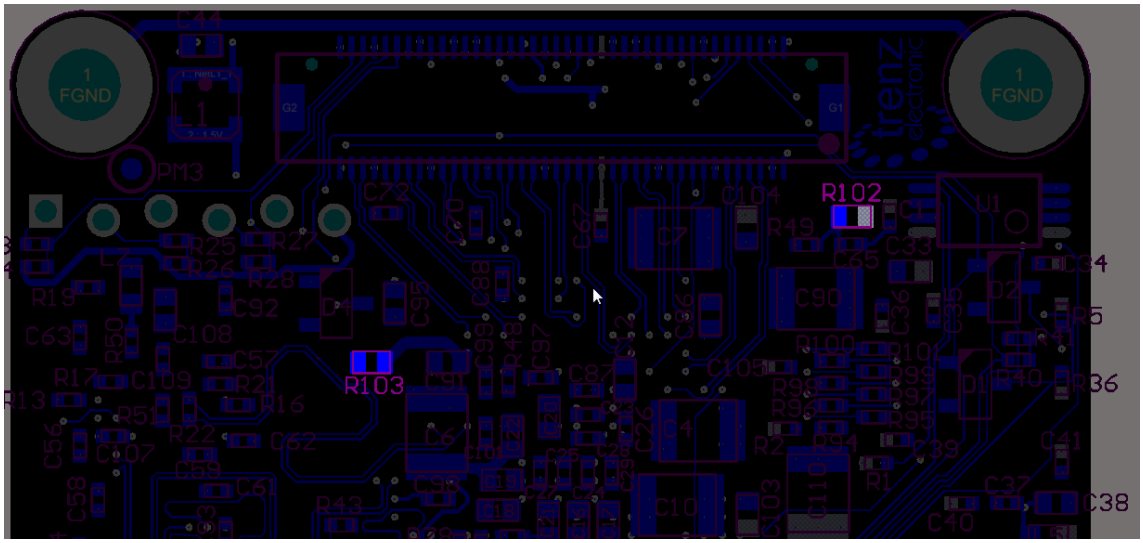


Figure 4: R102 and R103 location

Bank	Supply Voltage
B0	VCCIO0
B1	1.5V
B2	3.3V
B3	3.3V

Table 1: FPGA banks VCCIO power supply

Note that some of Spartan-6 I/O types are partially compatible, so pins of compatible types can be used as inputs for signal of other type. See “Spartan-6 FPGA SelectIO Resources” page 38 for detailed information.

2.2.4 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the supply rail remains below the threshold voltage(2.93 volt). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset prior to a regular system start-up. The typical delay time t_d of 200 ms starts after the supply rail has risen

2 See Spartan-6 documentation fo VCCIO power range.

Figure 8: Mating (carrier board) connector

Supplier	Header
Digikey	H11148DKR-ND H11148TR-ND H11148CT-ND
Hirose	DF17(4.0)-80DP-0.5V(57)
Trenz Electronic	22938

Table 5: Carrier board headers part numbers.

Figure 9 shows the definition of stacking height featured by the combination of the TE0630 receptacle with its corresponding header.

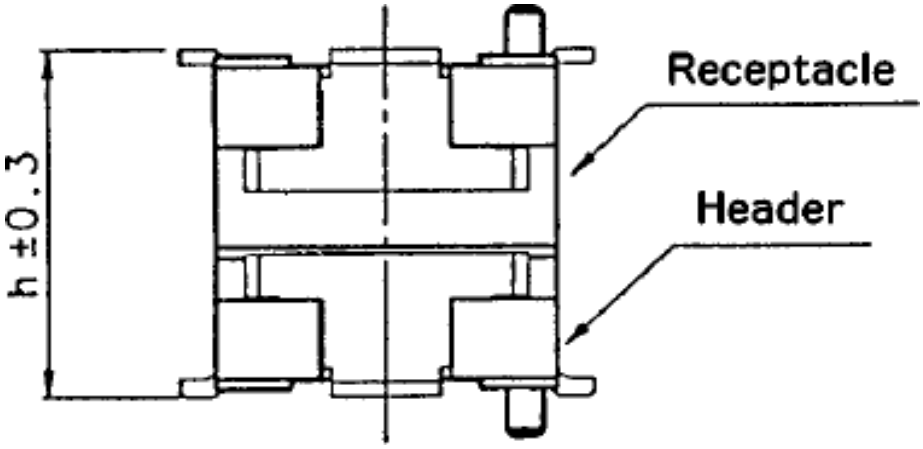


Figure 9: B2B stacking

The stacking height of the TE0630 B2B connectors is 7 (seven) mm. The stacking height does not include the solder paste thickness.

2.5 USB Connector

The module uses a mini-USB (B type) receptacle connector.

Figure 10: Mini-USB connector

2.6 JTAG connector

The offset holes of header J2 allow a removable press fit of standard 0.100 inch header pins to connect flying leads without any soldering necessary. JTAG signals are available on the dedicated header J2 through a JTAG programmer with flying leads as described in Table 6.

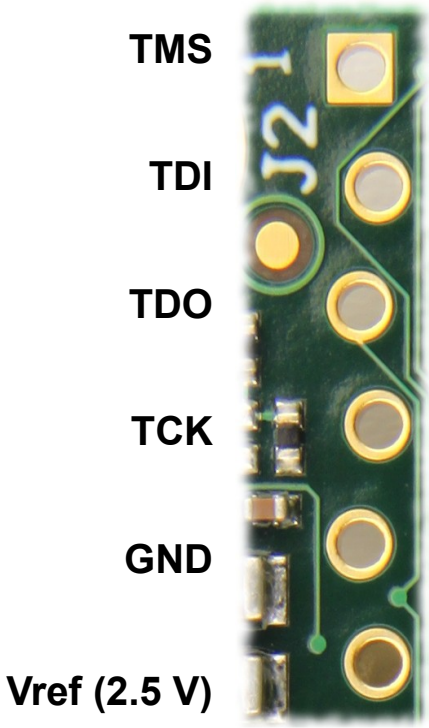


Table 6: JTAG header J2 pin-out

2.7 Serial EEPROM

TE0630 is equipped with a Micron Technology 24LC128 128 K I^2C CMOS Serial EEPROM (U1). It is used for EZ-USB FX2 firmware, vendor ID and device ID storage. EEPROM is accessible through the EZ-USB FX2 microcontroller.

2.8 SPI Flash

TE0630 is equipped with a Winbond W25Q64BV 64 Mb (8 MB) serial flash memory chip (U14). This serial flash chip can operate as general SPI memory mode and in double or quad modes. Usage of dual and quad modes increase bandwidth up to 40 MB/s. For more information see Winbond W25Q64BV product owerview.

Signal name	FPGA pin
BR0	R19
BR1	V19
BR2	V20
BR3	T17

Table 12: Board revision pins

To define low (zero) level BR pin connected to ground rail, to define high (one) level BR pin left float (open). These pins should be configured with "pullup" option in user design.

See Table 12 for current list of board revisions.

BR3	BR2	BR1	BR0	
0	0	0	0	00 Initial revision

Table 13: Board revisions

Module assembly variant encoded using AV[3:0] pins.

Signal name	FPGA pin
AV0	Y20
AV1	R15
AV2	R16
AV3	R17

Table 14: Assembly variants pins

To define low (zero) level AV pin connected to ground rail through zero resistor, to define high (one) level AV pin left float (open). These pins should be configured with "pullup" option in user design.

Available module assembly variants listed in Table 15.

AV3	AV2	AV1	AV0	
0	0	0	0	Base assembly variant

Table 15: Module assembly variants

3 TE0300 compatibility

TE0630 module designed to be compatible with TE0300 board by main mechanical and electrical characteristics.

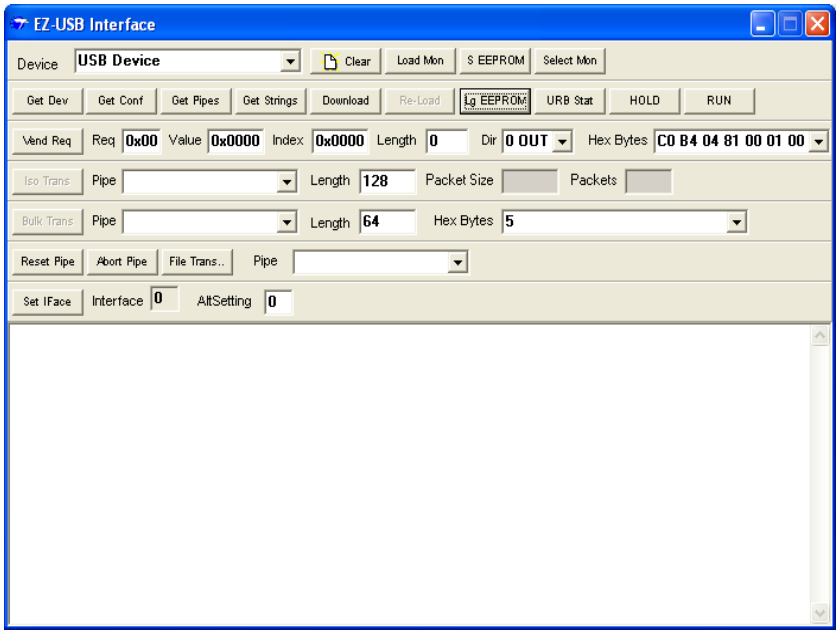
3.1 Mechanical compatibility

Both modules have the same board dimensions. TE0630 mount holes and B2B connectors locations are match with TE0300. See chapter 1.2 Dimensions for detailed information.

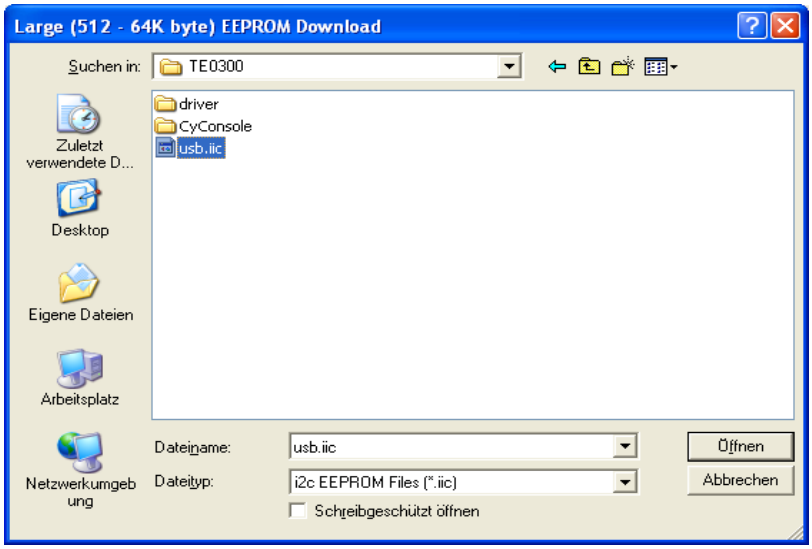
TE0300 and TE0630 uses same B2B connectors types. In chapter 2.4 Board-to-board Connectors you can find B2B connectors part numbers and main characteristics.

3.2 Electrical compatibility

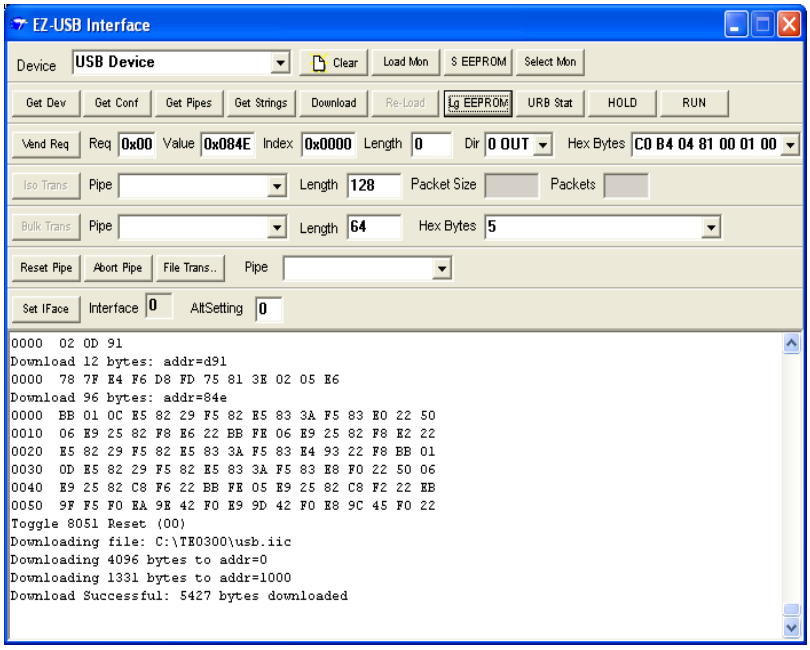
TE0300 and TE0630 have similar power requirements and matched power input pins. User signals to B2B connectors routed as differential pairs and single



"S EEPROM" button refers to the small EEPROM (256 bytes) whereas the "Lg EEPROM" refers to the large EEPROM (64 KB). Press the "Lg_EEPROM" button, select the "USB.iic" file and press the "Open" button to start writing to EEPROM.



Upgrade progress is displayed in status window and is completed when "Download Successful" text is displayed.



After that EEPROM will contain right VID/PID. To apply changes reconnect USB cable.

5 USB Drivers Installation

To provide convenient interface from host computer to TE0630 module, USB driver should be installed to operating system. There is 2 drivers to work with TE0630 module:

- Generic driver, which work with default controller configuration.
- Dedicated driver, which works with custom FX2 firmware.

Generic driver used only for initial USB microcontroller programming and **not needed for normal work flow**.

Most TE0630 users **need to install only dedicated driver** see chapter 5.2 Dedicated Driver.

5.1 Generic Driver

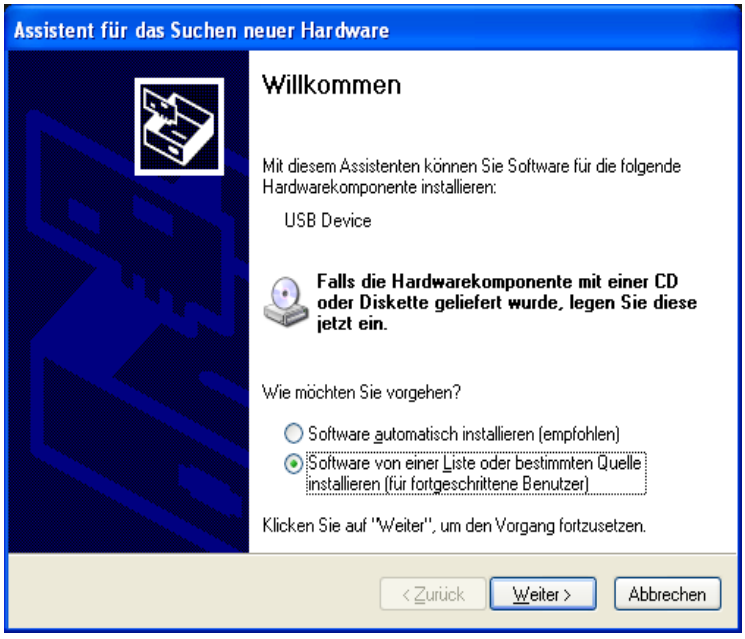
Most **users don't need this driver**, this driver used only for initial USB microcontroller programming, which was already done for all supplied TE0630 modules.

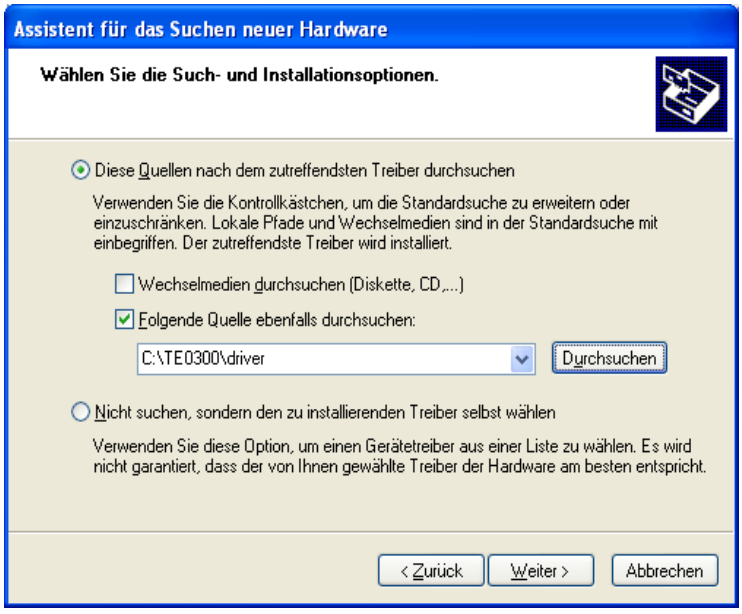
If the USB microcontroller (Cypress EZ-ESB FX2) driver is not installed on the host computer, then the easiest way to do it is the following:

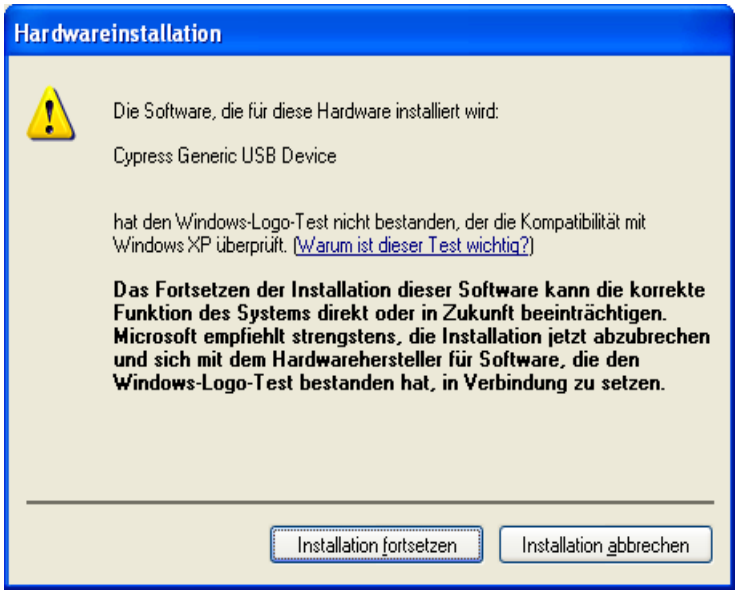
- disconnect the module if it connected or leave the module unconnected;
- configure the module such that the USB microcontroller will provide its default vendor ID and device ID to the USB host (i.e. Switch 1 (S1A) = "OFF" -- see chapter 4.4 EZ-USB FX2 Firmware Programming);
- connect the module to the host computer through the USB interface;
- wait until the operating system detects new hardware and starts the

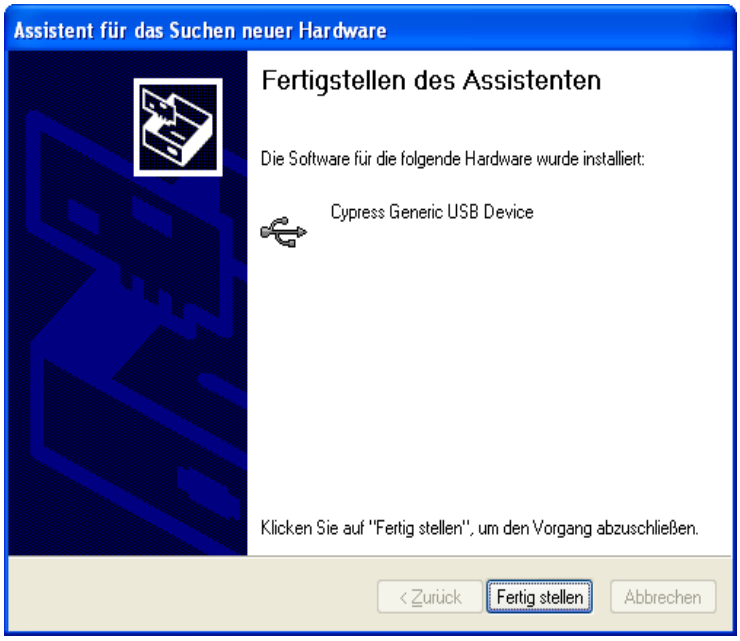
hardware assistant;

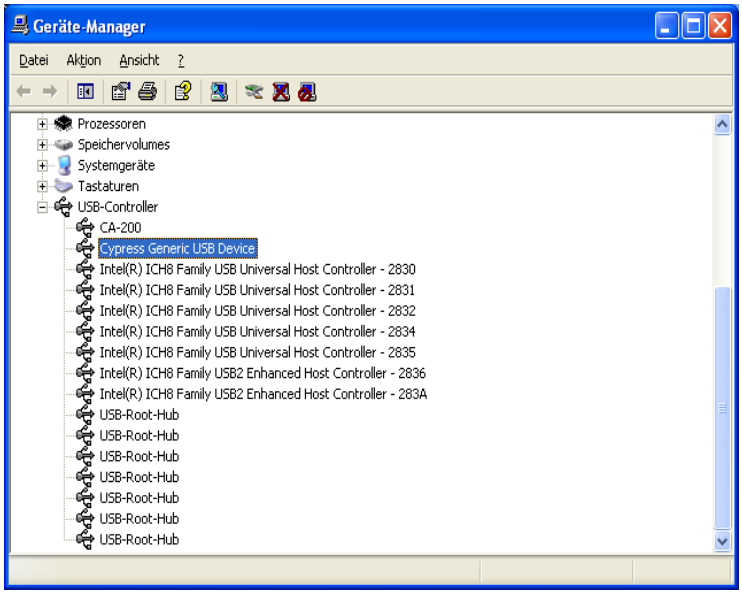
- put Switch 1 (S1A) to "ON" (EEPROM connected to USB microcontroller);
- answer the hardware assistant questions as shown in the following example.






Hardwareinstallation
Die Software, die für diese Hardware installiert wird:
Cypress Generic USB Device
hat den Windows-Logo-Test nicht bestanden, der die Kompatibilität mit Windows XP überprüft. (Warum ist dieser Test wichtig?)
Das Fortsetzen der Installation dieser Software kann die korrekte Funktion des Systems direkt oder in Zukunft beeinträchtigen. Microsoft empfiehlt strengstens, die Installation jetzt abzubrechen und sich mit dem Hardwarehersteller für Software, die den Windows-Logo-Test bestanden hat, in Verbindung zu setzen.
Installation fortsetzen
Installation abbrechen


Assistent für das Suchen neuer Hardware
Fertigstellen des Assistenten
Die Software für die folgende Hardware wurde installiert:
Cypress Generic USB Device
Klicken Sie auf "Fertig stellen", um den Vorgang abzuschließen.
< Zurück
Fertig stellen
Abbrechen



After that I^2C EEPROM should be programmed with right Vendor ID / Device ID, see chapter 4.5 EZ-USB FX2 EEPROM Programming.

5.2 Dedicated Driver

This driver used to work with modules which have DEWESoft firmware and Vendor ID / Device ID programmed. All TE0630 modules supplied with programmed USB controller and corresponding Vendor ID / Device ID in EEPROM.

Before connect USB cable, check that Switch 1 (S1A) is on "ON" state (USB controller connected to EEPROM).

Connect USB cable and wait until the operating system detects new hardware and starts the hardware assistant and answer the hardware assistant questions as shown in the following example.

6.1 Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "Vx_IO_yy_p" naming convention, where:

- Vx defines the FPGA bank (x = bank number);
- IO defines an "FPGA to B2B" signal type;
- yy defines a differential pair or signal number (yy = pair number);
- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Remaining signals use custom names.

6.2 Pin Types

Most pins of B2B connectors J1 and J2 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 5 different functional types of pins on the TE0630, as outlined in Table 20. In pin-out tables Table 21 and Table 22, the individual pins are colour-coded according to pin type as defined in Table 20.

type colour code	description
DIO	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CIO	Unrestricted, general-purpose differential user-I/O pin. This pin also can be used as FPGA clock input.
USB	USB signals.
JTAG	Dedicated JTAG signals.
GND	Dedicated ground pin. All must be connected.
SYS	System signal. See the description of each pin in the user manual for additional information on the corresponding signals.
POW	Power signals.

Table 20: TE0630 pin types

6.5 Signal Integrity Considerations

Traces of differential signals pairs are routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length[6]. For applications where traces length has to be matched or timing differences have to be compensated, Table 21 and Table 22 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 100 ohm. Single ended traces are routed with 60 ohm impedance.

An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

7 Related Materials and References

The following documents provide supplementary information useful with this user manual.

7.1 Data Sheets

- Winbond W25Q64BV product overview.

  http://www.winbond.com.tw/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/W25Q64BV.htm

- Xilinx DS160: Xilinx Spartan-6 Family overview

  http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf

- Cypress EZ-USB FX2 Controller datasheet

  http://www.cypress.com/?mpn=CY7C68013A-56LTXC

7.2 User Guides

- Xilinx UG380: Spartan-6 FPGA Configuration User Guide

  http://www.xilinx.com/support/documentation/user_guides/ug380.pdf

- Xilinx UG381: Spartan-6 FPGA SelectIO Resources

  http://www.xilinx.com/support/documentation/user_guides/ug381.pdf

8 Glossary of Abbreviations and Acronyms

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

6 Difference in signal lines length is negligible for used signal frequency.

Appendix A. Indirect SPI Programming using iMPACT

To indirect program SPI Flash using Xilinx iMPACT do following steps:

Connect JTAG cable to corresponding module connector (see 2.6 JTAG connector).

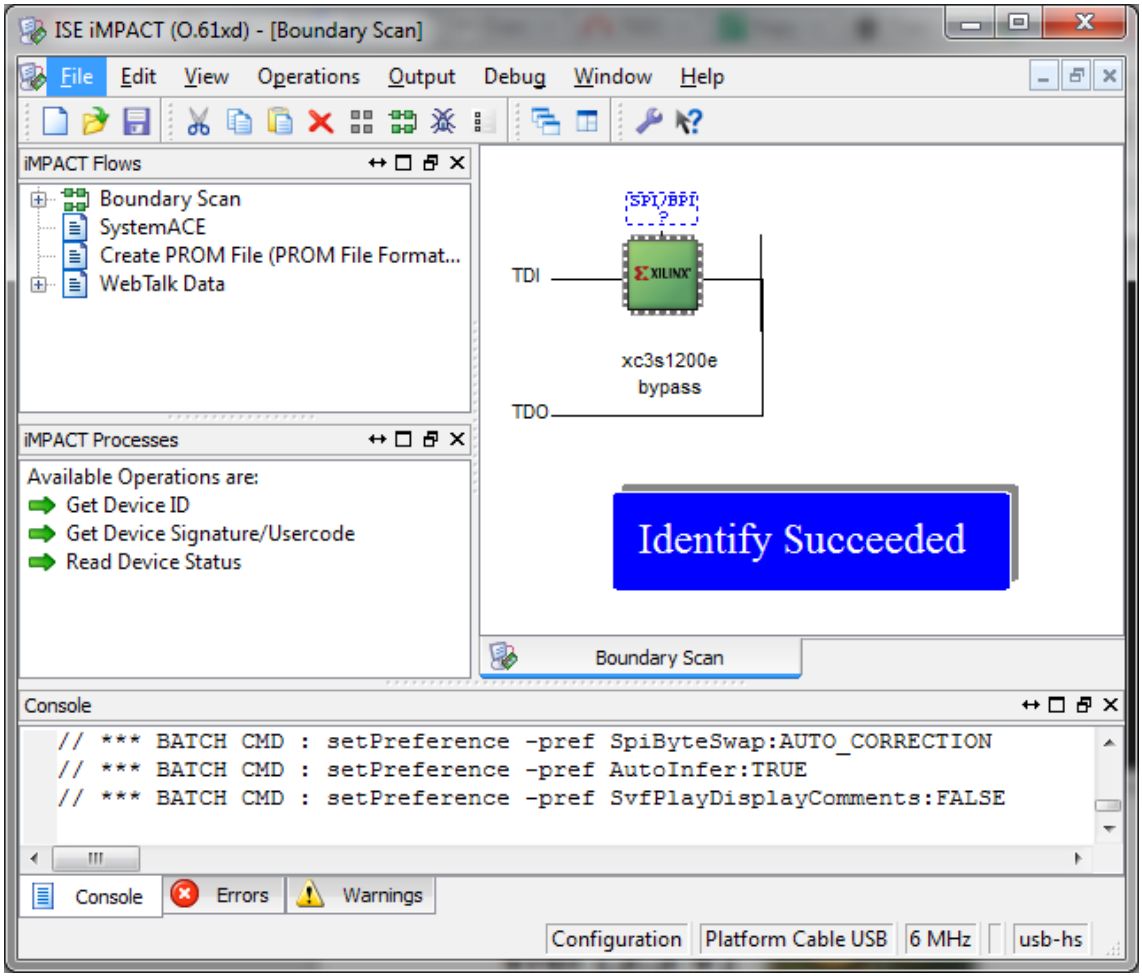
Connect JTAG cable to host computer with installed Xilinx iMPACT software.

Power-on module by external power supply source or by USB cable.

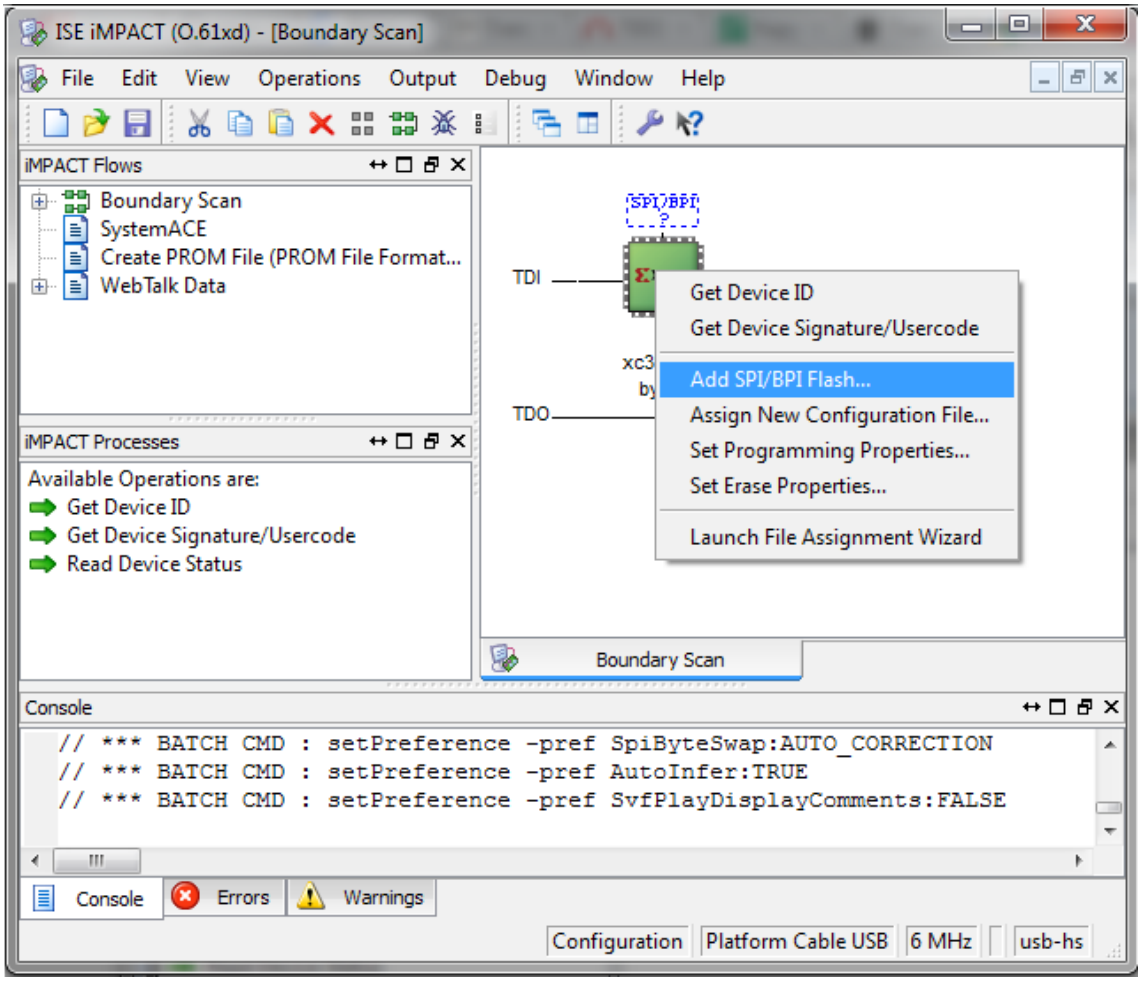
Run Xilinx iMPACT.

Select Boundary Scan mode.

After initialization iMPACT window should look like

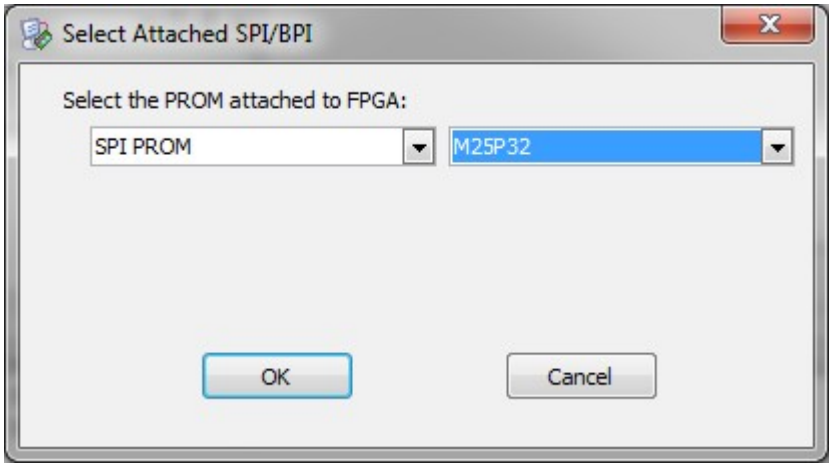


Right click on FPGA image and select “Add SPI/BPI Flash...” from menu.



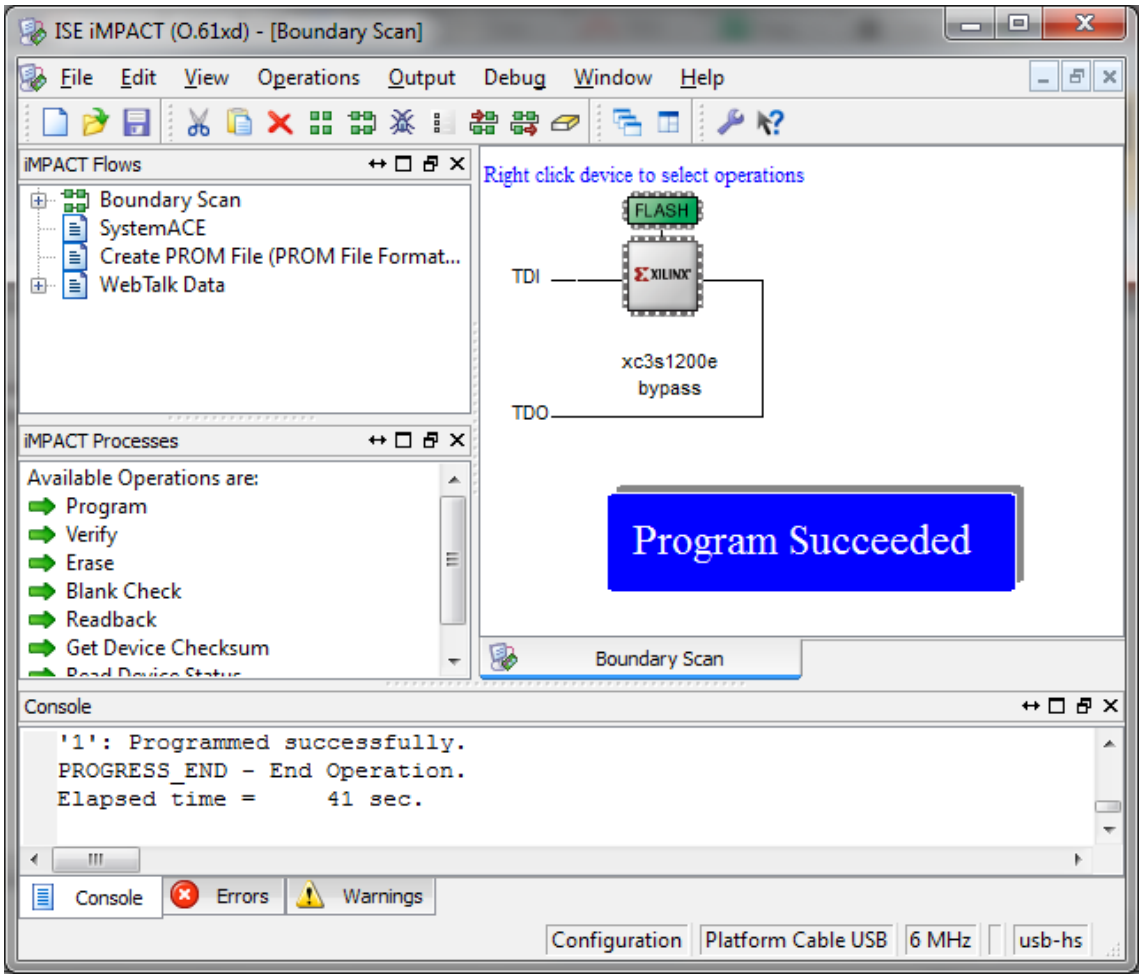
Select mcs file to program.

Select SPI Flash type corresponding to your module type and revision.



Right click on Flash image and select “Program” from menu.

After completion iMPACT window should show “Program Succeeded” sign.



Document Change History

ver.	date	author	description
0.01	07.10.11	AIK	Release.
0.02	08.10.11	AIK	Added block diagram and few sections.
0.03	10.10.11	AIK	Added USB controller section with pin-out.
0.04	12.10.11	FDR	First general review.
0.05	13.10.11	AIK	Fixes after review. Add power diagram.
0.06	17.10.11	AIK	Add USB driver section.
0.07	17.10.11	AIK	Additions to configuration section.
0.08	16.11.11	AIK	Added module photos.
0.09	17.11.11	AIK	Net length information.
0.10	21.11.11	AIK	TE0300 compatibility information
0.11	22.11.11	AIK	Additional information to compatibility chapter
0.12	30.11.11	AIK	Added eFUSE programming section
0.13	01.12.11	AIK	Adder board revision and assembly variant chapter
0.14	20.01.12	AIK	Added pin compatibility note and manual reference.
0.15	25.01.12	AIK	Added R102 R103 location image. Added Appendix A.
0.16	16.02.12	AIK	Module options chapter
0.17	05.09.12	AIK	Fixed JTAG Vref
0.18	12.09.12	AIK	Fixed net length table
0.19	27.11.12	AIK	Fixed J4 user pin count
0.20	13.03.13	AIK	Fixed Table 7
0.21	03.07.13	AIK	Fixed pin count