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**Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules**

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

**Applications of Embedded - Microcontroller,**

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Module/Board Type | FPGA, USB Core |
| Core Processor | Spartan-6 LX-75 |
| Co-Processor | Cypress EZ-USB FX2LP |
| Speed | 100MHz |
| Flash Size | 8MB |
| RAM Size | 128MB |
| Connector Type | B2B |
| Size / Dimension | 1.6" x 1.9" (40.5mm x 47.5mm) |
| Operating Temperature | -40°C ~ 85°C |
| Purchase URL | https://www.e-xfl.com/product-detail/trenz-electronic/te0630-01ibf |

# 1 Technical Specifications

## 1.1 Module options

**FPGA options**

Module can be ordered with Spartan-6 XC6SLX45, XC6SLX75, XC6SLX100, XC6SLX150 chip[1].

**Temperature grade options**

Module can be ordered in commercial or in extended (from -25 C° to +85 C°) temperature grade.

## 1.2 Dimensions

Figure 1 shows main module dimensions from top view.

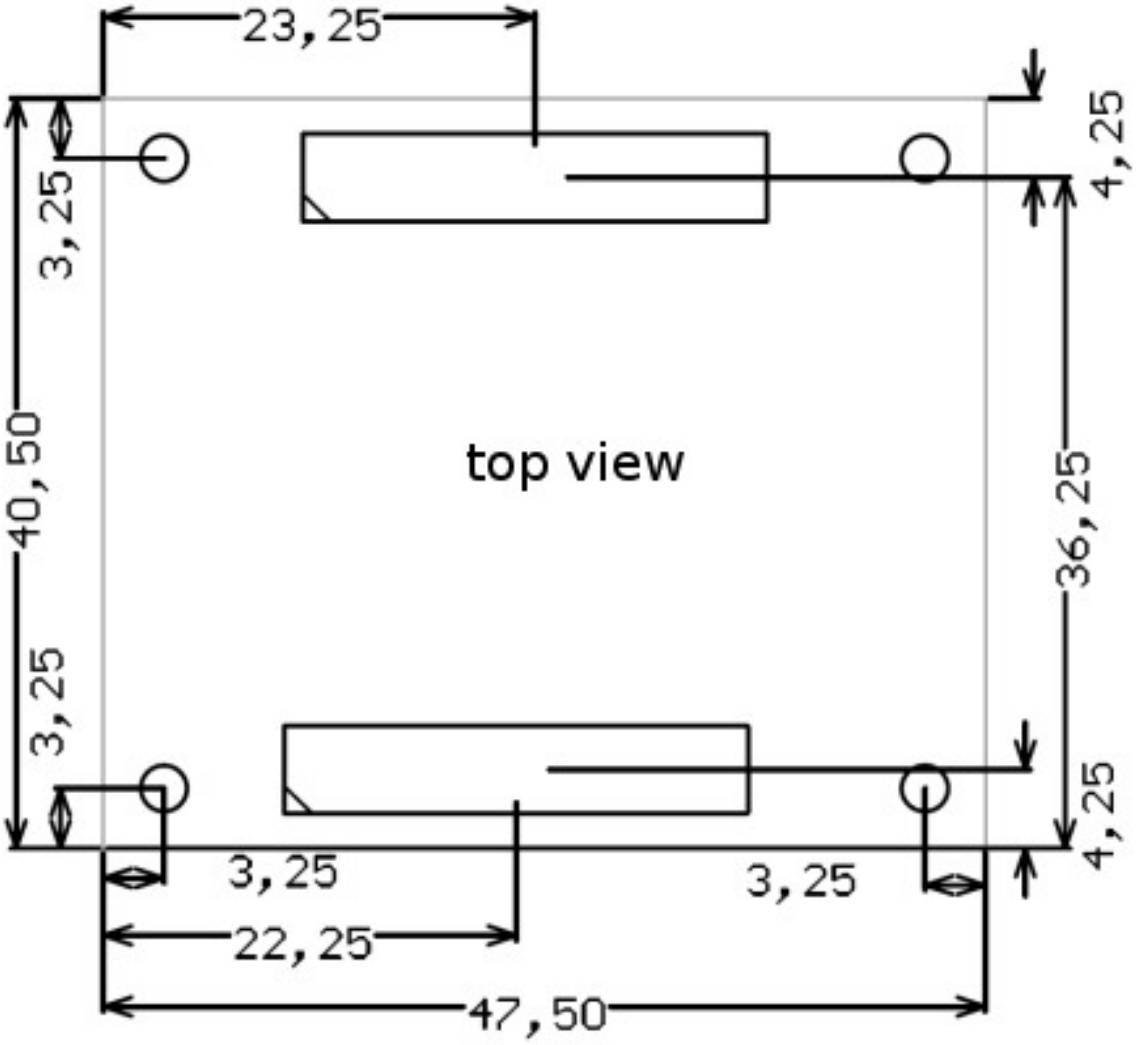



**Figure 1: Module dimensions in mm**

Mounting hole diameter is 3.2 mm.

1 Contact Trenz Electronic support for availability

- **External supply** - When **R103 is not populated** and **R102 is not populated**. In this case external supply source have to be connected to pins 1, 2, 3, 4 of J4 B2B connector[2].


**Others options of VCCIO0 power supply are not supported and can damage the FPGA!**

See Figure 4 to locate R102 and R103 on PCB.

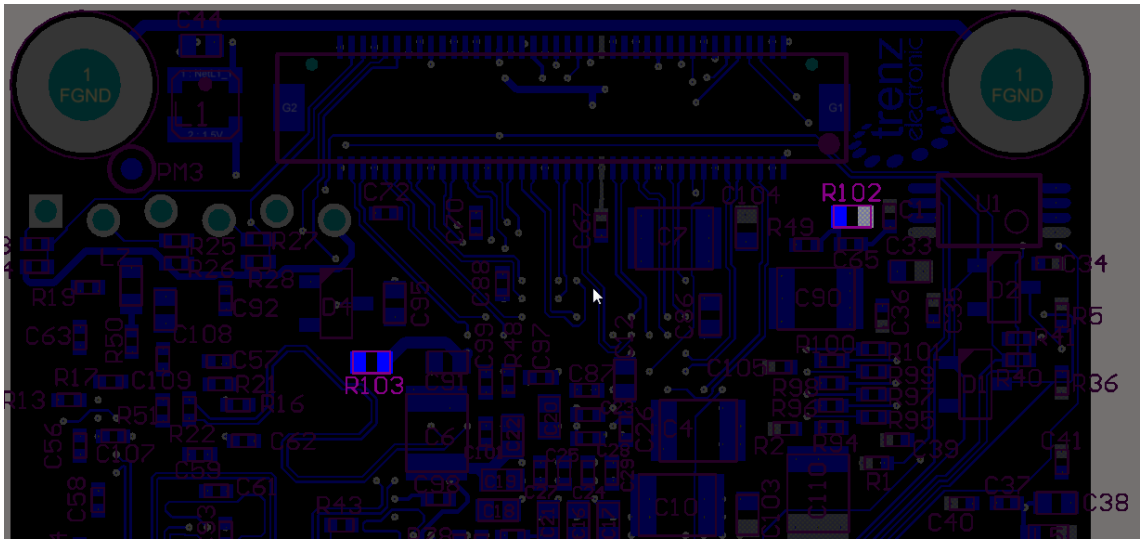



**Figure 4: R102 and R103 location**

| Bank | Supply Voltage |
|---|---|
| B0 | VCCIO0 |
| B1 | 1.5V |
| B2 | 3.3V |
| B3 | 3.3V |

**Table 1: FPGA banks VCCIO power supply**

Note that some of Spartan-6 I/O types are partially compatible, so pins of compatible types can be used as inputs for signal of other type. See “Spartan-6 FPGA SelectIO Resources” page 38 for detailed information.

## 2.2.4 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the supply rail remains below the threshold voltage(2.93 volt). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset prior to a regular system start-up. The typical delay time $t_d$ of 200 ms starts after the supply rail has risen

2 See Spartan-6 documentation fo VCCIO power range.

above the threshold voltage.

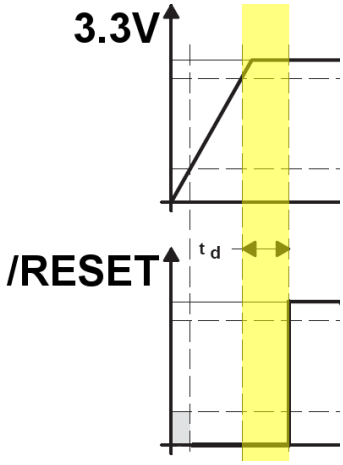



**Figure 5: Reset on power-on**

After this delay, the /RESET line is reset (high) and the FPGA configuration can start. When the supply rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again and stays active (low) as long as the rail voltage remains below the threshold voltage (2.93 volt). Once the rail voltage raises again and remains over the threshold voltage for more than the typical delay time $t_d$ of 200 ms, the /RESET line returns to the inactive state (high) to allow a new system start-up.

## 2.3 FPGA User I/Os

TE0630 provides user I/O signals connected to B2B connectors J4 and J5. There are 3 types of user I/O signals:

- Single ended;
- Differential pairs (each pair is configurable as 2 single-ended digital I/Os);
- Differential pairs, which can be used as clock inputs (each pair can be used as usual differential pair or 2 single-ended digital I/Os).

Table 2 show user I/O count for J4 and J5.

| | J4 | J5 | Total |
|---|---|---|---|
| Single ended | 12 | 18 | 30 |
| Differential | 18 | 16 | 34 |
| Differential (clock) | 4 | 2 | 6 |
| Total | 56 | 54 | 110 |

**Table 2: User I/O count by connector**

Table 3 show user I/O divided by VCCIO supply voltage.

| | VCCIO0 | 3.3V | Total |
|---|---|---|---|
| Single ended | 1 | 29 | 30 |
| Differential | 18 | 16 | 34 |
| Differential (clock) | 4 | 2 | 6 |
| Total | 45 | 65 | 110 |

**Table 3: User I/O count by VCCIO**

## 2.4 Board-to-board Connectors

The module has two B2B (board-to-board) receptacle connectors (J4 and J5) for a total of 160 contacts. Figure 6 shows B2B connectors location on board; USB connector is located on the top side and is shown to define module position.

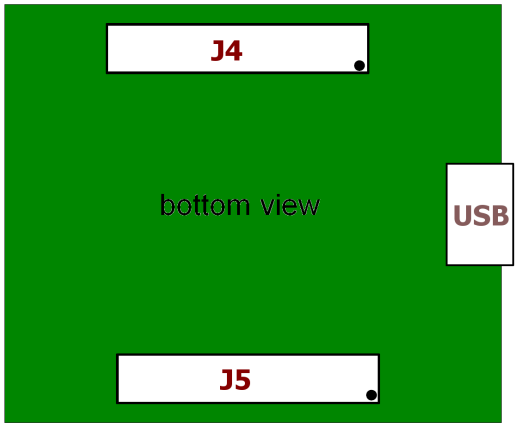



**Figure 6: B2B connectors location**

TE0630 uses high-density shockproof connectors shown in Figure 7. Connector part numbers are listed in Table 4.

**Figure 7: Module connector**

| Supplier | Header |
|---|---|
| Digikey | H11113CT-ND<br>H11113TR-ND<br>H11113DKR-ND |
| Hirose | DF17(3.0)-80DS-0.5V(57) |
| Trenz Electronic | 22684 |

**Table 4: Module connectors part numbers**

The on-board receptacles mate with their corresponding headers on the carrier board shown in Figure 8. Ordering numbers of mating connectors are listed in Table 5.

| Signal name | FPGA pin | LED |
|---|---|---|
| U_LED1 | F1 | D3 |
| U_LED2 | F2 | D5 |
| U_LED3 | J4 | D6 |
| U_LED4 | K8 | D7 |

**Table 9: LEDs pin-out**

## 2.13 Push-Button

TE0630 module is equipped with one active-high push-button (signal is set to logical "1" when button is pressed). Table 10 show push-button connection details.

| Signal name | FPGA pin | PB |
|---|---|---|
| PB | R7 | S5 |

**Table 10: Push button pin-out**

## 2.14 DIP Switch

On-board 4xDIP switch S1 used for system and user settings.

Switch 1 (S1A) is used to connect the USB controller to the $I^2C$ serial EEPROM. When S1A is "ON", serial $I^2C$ EEPROM is connected to the USB controller, when switch is "OFF", the USB controller is disconnected from the EEPROM[4]. Turn S1A off when programming the USB EEPROM (storing the USB vendor ID and device ID). This will force the USB controller to provide its default vendor ID and device ID.

Switch 2 (S1B) is used to control DC-DC converters. When switch is "OFF", converters are controlled by the USB controller. When switch is "ON", converters are enabled regardless of USB controller actions. At start-up, the USB controller switches off 1.2V, 1.5V and 2.5V power rails and starts up the module in low-power mode. After enumeration, the USB controller firmware switches the 1.2V, 1.5V and 2.5V power rails on, if enough current is available from the USB bus.

Switches 3 (S1C) and 4 (S1D) can be used as user switches. Switches are active-low. Pull-up resistors should be defined in user constrains file (UCF) to use this switches in FPGA design. See Table 11 for details.

| Signal name | FPGA pin | Switch |
|---|---|---|
| IO_L61_N_1 | AB21 | S1C |
| IO_L63_N_1 | AA22 | S1D |

**Table 11: DIP switch pin-out**

## 2.15 Board revisions and assembly variants

To determine PCB revision and assembly variant from FPGA, TE0630 have dedicated user signals, which can be read by user core.

Board revision coded in 4 bits BR[3:0]

4 Zero-resistor R90 (not populated by default) short this switch and connect EEPROM regardless of S1A position.

ended lines. Differences in pin types shown in Table 16, not listed signals have same or compatible[5] type.

| Connector:Pin | TE0300 pin name | TE0300 Type | TE0630 pin name | TE0630 Type |
|---|---|---|---|---|
| J4:5 | B3_L01_P | DIO | V3_IO_01 | SIO |
| J4:7 | B3_L01_N | DIO | V3_IO_02 | SIO |
| J4:9 | B3_L02_P | DIO | V3_IO_03 | SIO |
| J4:11 | B3_L02_N | DIO | V3_IO_04 | SIO |
| J4:17 | B0_L24_N | DIO | V0_IO_01 | SIO |
| J4:19 | B0_L24_P | DIO | V0_IO_01_N | DIO |
| J4:6 | B3_L07_P | DIO | V3_IO_06 | SIO |
| J4:8 | B3_L07_N | DIO | V3_IO_07 | SIO |
| J4:10 | B3_L03_N | DIO | V3_IO_08 | SIO |
| J4:12 | B3_L03_P | DIO | V3_IO_09 | SIO |
| J5:13 | B3_L22_P | DIO | V3_IO_12 | SIO |
| J5:15 | B3_L22_N | DIO | V3_IO_13 | SIO |
| J5:19 | B3_L20_P | DIO | V3_IO_14 | SIO |
| J5:21 | B3_L20_N | DIO | V3_IO_15 | SIO |
| J5:16 | B3_L21_N | DIO | V3_IO_17 | SIO |
| J5:18 | B3_L21_P | DIO | V3_IO_18 | SIO |
| J5:20 | B3_L23_N | DIO | V3_IO_19 | SIO |
| J5:22 | B3_L23_P | DIO | V3_IO_20 | SIO |
| J5:32 | B2_L06_P | DIO | V3_IO_24 | SIO |
| J5:34 | B2_L06_N | DIO | V3_IO_25 | SIO |
| J5:41 | B2_GCLK13 | CIO | V2_IO_02 | SIO |
| J5:49 | B2_GCLK_L13_N | CIO | V2_IO_24_P | DIO |
| J5:51 | B2_GCLK_L13_P | CIO | V2_IO_24_N | DIO |

**Table 16: TE0300 and TE0630 pin types differences.**

See Table 17 for pin types definitions.

| Type colour code | Description |
|---|---|
| DIO | Unrestricted, general-purpose differential user-I/O pin. |
| SIO | Unrestricted, general-purpose user-I/O pin. |
| CIO | Unrestricted, general-purpose differential user-I/O pin. This pin also can be used as FPGA clock input. |

**Table 17: TE0300 and TE0630 pin types**

Most user signals to B2B connectors routed from same FPGA banks. Differences shown in Table 18.

5 Signals routed as differential pairs can be used as single ended.

| Connector:Pin | TE0300 Bank | TE0630 Bank |
|---|---|---|
| J4:15 | 0 | 3 |
| J4:36 | 0 | 3 |
| J4:52 | 0 | 3 |
| J5:33 | 2 | 3 |
| J5:28 | 2 | 3 |
| J5:30 | 2 | 3 |
| J5:32 | 2 | 3 |
| J5:34 | 2 | 3 |
| J5:38 | 2 | 3 |
| J5:40 | 3 | 2 |
| J5:42 | 3 | 2 |
| J5:50 | 3 | 2 |
| J5:52 | 3 | 2 |

**Table 18: TE0300 and TE0630 user signals I/O banks differences.**

I/O Banks power supply for both modules shown in Table 19.

| Bank | TE0300 | TE0630 |
|---|---|---|
| B0 | VCCIO (1.2 V - 3.3 V) | VCCIO (1.2 V - 3.3 V) |
| B1 | 2.5 V | 1.5 V |
| B2 | 3.3 V | 3.3 V |
| B3 | 3.3 V | 3.3 V |

**Table 19: TE0300 and TE0630 FPGA I/O banks power supply.**

Bank 0 I/O supply voltage at both modules can be configured by user, see chapter 2.2.3 On-board Power Rails.

# 4 Module Configuration

Full module configuration cycle (for just assembled board) include steps:

1. Generic USB driver installation
2. USB microcontroller large EEPROM programming
3. EEPROM programming
4. Dedicated driver installation
5. SPI Flash configuration

**Steps 1-3** already performed at Trenz Electronic laboratory, and **not required** to perform by end user.

To work with TE0630 module using USB interface user should install dedicated USB driver, which provide API to work with main module functions, for complete instructions see chapter 5.2 Dedicated driver installation.

The FPGA on the TE0630 can be configured by SPI Flash or by JTAG connector.

## *4.1 JTAG FPGA Configuration*

Programming using JTAG interface provide convenient and fast way to test FPGA project. FPGA configuration programmed this way is volatile and lost

after reset or power cycle.

## 4.2 SPI FPGA Configuration

The bit-stream for the FPGA is stored in the SPI Flash. To use this bit-stream source FPGA configuration option is set to “Master Serial/SPI”. See 2.8 SPI Flash for additional information.

SPI Flash can be programmed in several ways:

- Direct programming by USB controller (usually done by Firmware Upgrade Tool).
- Indirect SPI programming via FPGA pins, controlled by JTAG (can be done using Xilinx iMPACT). See Appendix A. Indirect SPI Programming using iMPACT.
- Direct SPI programming by FPGA, using an SPI core (FPGA project should contain SPI interface core and software to work with it).

In SPI Flash mode, the FPGA’s internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM’s Slave Clock input pin. The FPGA begins configuring using its lowest frequency setting. If so specified in the configuration bitstream, the FPGA increases the CCLK frequency to the specified setting for the remainder of the configuration process. The maximum frequency is specified using the ConfigRate bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. For TE0630 SPI Flash PROM, use ConfigRate = 12 or lower.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Configuration Options > Configuration Rate > 12 (or lower)

## 4.3 eFUSE programming

To program eFUSE at TE0630 module follow the steps below.

- Connect 2.5V power rail to 3.3V power rail. It can be done on B2B connector see 6 B2B Connectors Pin Descriptions. Or if module connected to baseboard, better to short power rails on baseboard.
- Program eFUSE using JTAG cable and iMPACT software.
- Disconnect 2.5V and 3.3V power rails.

## 4.4 EZ-USB FX2 Firmware Programming

TE0630 module supplied with already programmed FX2 firmware, so this procedure is **not needed for normal work flow**. This procedure is required only if custom firmware used or to restore firmware.

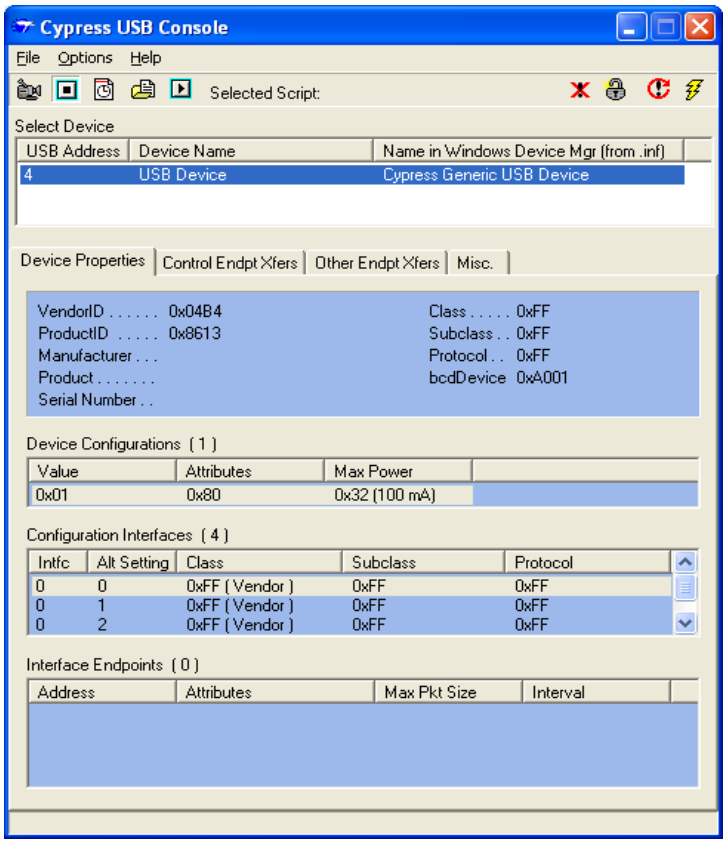
If the EEPROM has never been programmed before (virgin module) Switch 1 (S1A) can be switched to EEPROM (to "ON" state). See chapter 2.14 DIP Switch for details. The USB microcontroller will detect an empty EEPROM and

will provide its default vendor ID and device ID to the USB host. If the EEPROM has been programmed before (EEPROM not empty), S1A must be switched to "OFF". The USB microcontroller will detect a missing EEPROM and will provide its default vendor ID and device ID to the USB host.

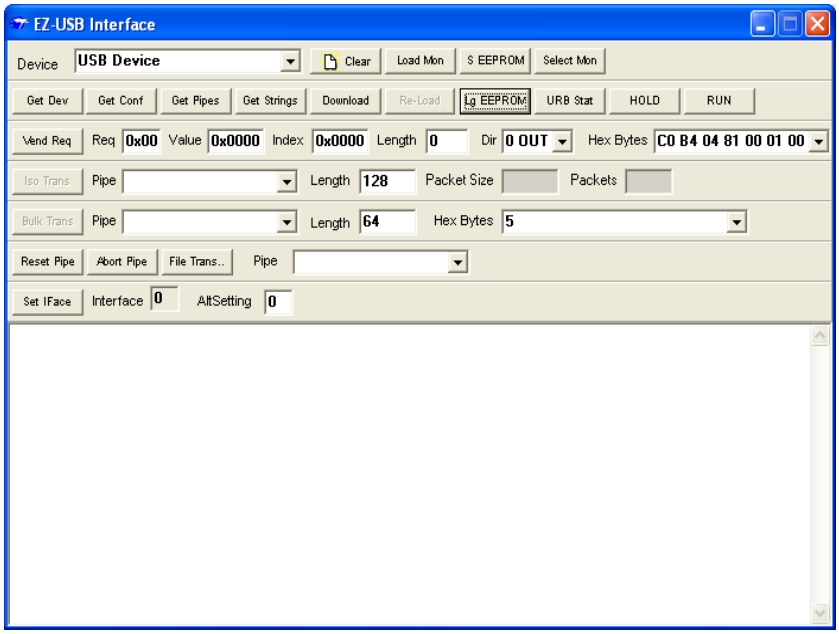
## 4.5 EZ-USB FX2 EEPROM Programming

TE0630 module supplied with already programmed EEPROM, so this procedure is **not needed for normal work flow**. This procedure is required only if custom firmware used or to restore firmware.

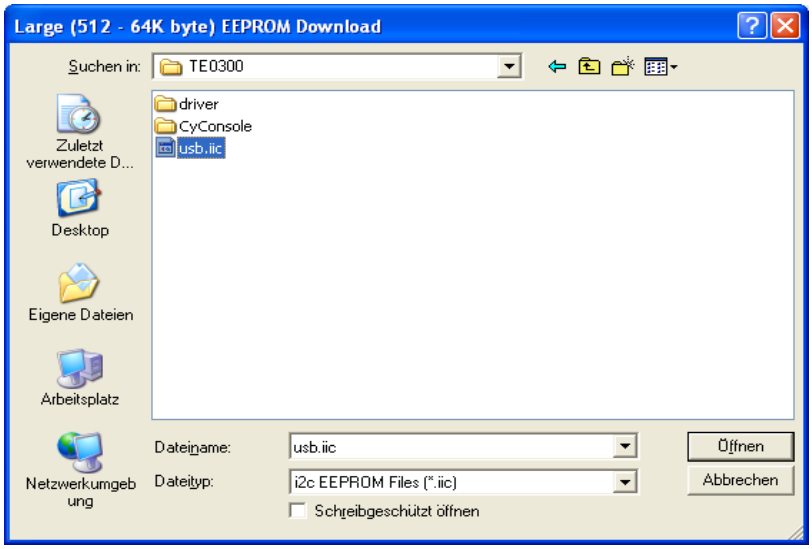
First of all, check that Switch 1 (S1A) is actually switched to EEPROM. The USB EEPROM can be programmed by opening the dedicated software “Cypress USB Console” (double click the “CyConsole.exe” file in the “1st_program\CyConsole” folder).



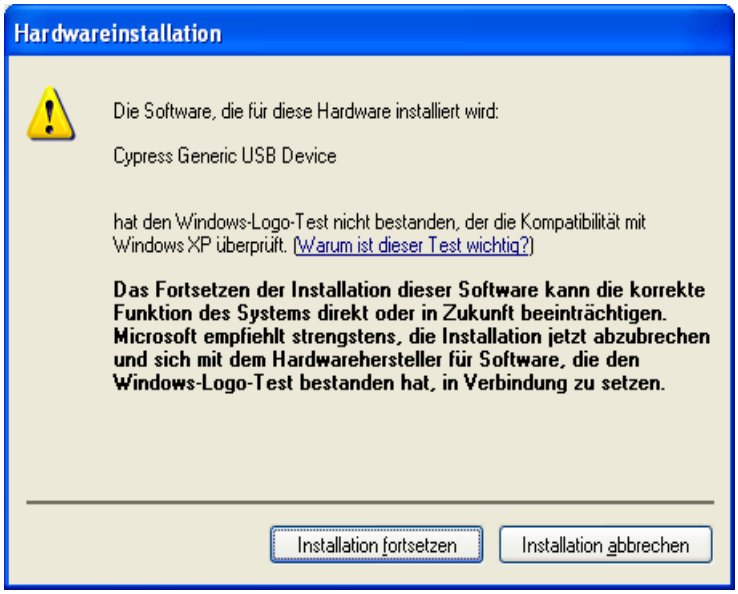

Click “Options > EZ-USB Interface” to Open EZ-USB Interface window.

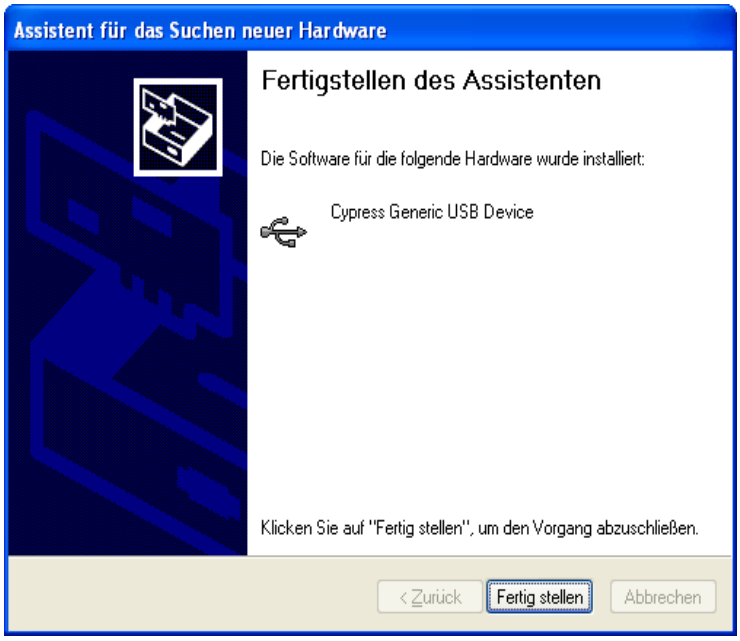


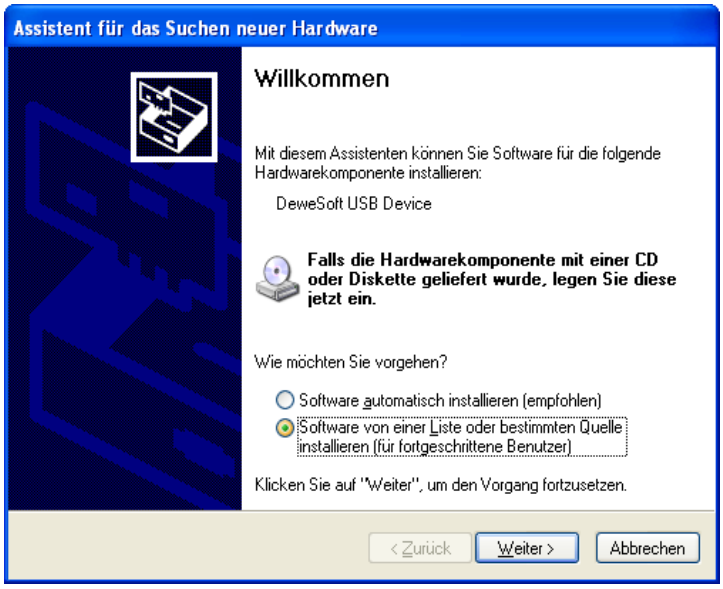

"S EEPROM" button refers to the small EEPROM (256 bytes) whereas the "Lg EEPROM" refers to the large EEPROM (64 KB). Press the "Lg_EEPROM" button, select the "USB.iic" file and press the "Open" button to start writing to EEPROM.

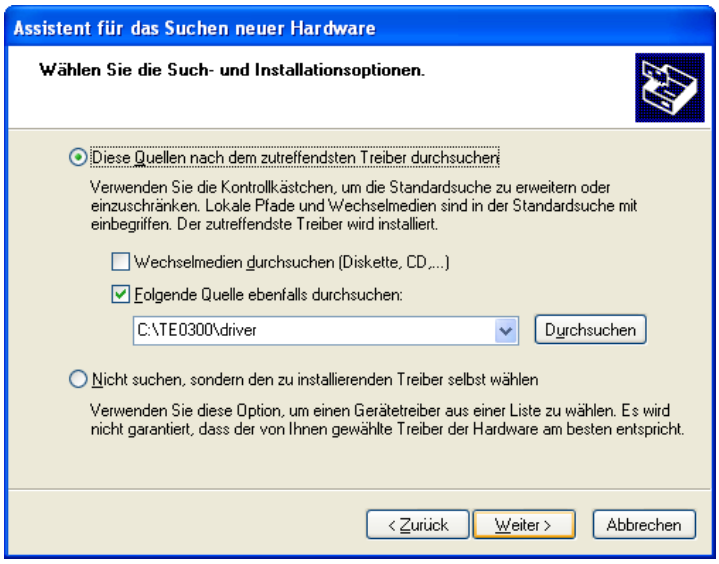


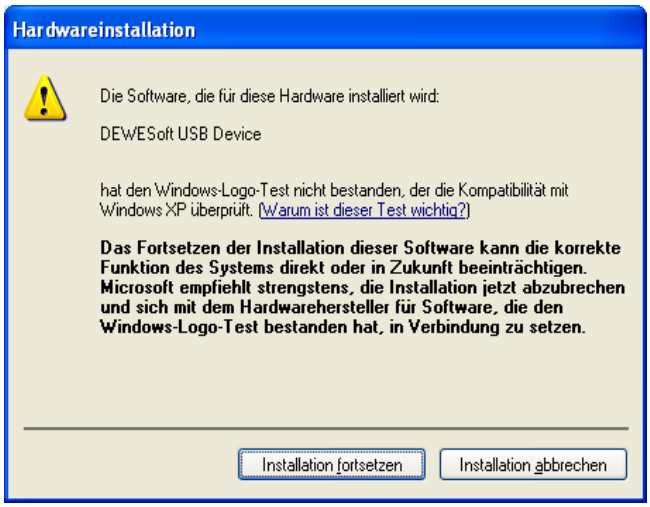

Upgrade progress is displayed in status window and is completed when "Download Successful" text is displayed.


Hardwareinstallation
Die Software, die für diese Hardware installiert wird:
Cypress Generic USB Device
hat den Windows-Logo-Test nicht bestanden, der die Kompatibilität mit Windows XP überprüft. (Warum ist dieser Test wichtig?)
Das Fortsetzen der Installation dieser Software kann die korrekte Funktion des Systems direkt oder in Zukunft beeinträchtigen. Microsoft empfiehlt strengstens, die Installation jetzt abzubrechen und sich mit dem Hardwarehersteller für Software, die den Windows-Logo-Test bestanden hat, in Verbindung zu setzen.
Installation fortsetzen
Installation abbrechen


Assistent für das Suchen neuer Hardware
Fertigstellen des Assistenten
Die Software für die folgende Hardware wurde installiert:
Cypress Generic USB Device
Klicken Sie auf "Fertig stellen", um den Vorgang abzuschließen.
< Zurück
Fertig stellen
Abbrechen


Assistent für das Suchen neuer Hardware
Willkommen
Mit diesem Assistenten können Sie Software für die folgende Hardwarekomponente installieren:
DeweSoft USB Device
Falls die Hardwarekomponente mit einer CD oder Diskette geliefert wurde, legen Sie diese jetzt ein.
Wie möchten Sie vorgehen?
Software automatisch installieren (empfohlen)
Software von einer Liste oder bestimmten Quelle installieren (für fortgeschrittene Benutzer)
Klicken Sie auf "Weiter", um den Vorgang fortzusetzen.
< Zurück
Weiter >
Abbrechen


Assistent für das Suchen neuer Hardware
Wählen Sie die Such- und Installationsoptionen.
Diese Quellen nach dem zutreffendsten Treiber durchsuchen
Verwenden Sie die Kontrollkästchen, um die Standardsuche zu erweitern oder einzuschränken. Lokale Pfade und Wechselmedien sind in der Standardsuche mit einbegriffen. Der zutreffendste Treiber wird installiert.
Wechselmedien durchsuchen (Diskette, CD,...)
Folgende Quelle ebenfalls durchsuchen:
C:\TE0300\driver
Durchsuchen
Nicht suchen, sondern den zu installierenden Treiber selbst wählen
Verwenden Sie diese Option, um einen Gerätetreiber aus einer Liste zu wählen. Es wird nicht garantiert, dass der von Ihnen gewählte Treiber der Hardware am besten entspricht.
< Zurück
Weiter >
Abbrechen


Hardwareinstallation
Die Software, die für diese Hardware installiert wird:
DEWESoft USB Device
hat den Windows-Logo-Test nicht bestanden, der die Kompatibilität mit Windows XP überprüft. (Warum ist dieser Test wichtig?)
Das Fortsetzen der Installation dieser Software kann die korrekte Funktion des Systems direkt oder in Zukunft beeinträchtigen. Microsoft empfiehlt strengstens, die Installation jetzt abzubrechen und sich mit dem Hardwarehersteller für Software, die den Windows-Logo-Test bestanden hat, in Verbindung zu setzen.
Installation fortsetzen
Installation abbrechen

## 6.3 J4 Pin-out

| J4 pin | Net | Type | FPGA pin | Net Length (mm) | J4 pin | Net | Type | FPGA pin | Net Length (mm) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | VCCIO0 | POW | - | - | 2 | VCCIO0 | POW | - | - |
| 3 | VCCIO0 | POW | - | - | 4 | VCCIO0 | POW | - | - |
| 5 | V3_IO_01 | SIO | G6 | 13.30 | 6 | V3_IO_06 | SIO | C4 | 15.26 |
| 7 | V3_IO_02 | SIO | G4 | 11.05 | 8 | V3_IO_07 | SIO | D3 | 17.04 |
| 9 | V3_IO_03 | SIO | F5 | 10.46 | 10 | V3_IO_08 | SIO | E6 | 14.97 |
| 11 | V3_IO_04 | SIO | E5 | 10.08 | 12 | V3_IO_09 | SIO | D5 | 13.84 |
| 13 | GND | GND | - | - | 14 | GND | GND | - | - |
| 15 | V3_IO_05 | SIO | F7 | 10.16 | 16 | V0_IO_11_P | DIO | B6 | 12.29 |
| 17 | V0_IO_01 | SIO | A4 | 5.16 | 18 | V0_IO_11_N | DIO | A6 | 10.84 |
| 19 | V0_IO_01_N | DIO | A5 | 5.14 | 20 | V0_IO_12_N | DIO | A7 | 10.95 |
| 21 | V0_IO_01_P | DIO | C5 | 6.84 | 22 | V0_IO_12_P | DIO | C7 | 12.30 |
| 23 | GND | GND | - | - | 24 | GND | GND | - | - |
| 25 | V0_IO_02_N | DIO | C6 | 7.27 | 26 | V0_IO_13_N | DIO | A8 | 10.41 |
| 27 | V0_IO_02_P | DIO | D6 | 8.16 | 28 | V0_IO_13_P | DIO | B8 | 11.74 |
| 29 | V0_IO_03_P | DIO | D7 | 7.93 | 30 | V0_IO_14_N | DIO | A9 | 10.40 |
| 31 | V0_IO_03_N | DIO | C8 | 7.21 | 32 | V0_IO_14_P | DIO | C9 | 12.81 |
| 33 | 3.3V | POW | - | - | 34 | 3.3V | POW | - | - |
| 35 | V0_IO_04_P | DIO | D9 | 9.34 | 36 | V3_IO_10 | SIO | M7 | 21.84 |
| 37 | V0_IO_04_N | DIO | D8 | 10.08 | 38 | V0_CLK_04_N | CIO | C12 | 12.96 |
| 39 | V0_CLK_03_P | CIO | B12 | 6.00 | 40 | V0_CLK_04_P | CIO | D11 | 13.32 |
| 41 | V0_CLK_03_N | CIO | A12 | 05.01 | 42 | V0_CLK_01_N | CIO | A10 | 10.97 |
| 43 | GND | GND | - | - | 44 | V0_CLK_01_P | CIO | B10 | 11.84 |
| 45 | V0_CLK_02_P | CIO | C11 | 7.93 | 46 | GND | GND | - | - |
| 47 | V0_CLK_02_N | CIO | A11 | 10.76 | 48 | V0_IO_15_N | DIO | A15 | 11.79 |
| 49 | V0_IO_05_P | DIO | C13 | 7.20 | 50 | V0_IO_15_P | DIO | C15 | 13.66 |
| 51 | V0_IO_05_N | DIO | A13 | 6.11 | 52 | V3_IO_11 | SIO | M8 | 26.06 |
| 53 | 2.5V | POW | - | - | 54 | 2.5V | POW | - | - |
| 55 | V0_IO_06_P | DIO | D10 | 12.84 | 56 | V0_IO_16_P | DIO | B16 | 12.98 |
| 57 | V0_IO_06_N | DIO | C10 | 13.09 | 58 | V0_IO_16_N | DIO | A16 | 10.96 |
| 59 | V0_IO_07_P | DIO | F10 | 16.22 | 60 | V0_IO_17_P | DIO | C17 | 16.33 |
| 61 | V0_IO_07_N | DIO | E10 | 15.43 | 62 | V0_IO_17_N | DIO | A17 | 13.51 |
| 63 | GND | GND | - | - | 64 | GND | GND | - | - |
| 65 | V0_IO_08_N | DIO | A14 | 8.21 | 66 | V0_IO_18_P | DIO | B18 | 15.19 |
| 67 | V0_IO_08_P | DIO | B14 | 9.11 | 68 | V0_IO_18_N | DIO | A18 | 13.77 |
| 69 | V0_IO_09_N | DIO | C14 | 9.40 | 70 | TDI | JTAG | E18 | - |
| 71 | V0_IO_09_P | DIO | D15 | 9.40 | 72 | TDO | JTAG | E14 | - |
| 73 | 1.2V | POW | - | - | 74 | 1.2V | POW | - | - |
| 75 | V0_IO_10_N | DIO | C16 | 9.65 | 76 | TCK | JTAG | D14 | - |
| 77 | V0_IO_10_P | DIO | D17 | 9.58 | 78 | TMS | JTAG | E16 | - |
| 79 | GND | GND | - | - | 80 | GND | GND | - | - |

**Table 21: J4 connector pin-out**

## 6.4 J5 Pin-out

| J5 pin | Net | Type | FPGA pin | Net Length (mm) | J5 pin | Net | Type | FPGA pin | Net Length (mm) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 5Vb2b | POW | - | - | 2 | 5Vb2b | POW | - | - |
| 3 | 5Vb2b | POW | - | - | 4 | 5Vb2b | POW | - | - |
| 5 | 5V | POW | - | - | 6 | /MR | SYS | - | - |
| 7 | B2B_D_P | USB | - | - | 8 | /RESET | SYS | - | - |
| 9 | B2B_D_N | USB | - | - | 10 | RESET | SYS | - | - |
| 11 | GND | GND | - | - | 12 | GND | GND | - | - |
| 13 | V3_IO_12 | SIO | T2 | 19.97 | 14 | V3_IO_16 | SIO | U1 | 10.26 |
| 15 | V3_IO_13 | SIO | T1 | 18.91 | 16 | V3_IO_17 | SIO | U3 | 11.74 |
| 17 | V2_IO_01 | SIO | V15 | 18.18 | 18 | V3_IO_18 | SIO | V1 | 9.72 |
| 19 | V3_IO_14 | SIO | AA2 | 16.26 | 20 | V3_IO_19 | SIO | V2 | 10.03 |
| 21 | V3_IO_15 | SIO | AB2 | 15.23 | 22 | V3_IO_20 | SIO | Y1 | 9.21 |
| 23 | GND | GND | - | - | 24 | GND | GND | - | - |
| 25 | V2_IO_01_N | DIO | AB6 | 10.68 | 26 | V3_IO_21 | SIO | Y2 | 8.73 |
| 27 | V2_IO_01_P | DIO | AA6 | 12.54 | 28 | V3_IO_22 | SIO | AB3 | 6.68 |
| 29 | V2_IO_02_P | DIO | Y7 | 13.32 | 30 | V3_IO_23 | SIO | Y3 | 8.38 |
| 31 | V2_IO_02_N | DIO | AB7 | 11.56 | 32 | V3_IO_24 | SIO | AB4 | 6.65 |
| 33 | V3_IO_27 | SIO | U8 | 8.41 | 34 | V3_IO_25 | SIO | AA4 | 7.51 |
| 35 | 3.3V | POW | - | - | 36 | 3.3V | POW | - | - |
| 37 | V2_IO_03_N | DIO | AB8 | 12.43 | 38 | V3_IO_26 | SIO | Y4 | 8.41 |
| 39 | V2_IO_03_P | DIO | AA8 | 13.01 | 40 | V2_IO_10_P | DIO | W6 | 9.20 |
| 41 | V2_IO_02 | SIO | AB12 | 12.62 | 42 | V2_IO_10_N | DIO | Y6 | 8.31 |
| 43 | GND | GND | - | - | 44 | GND | GND | - | - |
| 45 | V2_CLK_01_N | CIO | AB11 | 11.34 | 46 | V2_IO_11_N | DIO | Y8 | 8.09 |
| 47 | V2_CLK_01_P | CIO | Y11 | 12.64 | 48 | V2_IO_11_P | DIO | W9 | 9.10 |
| 49 | V2_IO_04_P | DIO | W15 | 14.63 | 50 | V2_IO_12_P | DIO | Y9 | 8.40 |
| 51 | V2_IO_04_N | DIO | Y16 | 12.42 | 52 | V2_IO_12_N | DIO | AB9 | 6.60 |
| 53 | 2.5V | POW | - | - | 54 | 2.5V | POW | - | - |
| 55 | V2_IO_05_N | DIO | U14 | 17.21 | 56 | V2_CLK_02_N | CIO | AB10 | 7.26 |
| 57 | V2_IO_05_P | DIO | T14 | 18.75 | 58 | V2_CLK_02_P | CIO | AA10 | 8.16 |
| 59 | V2_IO_06_P | DIO | AA14 | 12.39 | 60 | V2_IO_13_P | DIO | W11 | 11.39 |
| 61 | V2_IO_06_N | DIO | AB14 | 11.34 | 62 | V2_IO_13_N | DIO | Y10 | 10.30 |
| 63 | GND | GND | - | - | 64 | GND | GND | - | - |
| 65 | V2_IO_07_N | DIO | AB15 | 11.87 | 66 | V2_IO_14_N | DIO | Y12 | 9.80 |
| 67 | V2_IO_07_P | DIO | Y15 | 13.55 | 68 | V2_IO_14_P | DIO | W12 | 10.80 |
| 69 | V2_IO_08_P | DIO | AA16 | 12.61 | 70 | V2_IO_15_P | DIO | Y13 | 10.20 |
| 71 | V2_IO_08_N | DIO | AB16 | 11.72 | 72 | V2_IO_15_N | DIO | AB13 | 8.40 |
| 73 | 1.2V | POW | - | - | 74 | 1.2V | POW | - | - |
| 75 | V2_IO_09_N | DIO | AB18 | 11.91 | 76 | V2_IO_16_N | DIO | Y14 | 9.72 |
| 77 | V2_IO_09_P | DIO | AA18 | 12.57 | 78 | V2_IO_16_P | DIO | W14 | 10.72 |
| 79 | GND | GND | - | - | 80 | GND | GND | - | - |

**Table 22: J5 connector pin-out**

A CAUTION notice denotes a risk. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in a fault. (undesired condition that can lead to an error) Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

| | |
|---|---|
| **API** | application programming interface |
| **B2B** | board-to-board |
| **DSP** | digital signal processing; digital signal processor |
| **EDK** | Embedded Development Kit |
| **IOB** | input / output blocks; I/O blocks |
| **IP** | intellectual property |
| **ISP** | In-System Programmability |
| **PB** | push button |
| **SDK** | Software Development Kit |
| **TE** | Trenz Electronic |
| **XPS** | Xilinx Platform Studio |

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# Appendix A. Indirect SPI Programming using iMPACT

To indirect program SPI Flash using Xilinx iMPACT do following steps:

Connect JTAG cable to corresponding module connector (see 2.6 JTAG connector).

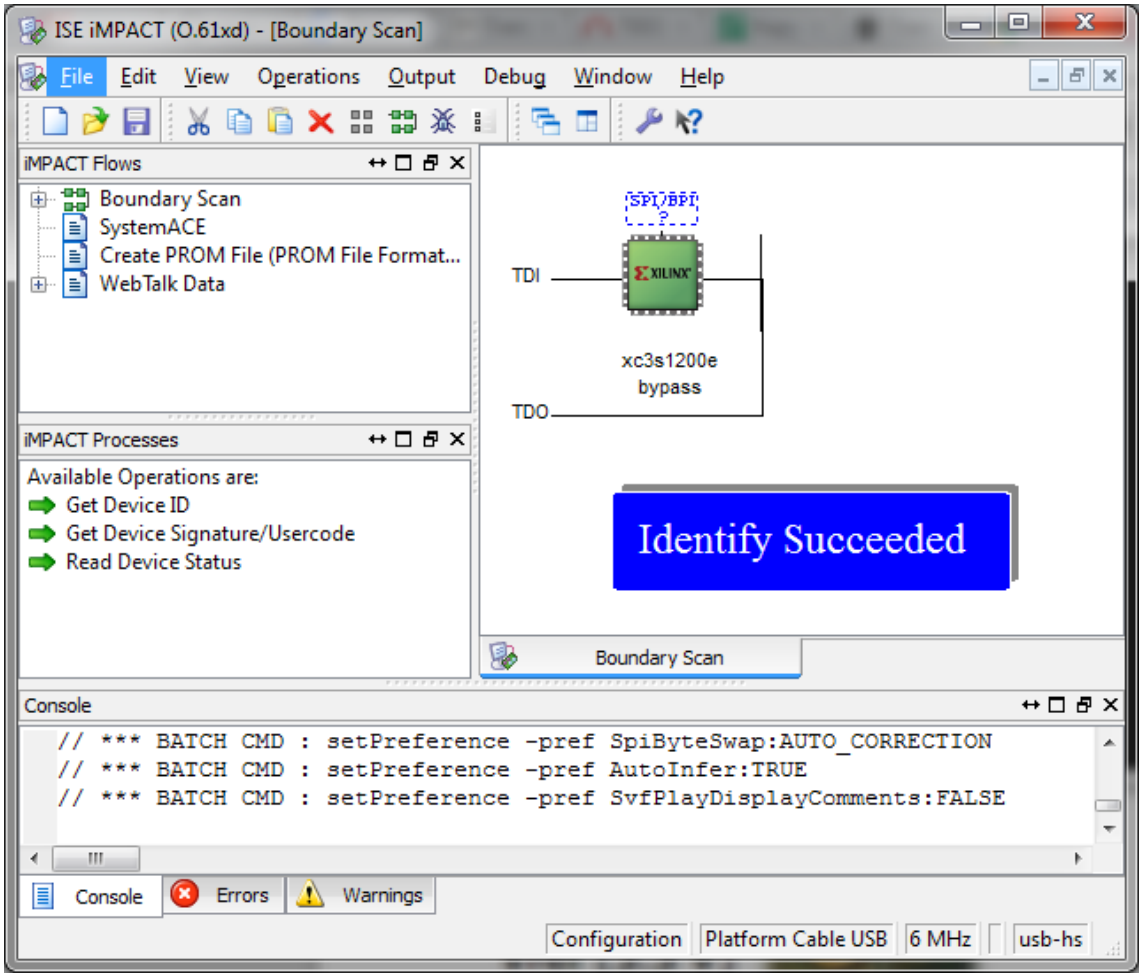
Connect JTAG cable to host computer with installed Xilinx iMPACT software.

Power-on module by external power supply source or by USB cable.

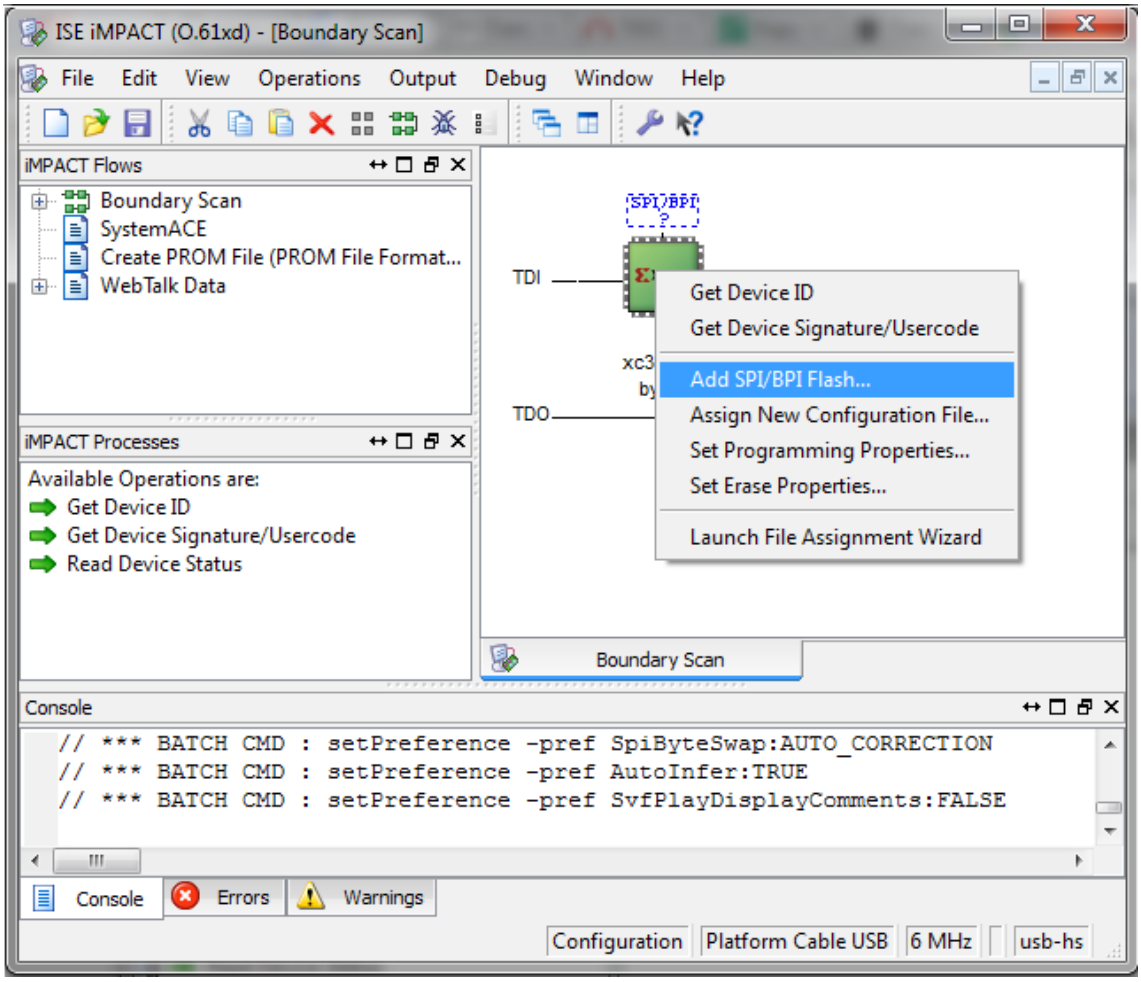
Run Xilinx iMPACT.

Select Boundary Scan mode.

After initialization iMPACT window should look like

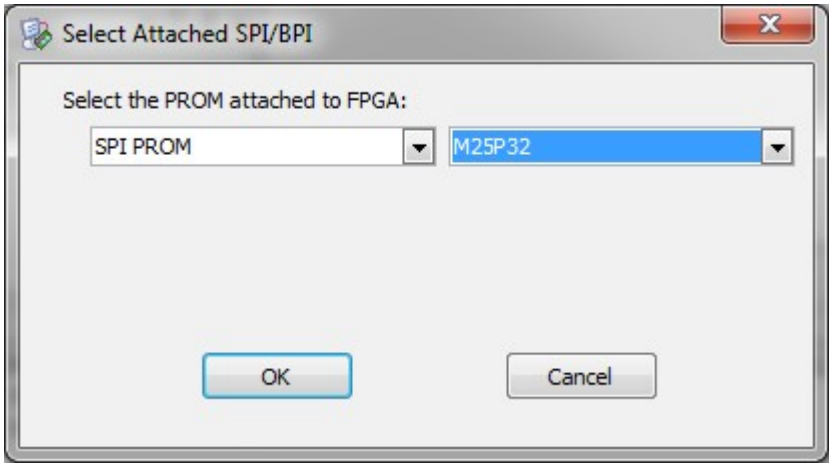



Right click on FPGA image and select “Add SPI/BPI Flash...” from menu.

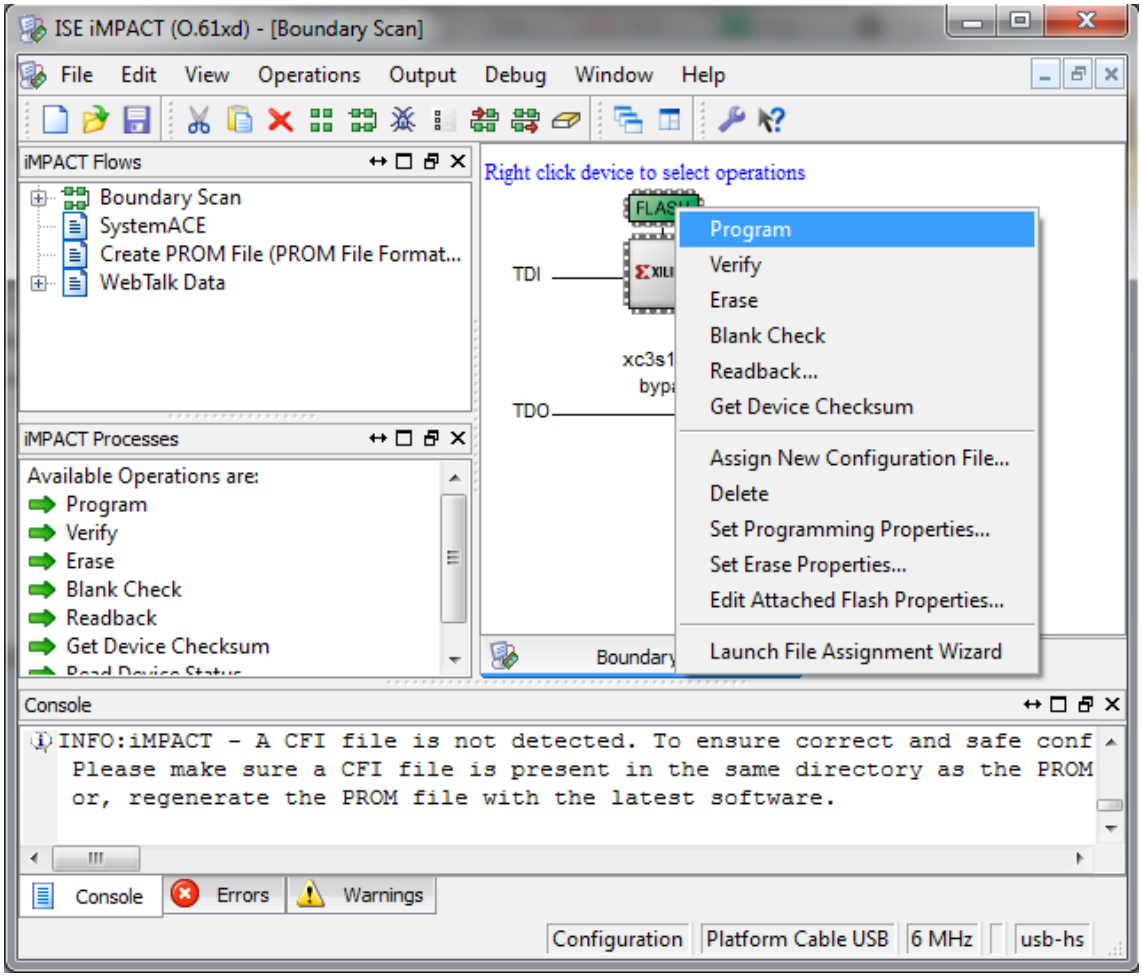



Select mcs file to program.

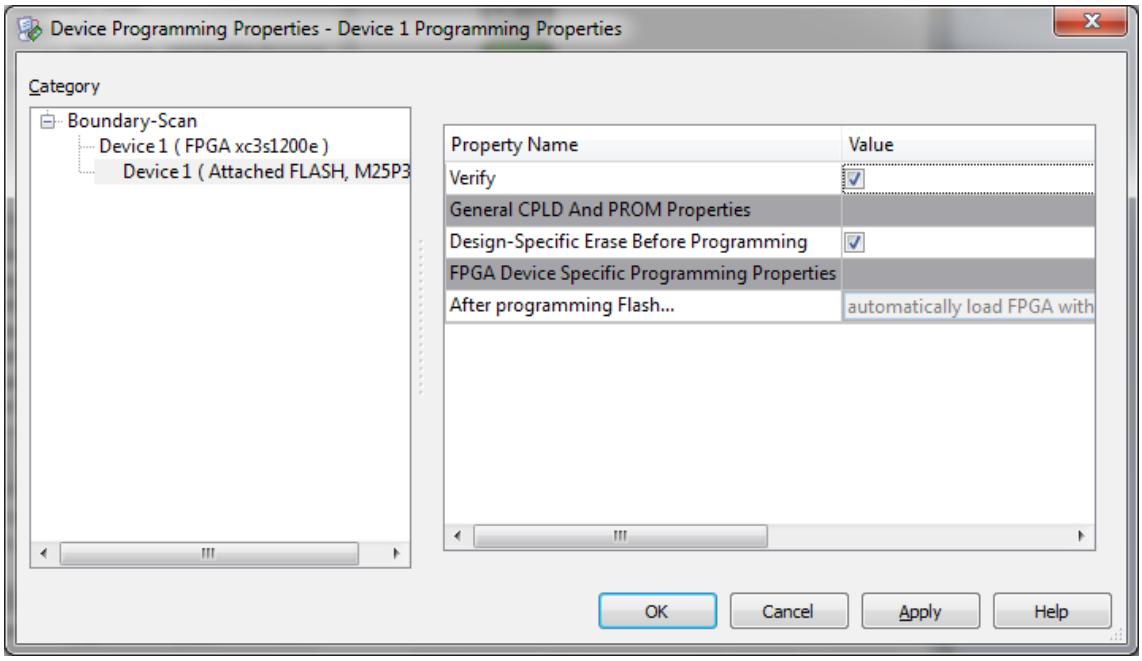
Select SPI Flash type corresponding to your module type and revision.




Right click on Flash image and select “Program” from menu.




Leave default programming properties and press “OK”.




Wait for operation to complete.