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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA, USB Core
Core Processor	Spartan-6 LX-150
Co-Processor	Cypress EZ-USB FX2LP
Speed	100MHz
Flash Size	8MB
RAM Size	128MB
Connector Type	B2B
Size / Dimension	1.6" x 1.9" (40.5mm x 47.5mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0630-01iv

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- no power supply is provided by B2B connectors.

In this case, other components (e.g. extension or carrier boards) may also be powered by the corresponding 5 volt line (5V) of B2B connector J5.

2.2.3 On-board Power Rails

Three on-board voltage regulators provide the following power supply rails needed by the components on the module:

- 1.2V, 3.0 A max
- 2.5V, 0.8 A max
- 3.3V, 3.0 A max
- 1.5V, 1.0 A max

Figure 3 show power supply diagram.

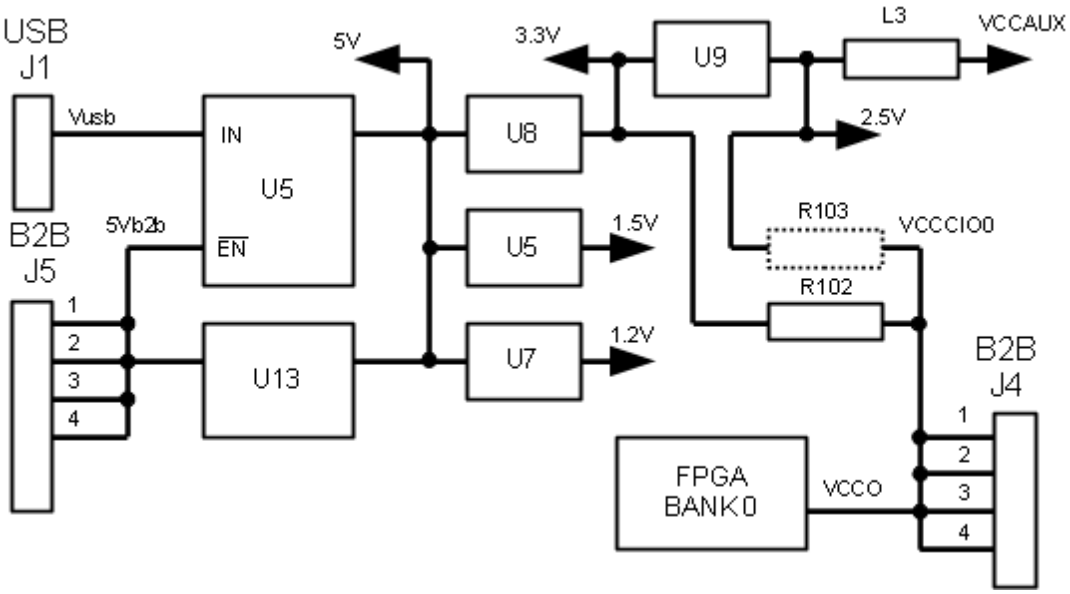


Figure 3: TE0630 Power diagram

The power rails are available for the FPGA and can be shared with a carrier board by the **corresponding** lines of the B2B connectors J4 and J5. Please note that the **power consumption of the FPGA is highly dependent on the design actually loaded.** So please use a tool like Xilinx Xpower to estimate the expected power consumption of your design.

Even if the provided voltages of the module are not used on the carrier board, it is recommended to bypass them to ground with 10 nF - 100 nF capacitors.

FPGA I/O banks power supply

Spartan-6 architecture organizes I/Os into four I/O banks, see Table 1 for supply voltage used for each bank.

VCCIO0 voltage can be configured in 3 ways:

- **2.5V** - When resistor **R103 is populated** and resistor **R102 is not populated**.
- **3.3V** - When **R103 is not populated** and resistor **R102 is populated**.

2.4 Board-to-board Connectors

The module has two B2B (board-to-board) receptacle connectors (J4 and J5) for a total of 160 contacts. Figure 6 shows B2B connectors location on board; USB connector is located on the top side and is shown to define module position.

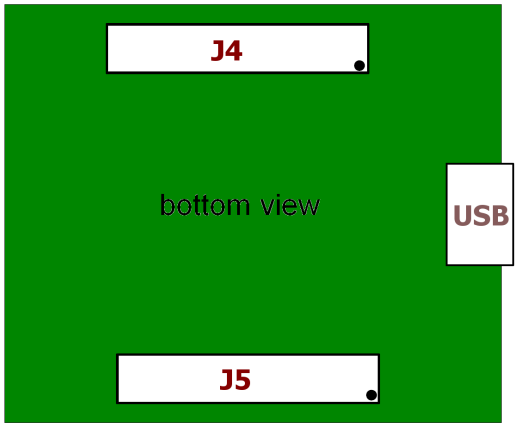


Figure 6: B2B connectors location

TE0630 uses high-density shockproof connectors shown in Figure 7. Connector part numbers are listed in Table 4.

Figure 7: Module connector

Supplier	Header
Digikey	H11113CT-ND H11113TR-ND H11113DKR-ND
Hirose	DF17(3.0)-80DS-0.5V(57)
Trenz Electronic	22684

Table 4: Module connectors part numbers

The on-board receptacles mate with their corresponding headers on the carrier board shown in Figure 8. Ordering numbers of mating connectors are listed in Table 5.

Signal name	FPGA pin
FD0	J6
FD1	H8
FD2	H5
FD3	H6
FD4	G7
FD5	G8
FD6	F8
FD7	A3
24MHZ1	G3
PA0/INT0	D1
PA1/INT1	D2
PA2/SLOE	C1
PA3/WU	E4
PA4/FIFOADDR0	B1
PA5/FIFOADDR1	C3
PA6/PKTEND	B2
PA7/FLAGD/SLCS	A2
RDY1/SLWR	M3
RDY0/SLRD	M4
CTL2/FLAGC	E3
CTL1/FLAGB	E1
CTL0/FLAGA	F3
IFCLK	N4

Table 7: USB controller interface: FPGA pin-out

2.11 Clock Oscillators

Two clock oscillators are installed on the TE0630.

Clock oscillator U10 generates a 24 MHz clock signal for the FPGA and the USB controller. This clock signal is used for synchronous communication between FPGA and USB controller.

Clock oscillator U11 generates a 100 MHz[3] clock signal used as a main system clock in FPGA designs. See Table 8 for pin-out information.

Signal	Frequency	FPGA pin
24MHZ1	24 MHz	G3
SYSCLK	100 MHz	AA12

Table 8: Clock signals pin-out

2.12 LEDs

TE0630 is equipped with four active-high LEDs. See Table 9 for details.

3 Oscillator frequency can be changed by user request. Contact Trenz Electronic for details.

Signal name	FPGA pin	LED
U_LED1	F1	D3
U_LED2	F2	D5
U_LED3	J4	D6
U_LED4	K8	D7

Table 9: LEDs pin-out

2.13 Push-Button

TE0630 module is equipped with one active-high push-button (signal is set to logical "1" when button is pressed). Table 10 show push-button connection details.

Signal name	FPGA pin	PB
PB	R7	S5

Table 10: Push button pin-out

2.14 DIP Switch

On-board 4xDIP switch S1 used for system and user settings.

Switch 1 (S1A) is used to connect the USB controller to the I^2C serial EEPROM. When S1A is "ON", serial I^2C EEPROM is connected to the USB controller, when switch is "OFF", the USB controller is disconnected from the EEPROM[4]. Turn S1A off when programming the USB EEPROM (storing the USB vendor ID and device ID). This will force the USB controller to provide its default vendor ID and device ID.

Switch 2 (S1B) is used to control DC-DC converters. When switch is "OFF", converters are controlled by the USB controller. When switch is "ON", converters are enabled regardless of USB controller actions. At start-up, the USB controller switches off 1.2V, 1.5V and 2.5V power rails and starts up the module in low-power mode. After enumeration, the USB controller firmware switches the 1.2V, 1.5V and 2.5V power rails on, if enough current is available from the USB bus.

Switches 3 (S1C) and 4 (S1D) can be used as user switches. Switches are active-low. Pull-up resistors should be defined in user constrains file (UCF) to use this switches in FPGA design. See Table 11 for details.

Signal name	FPGA pin	Switch
IO_L61_N_1	AB21	S1C
IO_L63_N_1	AA22	S1D

Table 11: DIP switch pin-out

2.15 Board revisions and assembly variants

To determine PCB revision and assembly variant from FPGA, TE0630 have dedicated user signals, which can be read by user core.

Board revision coded in 4 bits BR[3:0]

4 Zero-resistor R90 (not populated by default) short this switch and connect EEPROM regardless of S1A position.

Signal name	FPGA pin
BR0	R19
BR1	V19
BR2	V20
BR3	T17

Table 12: Board revision pins

To define low (zero) level BR pin connected to ground rail, to define high (one) level BR pin left float (open). These pins should be configured with "pullup" option in user design.

See Table 12 for current list of board revisions.

BR3	BR2	BR1	BR0	
0	0	0	0	00 Initial revision

Table 13: Board revisions

Module assembly variant encoded using AV[3:0] pins.

Signal name	FPGA pin
AV0	Y20
AV1	R15
AV2	R16
AV3	R17

Table 14: Assembly variants pins

To define low (zero) level AV pin connected to ground rail through zero resistor, to define high (one) level AV pin left float (open). These pins should be configured with "pullup" option in user design.

Available module assembly variants listed in Table 15.

AV3	AV2	AV1	AV0	
0	0	0	0	Base assembly variant

Table 15: Module assembly variants

3 TE0300 compatibility

TE0630 module designed to be compatible with TE0300 board by main mechanical and electrical characteristics.

3.1 Mechanical compatibility

Both modules have the same board dimensions. TE0630 mount holes and B2B connectors locations are match with TE0300. See chapter 1.2 Dimensions for detailed information.

TE0300 and TE0630 uses same B2B connectors types. In chapter 2.4 Board-to-board Connectors you can find B2B connectors part numbers and main characteristics.

3.2 Electrical compatibility

TE0300 and TE0630 have similar power requirements and matched power input pins. User signals to B2B connectors routed as differential pairs and single

ended lines. Differences in pin types shown in Table 16, not listed signals have same or compatible[5] type.

Connector:Pin	TE0300 pin name	TE0300 Type	TE0630 pin name	TE0630 Type
J4:5	B3_L01_P	DIO	V3_IO_01	SIO
J4:7	B3_L01_N	DIO	V3_IO_02	SIO
J4:9	B3_L02_P	DIO	V3_IO_03	SIO
J4:11	B3_L02_N	DIO	V3_IO_04	SIO
J4:17	B0_L24_N	DIO	V0_IO_01	SIO
J4:19	B0_L24_P	DIO	V0_IO_01_N	DIO
J4:6	B3_L07_P	DIO	V3_IO_06	SIO
J4:8	B3_L07_N	DIO	V3_IO_07	SIO
J4:10	B3_L03_N	DIO	V3_IO_08	SIO
J4:12	B3_L03_P	DIO	V3_IO_09	SIO
J5:13	B3_L22_P	DIO	V3_IO_12	SIO
J5:15	B3_L22_N	DIO	V3_IO_13	SIO
J5:19	B3_L20_P	DIO	V3_IO_14	SIO
J5:21	B3_L20_N	DIO	V3_IO_15	SIO
J5:16	B3_L21_N	DIO	V3_IO_17	SIO
J5:18	B3_L21_P	DIO	V3_IO_18	SIO
J5:20	B3_L23_N	DIO	V3_IO_19	SIO
J5:22	B3_L23_P	DIO	V3_IO_20	SIO
J5:32	B2_L06_P	DIO	V3_IO_24	SIO
J5:34	B2_L06_N	DIO	V3_IO_25	SIO
J5:41	B2_GCLK13	CIO	V2_IO_02	SIO
J5:49	B2_GCLK_L13_N	CIO	V2_IO_24_P	DIO
J5:51	B2_GCLK_L13_P	CIO	V2_IO_24_N	DIO

Table 16: TE0300 and TE0630 pin types differences.

See Table 17 for pin types definitions.

Type colour code	Description
DIO	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CIO	Unrestricted, general-purpose differential user-I/O pin. This pin also can be used as FPGA clock input.

Table 17: TE0300 and TE0630 pin types

Most user signals to B2B connectors routed from same FPGA banks. Differences shown in Table 18.

5 Signals routed as differential pairs can be used as single ended.

Connector:Pin	TE0300 Bank	TE0630 Bank
J4:15	0	3
J4:36	0	3
J4:52	0	3
J5:33	2	3
J5:28	2	3
J5:30	2	3
J5:32	2	3
J5:34	2	3
J5:38	2	3
J5:40	3	2
J5:42	3	2
J5:50	3	2
J5:52	3	2

Table 18: TE0300 and TE0630 user signals I/O banks differences.

I/O Banks power supply for both modules shown in Table 19.

Bank	TE0300	TE0630
B0	VCCIO (1.2 V - 3.3 V)	VCCIO (1.2 V - 3.3 V)
B1	2.5 V	1.5 V
B2	3.3 V	3.3 V
B3	3.3 V	3.3 V

Table 19: TE0300 and TE0630 FPGA I/O banks power supply.

Bank 0 I/O supply voltage at both modules can be configured by user, see chapter 2.2.3 On-board Power Rails.

4 Module Configuration

Full module configuration cycle (for just assembled board) include steps:

1. Generic USB driver installation
2. USB microcontroller large EEPROM programming
3. EEPROM programming
4. Dedicated driver installation
5. SPI Flash configuration

Steps 1-3 already performed at Trenz Electronic laboratory, and **not required** to perform by end user.

To work with TE0630 module using USB interface user should install dedicated USB driver, which provide API to work with main module functions, for complete instructions see chapter 5.2 Dedicated driver installation.

The FPGA on the TE0630 can be configured by SPI Flash or by JTAG connector.

4.1 JTAG FPGA Configuration

Programming using JTAG interface provide convenient and fast way to test FPGA project. FPGA configuration programmed this way is volatile and lost

after reset or power cycle.

4.2 SPI FPGA Configuration

The bit-stream for the FPGA is stored in the SPI Flash. To use this bit-stream source FPGA configuration option is set to “Master Serial/SPI”. See 2.8 SPI Flash for additional information.

SPI Flash can be programmed in several ways:

- Direct programming by USB controller (usually done by Firmware Upgrade Tool).
- Indirect SPI programming via FPGA pins, controlled by JTAG (can be done using Xilinx iMPACT). See Appendix A. Indirect SPI Programming using iMPACT.
- Direct SPI programming by FPGA, using an SPI core (FPGA project should contain SPI interface core and software to work with it).

In SPI Flash mode, the FPGA’s internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM’s Slave Clock input pin. The FPGA begins configuring using its lowest frequency setting. If so specified in the configuration bitstream, the FPGA increases the CCLK frequency to the specified setting for the remainder of the configuration process. The maximum frequency is specified using the ConfigRate bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. For TE0630 SPI Flash PROM, use ConfigRate = 12 or lower.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Configuration Options > Configuration Rate > 12 (or lower)

4.3 eFUSE programming

To program eFUSE at TE0630 module follow the steps below.

- Connect 2.5V power rail to 3.3V power rail. It can be done on B2B connector see 6 B2B Connectors Pin Descriptions. Or if module connected to baseboard, better to short power rails on baseboard.
- Program eFUSE using JTAG cable and iMPACT software.
- Disconnect 2.5V and 3.3V power rails.

4.4 EZ-USB FX2 Firmware Programming

TE0630 module supplied with already programmed FX2 firmware, so this procedure is **not needed for normal work flow**. This procedure is required only if custom firmware used or to restore firmware.

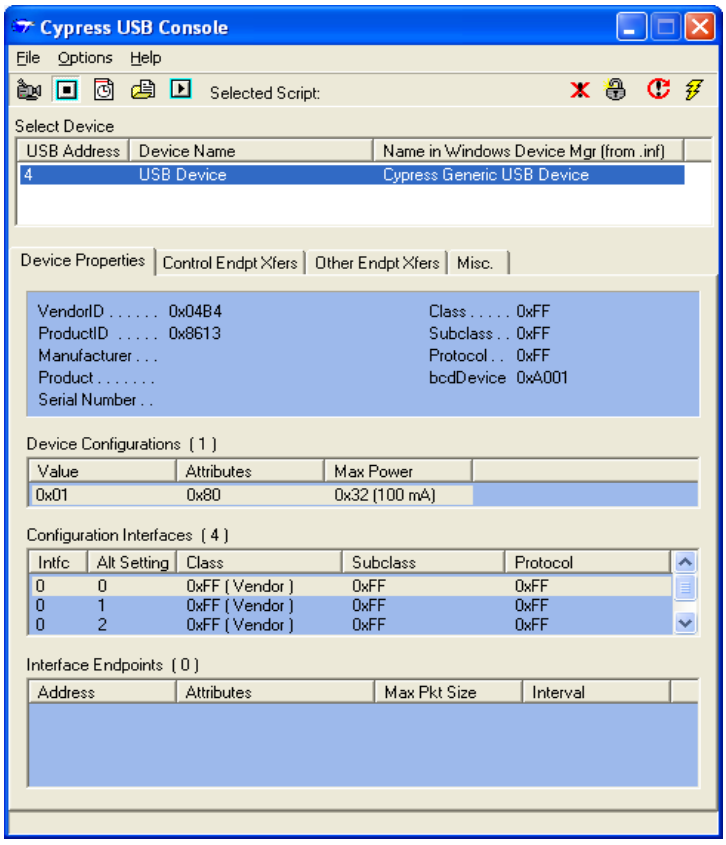
If the EEPROM has never been programmed before (virgin module) Switch 1 (S1A) can be switched to EEPROM (to "ON" state). See chapter 2.14 DIP Switch for details. The USB microcontroller will detect an empty EEPROM and

will provide its default vendor ID and device ID to the USB host. If the EEPROM has been programmed before (EEPROM not empty), S1A must be switched to "OFF". The USB microcontroller will detect a missing EEPROM and will provide its default vendor ID and device ID to the USB host.

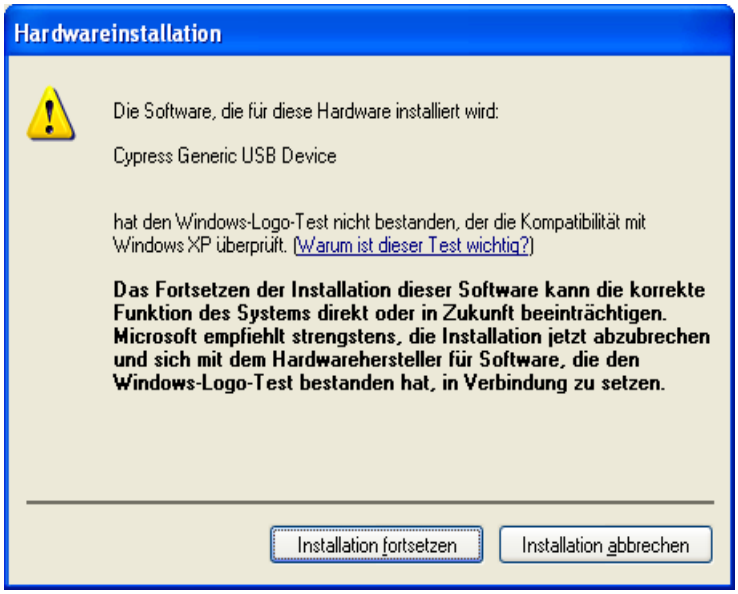
4.5 EZ-USB FX2 EEPROM Programming

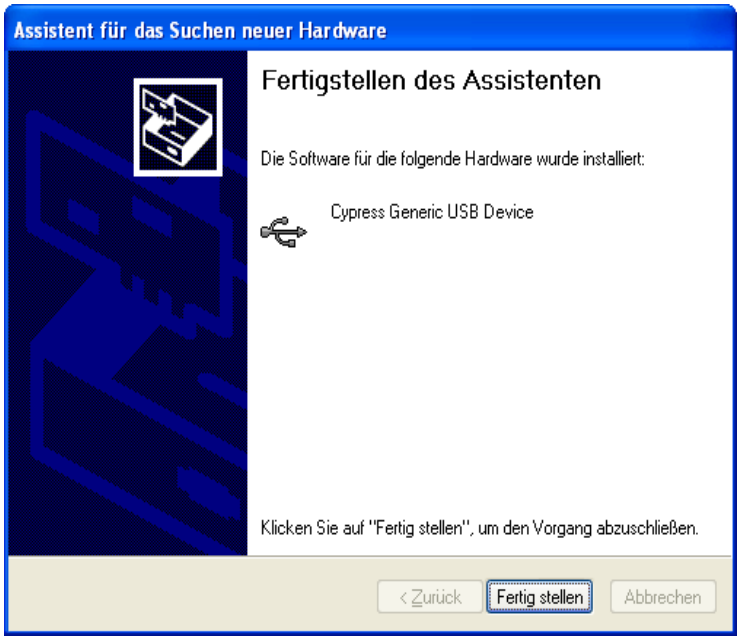
TE0630 module supplied with already programmed EEPROM, so this procedure is **not needed for normal work flow**. This procedure is required only if custom firmware used or to restore firmware.

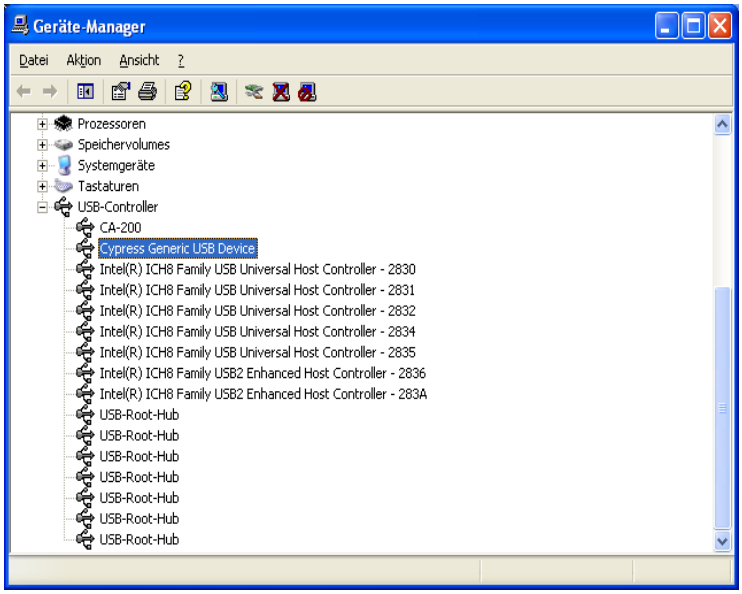
First of all, check that Switch 1 (S1A) is actually switched to EEPROM. The USB EEPROM can be programmed by opening the dedicated software “Cypress USB Console” (double click the “CyConsole.exe” file in the “1st_program\CyConsole” folder).



Click “Options > EZ-USB Interface” to Open EZ-USB Interface window.


Hardwareinstallation
Die Software, die für diese Hardware installiert wird:
Cypress Generic USB Device
hat den Windows-Logo-Test nicht bestanden, der die Kompatibilität mit Windows XP überprüft. (Warum ist dieser Test wichtig?)
Das Fortsetzen der Installation dieser Software kann die korrekte Funktion des Systems direkt oder in Zukunft beeinträchtigen. Microsoft empfiehlt strengstens, die Installation jetzt abzubrechen und sich mit dem Hardwarehersteller für Software, die den Windows-Logo-Test bestanden hat, in Verbindung zu setzen.
Installation fortsetzen
Installation abbrechen


Assistent für das Suchen neuer Hardware
Fertigstellen des Assistenten
Die Software für die folgende Hardware wurde installiert:
Cypress Generic USB Device
Klicken Sie auf "Fertig stellen", um den Vorgang abzuschließen.
< Zurück
Fertig stellen
Abbrechen



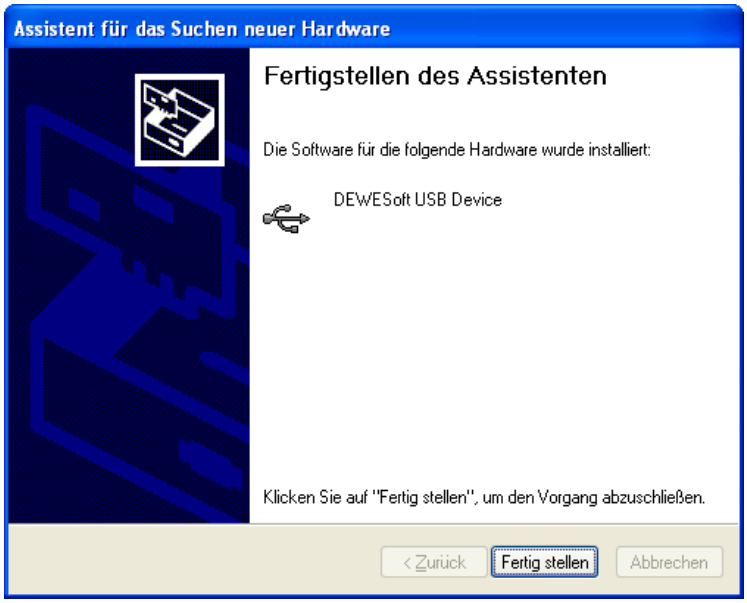
After that I^2C EEPROM should be programmed with right Vendor ID / Device ID, see chapter 4.5 EZ-USB FX2 EEPROM Programming.

5.2 Dedicated Driver

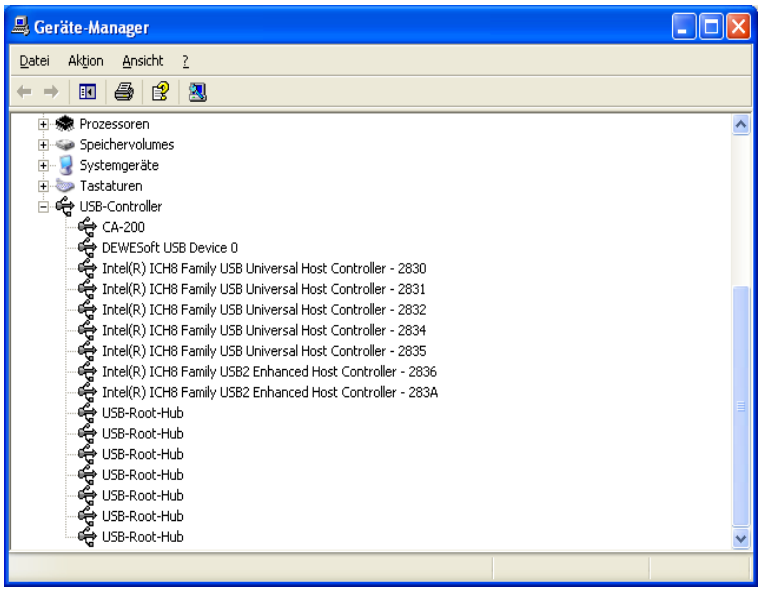
This driver used to work with modules which have DEWESoft firmware and Vendor ID / Device ID programmed. All TE0630 modules supplied with programmed USB controller and corresponding Vendor ID / Device ID in EEPROM.

Before connect USB cable, check that Switch 1 (S1A) is on "ON" state (USB controller connected to EEPROM).

Connect USB cable and wait until the operating system detects new hardware and starts the hardware assistant and answer the hardware assistant questions as shown in the following example.



Check that in the “Device Manager” under “USB-Controller” the “DEWESoft USB Device 0” has been added.



6 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors J4 and J5 are connected to TE0630 on-board components. There are four main signal types connected to B2B connectors:

- FPGA users signals;
- USB signals;
- Power signals;
- System reset signals.

6.1 Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "Vx_IO_yy_p" naming convention, where:

- Vx defines the FPGA bank (x = bank number);
- IO defines an "FPGA to B2B" signal type;
- yy defines a differential pair or signal number (yy = pair number);
- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Remaining signals use custom names.

6.2 Pin Types

Most pins of B2B connectors J1 and J2 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 5 different functional types of pins on the TE0630, as outlined in Table 20. In pin-out tables Table 21 and Table 22, the individual pins are colour-coded according to pin type as defined in Table 20.

type colour code	description
DIO	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CIO	Unrestricted, general-purpose differential user-I/O pin. This pin also can be used as FPGA clock input.
USB	USB signals.
JTAG	Dedicated JTAG signals.
GND	Dedicated ground pin. All must be connected.
SYS	System signal. See the description of each pin in the user manual for additional information on the corresponding signals.
POW	Power signals.

Table 20: TE0630 pin types

6.5 Signal Integrity Considerations

Traces of differential signals pairs are routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length[6]. For applications where traces length has to be matched or timing differences have to be compensated, Table 21 and Table 22 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 100 ohm. Single ended traces are routed with 60 ohm impedance.

An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

7 Related Materials and References

The following documents provide supplementary information useful with this user manual.

7.1 Data Sheets

- Winbond W25Q64BV product overview.

  http://www.winbond.com.tw/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/W25Q64BV.htm

- Xilinx DS160: Xilinx Spartan-6 Family overview

  http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf

- Cypress EZ-USB FX2 Controller datasheet

  http://www.cypress.com/?mpn=CY7C68013A-56LTXC

7.2 User Guides

- Xilinx UG380: Spartan-6 FPGA Configuration User Guide

  http://www.xilinx.com/support/documentation/user_guides/ug380.pdf

- Xilinx UG381: Spartan-6 FPGA SelectIO Resources

  http://www.xilinx.com/support/documentation/user_guides/ug381.pdf

8 Glossary of Abbreviations and Acronyms

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

6 Difference in signal lines length is negligible for used signal frequency.

A CAUTION notice denotes a risk. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in a fault. (undesired condition that can lead to an error) Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit
IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio

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According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products.

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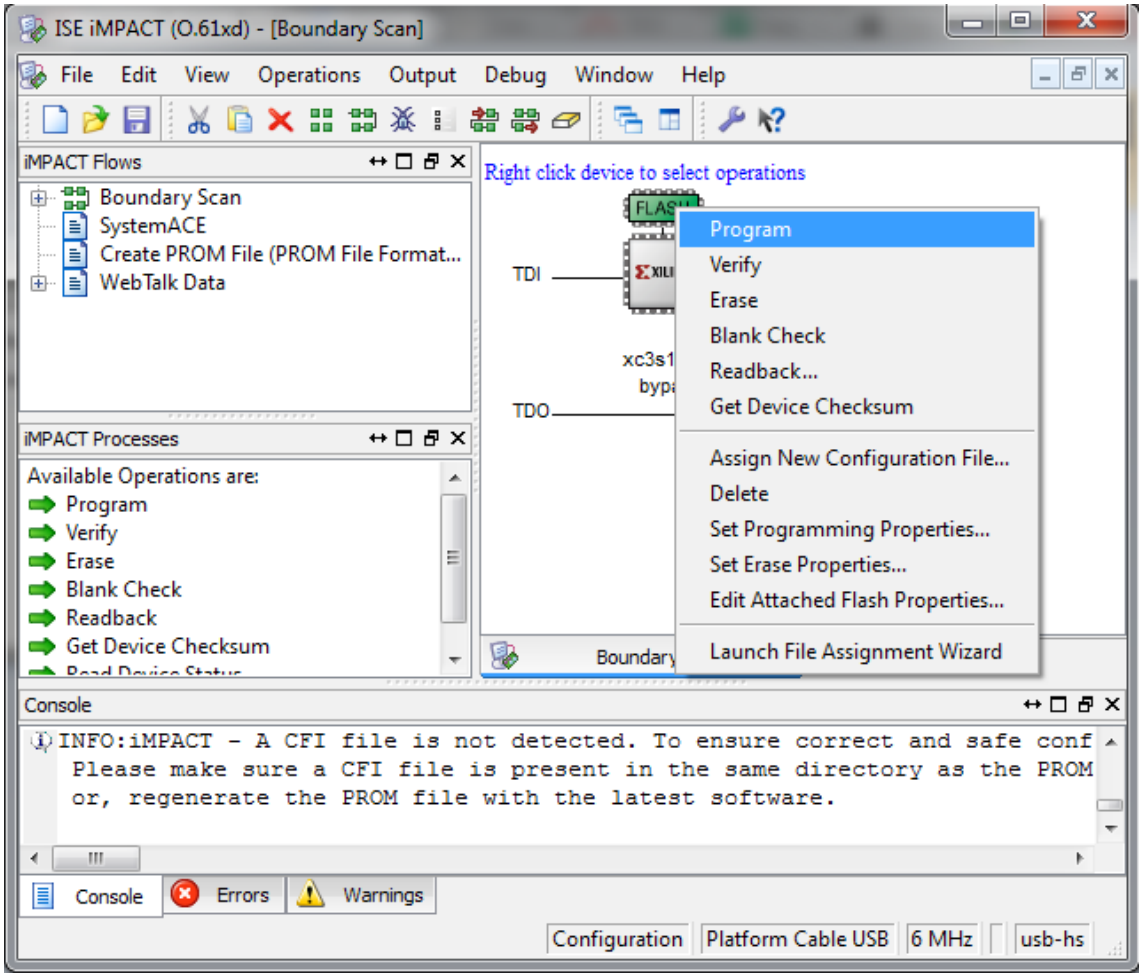
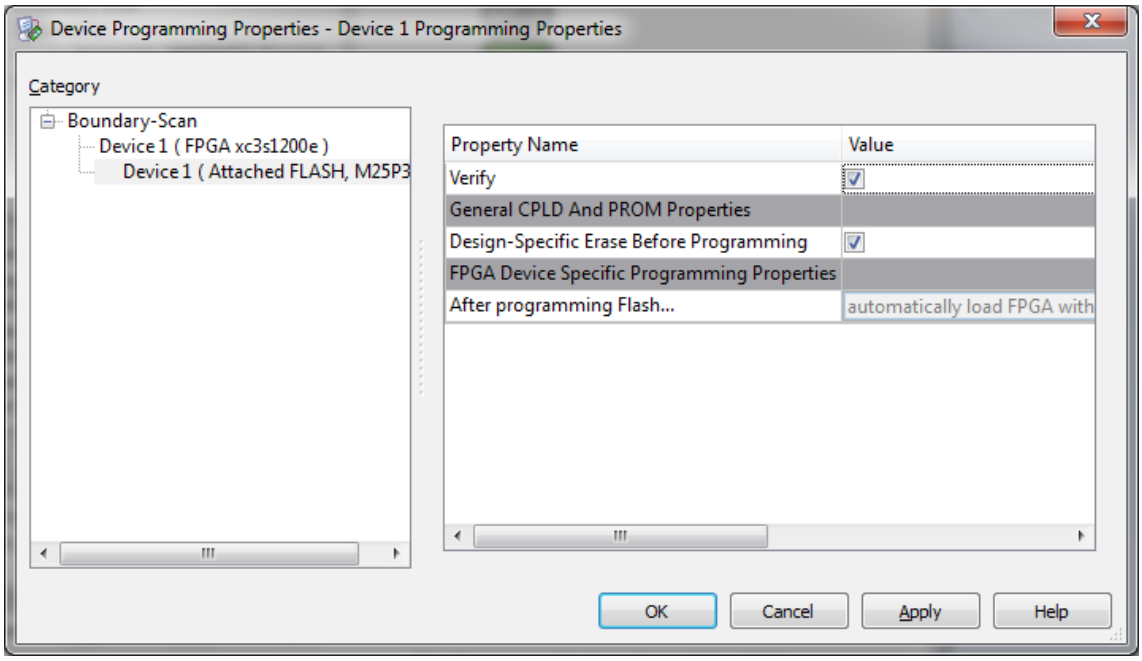
Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment.

Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.



Leave default programming properties and press “OK”.



Wait for operation to complete.