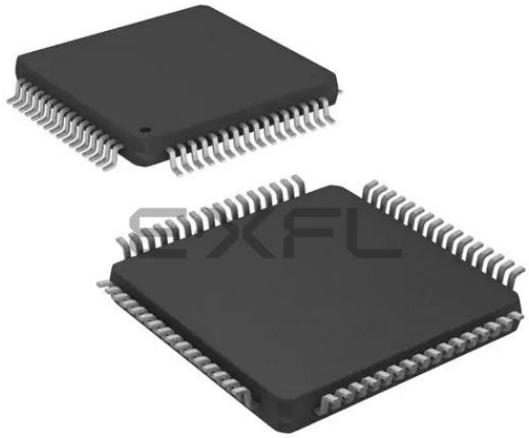

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx534f064h-v-pt

TABLE 10: PIN NAMES FOR USB AND CAN DEVICES

121-PIN TFBGA (BOTTOM VIEW)

L11

PIC32MX534F064L
PIC32MX564F064L
PIC32MX564F128L
PIC32MX575F256L
PIC32MX575F512L

L1

A11

Note: The TFBGA package skips from row "H" to row "J" and has no "I" row.

A1

Pin #	Full Pin Name	Pin #	Full Pin Name
A1	PMD4/RE4	E2	T4CK/RC3
A2	PMD3/RE3	E3	SCK2/U6TXU6TX/U3RTS/PMA5/CN8/RG6
A3	TRD0/RG13	E4	T3CK/RC2
A4	PMD0/RE0	E5	VDD
A5	PMD8/RG0	E6	PMD9/RG1
A6	C1TX/PMD10/RF1	E7	VSS
A7	VDD	E8	SDA1/INT4/RA15
A8	VSS	E9	RTCC/IC1/RD8
A9	IC5/PMD12/RD12	E10	SS1/IC2/RD9
A10	OC3/RD2	E11	SCL1/INT3/RA14
A11	OC2/RD1	F1	MCLR
B1	No Connect (NC)	F2	SCL4/SDO2/U3TX/PMA3/CN10/RG8
B2	RG15	F3	SS2/U6RX/U3CTS/PMA2/CN11/RG9
B3	PMD2/RE2	F4	SDA4/SDI2/U3RX/PMA4/CN9/RG7
B4	PMD1/RE1	F5	VSS
B5	TRD3/RA7	F6	No Connect (NC)
B6	C1RX/PMD11/RF0	F7	No Connect (NC)
B7	VCAP	F8	VDD
B8	PMRD/CN14/RD5	F9	OSC1/CLKI/RC12
B9	OC4/RD3	F10	VSS
B10	VSS	F11	OSC2/CLKO/RC15
B11	SOSCO/T1CK/CN0/RC14	G1	INT1/RE8
C1	PMD6/RE6	G2	INT2/RE9
C2	VDD	G3	TMS/RA0
C3	TRD1/RG12	G4	No Connect (NC)
C4	TRD2/RG14	G5	VDD
C5	TRCLK/RA6	G6	VSS
C6	No Connect (NC)	G7	VSS
C7	PMD15/CN16/RD7	G8	No Connect (NC)
C8	OC5/PMWR/CN13/RD4	G9	TDO/RA5
C9	VDD	G10	SDA2/RA3
C10	SOSCI/CN1/RC13	G11	TDI/RA4
C11	IC4/PMCS1/PMA14/RD11	H1	AN5/C1IN+/VBUSON/CN7/RB5
D1	T2CK/RC1	H2	AN4/C1IN-/CN6/RB4
D2	PMD7/RE7	H3	VSS
D3	PMD5/RE5	H4	VDD
D4	VSS	H5	No Connect (NC)
D5	VSS	H6	VDD
D6	No Connect (NC)	H7	No Connect (NC)
D7	PMD14/CN15/RD6	H8	VBUS
D8	PMD13/CN19/RD13	H9	VUSB3V3
D9	SDO1/OC1/INT0/RD0	H10	D+/RG2
D10	No Connect (NC)	H11	SCL2/RA2
D11	SCK1/IC3/PMCS2/PMA15/RD10	J1	AN3/C2IN+/CN5/RB3
E1	T5CK/SDI1/RC4	J2	AN2/C2IN-/CN4/RB2

Note 1: Shaded pins are 5V tolerant.

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)

L11

PIC32MX664F064L
PIC32MX664F128L
PIC32MX675F256L
PIC32MX675F512L
PIC32MX695F512L

L1

A11

A1

Note: The TFBGA package skips from row "H" to row "J" and has no "I" row.

Pin #	Full Pin Name
J3	PGED2/AN7/RB7
J4	AVDD
J5	AN11/ERXERR/AETXERR/PMA12/RB11
J6	TCK/RA1
J7	AN12/ERXD0/AECRS/PMA11/RB12
J8	No Connect (NC)
J9	No Connect (NC)
J10	SCL3/SDO3/U1TX/RF8
J11	D-/RG3
K1	PGEC1/AN1/CN3/RB1
K2	PGED1/AN0/CN2/RB0
K3	VREF+/CVREF+/AERXD3/PMA6/RA10
K4	AN8/C1OUT/RB8
K5	No Connect (NC)
K6	$\overline{SS4}$/U5RX/$\overline{U2CTS}$/RF12
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14
K8	VDD
K9	AETXD1/SCK3/U4TX/$\overline{U1RTS}$/CN21/RD15
K10	USBID/RF3
K11	SDA3/SDI3/U1RX/RF2
L1	PGEC2/AN6/OCFA/RB6
L2	VREF-/CVREF-/AERXD2/PMA7/RA9
L3	AVSS
L4	AN9/C2OUT/RB9
L5	AN10/CVREFOUT/PMA13/RB10
L6	SCK4/U5TX/$\overline{U2RTS}$/RF13
L7	AN13/ERXD1/AECOL/PMA10/RB13
L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
L9	AETXD0/$\overline{SS3}$/U4RX/$\overline{U1CTS}$/CN20/RD14
L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5

Note 1: Shaded pins are 5V tolerant.

Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the PIC32MX795F512L product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. "Introduction"** (DS60001127)
- **Section 2. "CPU"** (DS60001113)
- **Section 4. "Prefetch Cache"** (DS60001119)
- **Section 3. "Memory Organization"** (DS60001115)
- **Section 5. "Flash Program Memory"** (DS60001121)
- **Section 6. "Oscillator Configuration"** (DS60001112)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog Timer and Power-up Timer** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Capture"** (DS60001111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit (I2C)"** (DS60001116)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 35. "Ethernet Controller"** (DS60001155)

TABLE 7-4: INTERRUPT REGISTER MAP FOR PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	—	—	—	—	—	—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		—	—	—	U1IP<2:0>			U1IS<1:0>		0000
														SPI3IP<2:0>			SPI3IS<1:0>		
														I2C3IP<2:0>			I2C3IS<1:0>		
1100	IPC7	31:16	—	—	—	U3IP<2:0>			U3IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
						SPI2IP<2:0>			SPI2IS<1:0>										
						I2C4IP<2:0>			I2C4IS<1:0>										
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	U2IP<2:0>			U2IS<1:0>		0000
														SPI4IP<2:0>			SPI4IS<1:0>		
														I2C5IP<2:0>			I2C5IS<1:0>		
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
1130	IPC10	31:16	—	—	—	DMA7IP<2:0>(2)			DMA7IS<1:0>(2)		—	—	—	DMA6IP<2:0>(2)			DMA6IS<1:0>(2)		0000
		15:0	—	—	—	DMA5IP<2:0>(2)			DMA5IS<1:0>(2)		—	—	—	DMA4IP<2:0>(2)			DMA4IS<1:0>(2)		0000
1140	IPC11	31:16	—	—	—	CAN2IP<2:0>(2)			CAN2IS<1:0>(2)		—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000
1150	IPC12	31:16	—	—	—	U5IP<2:0>			U5IS<1:0>		—	—	—	U6IP<2:0>			U6IS<1:0>		0000
		15:0	—	—	—	U4IP<2:0>			U4IS<1:0>		—	—	—	ETHIP<2:0>			ETHIS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This bit is unimplemented on PIC32MX764F128H device.

3: This register does not have associated CLR, SET, and INV registers.

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)

bit 12-10 **IP01<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 9-8 **IS01<1:0>:** Interrupt Sub-priority bits
11 = Interrupt sub-priority is 3
10 = Interrupt sub-priority is 2
01 = Interrupt sub-priority is 1
00 = Interrupt sub-priority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP00<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS00<1:0>:** Interrupt Sub-priority bits
11 = Interrupt sub-priority is 3
10 = Interrupt sub-priority is 2
01 = Interrupt sub-priority is 1
00 = Interrupt sub-priority is 0

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 10-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.
Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.
Note: This must be the physical address of the destination.

11.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded Host, full-speed Device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The USB module includes the following features:

- USB Full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

TABLE 12-11: PORTG REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6180	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	—	—	03CC
6190	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	RG3	RG2	—	—	xxxx
61A0	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	—	—	xxxx
61B0	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	ODCG3	ODCG2	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 12-12: PORTG REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6180	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	TRISG1	TRISG0	F3CF
6190	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	RG3	RG2	RG1	RG0	xxxx
61A0	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	LATG1	LATG0	xxxx
61B0	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCG15	ODCG14	ODCG13	ODCG12	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	ODCG3	ODCG2	ODCG1	ODCG0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

13.2 Control Registers

TABLE 13-1: TIMER1 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0610	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0620	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 19-2: I2CxSTAT: I^{2}C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF

Legend:	HS = Set by hardware	HSC = Hardware set/cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I^{2}C master, applicable to master transmit operation)
This bit is set or cleared by hardware at the end of a slave Acknowledge.
1 = NACK received from slave
0 = ACK received from slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^{2}C master, applicable to master transmit operation)
This bit is set by hardware at the beginning of a master transmission, and is cleared by hardware at the end of a slave Acknowledge.
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
This bit is set by hardware at the detection of a bus collision.
1 = A bus collision has been detected during a master operation
0 = No collision

bit 9 **GCSTAT:** General Call Status bit
This bit is set by hardware when the address matches the general call address, and is cleared by hardware clear at a Stop detection.
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-bit Address Status bit
This bit is set by hardware upon a match of the 2nd byte of the matched 10-bit address, and is cleared by hardware at a Stop detection.
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** Write Collision Detect bit
This bit is set by hardware at the occurrence of a write to I2CxTRN while busy (cleared by software).
1 = An attempt to write the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision

bit 6 **I2COV:** Receive Overflow Flag bit
This bit is set by hardware at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ADM_EN
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0, HS	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

Legend:	HS = Set by hardware	HC = Cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ADM_EN:** Automatic Address Detect Mode Enable bit
- 1 = Automatic Address Detect mode is enabled
- 0 = Automatic Address Detect mode is disabled

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

When the ADM_EN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits
- 11 = Reserved, do not use
- 10 = Interrupt is generated and asserted while the transmit buffer is empty
- 01 = Interrupt is generated and asserted when all characters have been transmitted
- 00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):
- 1 = IrDA encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** Receiver Enable bit
- 1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module. UxRX pin is controlled by port.

bit 11 **UTXBRK:** Transmit Break bit
- 1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion.
- 0 = Break transmission is disabled or completed

bit 10 **UTXEN:** Transmit Enable bit
- 1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset. UxTX pin is controlled by port.

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

REGISTER 23-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	—	CSCNA	—	—
7:0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFS	—	SMPI<3:0>				BUFM	ALTS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

Bit Value	VREFH	VREFL
1xx	AVDD	AVss
011	External VREF+ pin	External VREF- pin
010	AVDD	External VREF- pin
001	External VREF+ pin	AVSS
000	AVDD	AVss

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
1 = Enable Offset Calibration mode
Positive and negative inputs of the S&H circuit are connected to VREFL.
0 = Disable Offset Calibration mode
The inputs to the S&H circuit are controlled by AD1CHS or AD1CSSL.

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit
1 = Scan inputs
0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1.
1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit
1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses Sample A input multiplexer settings for first sample, and then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
0 = Always use Sample A input multiplexer settings

REGISTER 24-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' (n = 0 THROUGH 31)

bit 6 **TXABAT:** Message Aborted bit(2)
1 = Message was aborted
0 = Message completed successfully

bit 5 **TXLARB:** Message Lost Arbitration bit(3)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERR:** Error Detected During Transmission bit(3)
1 = A bus error occured while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQ:** Message Send Request
TXEN = 1: (FIFO configured as a Transmit FIFO)
Setting this bit to '1' requests sending a message.
The bit will automatically clear when all the messages queued in the FIFO are successfully sent.
Clearing the bit to '0' while set ('1') will request a message abort.
TXEN = 0: (FIFO configured as a receive FIFO)
This bit has no effect.

bit 2 **RTREN:** Auto RTR Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXPR<1:0>:** Message Transmit Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).
2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
3: This bit is reset on any read of this register or when the FIFO is reset.

31.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

31.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

31.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

31.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

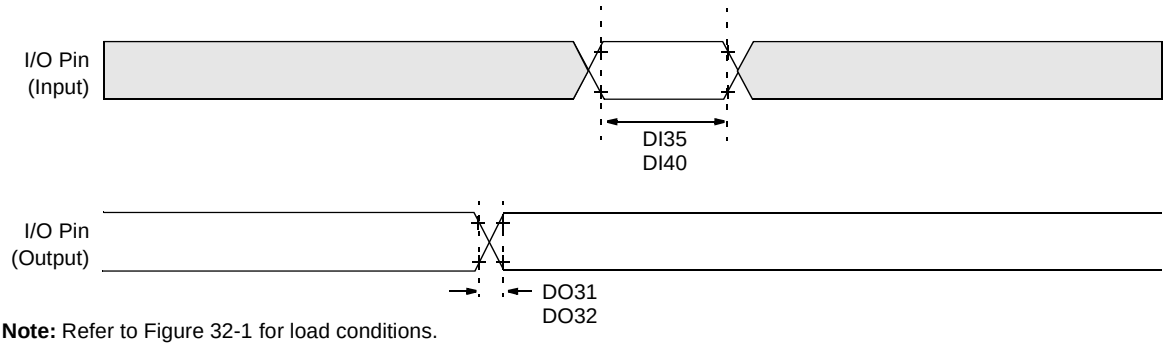
- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 32-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
LPRC @ 31.25 kHz(1)						
F21	LPRC	-15	—	+15	%	—

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 32-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

TABLE 32-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	5	15	ns	VDD < 2.5V
			—	5	10	ns	VDD > 2.5V
DO32	TIOF	Port Output Fall Time	—	5	15	ns	VDD < 2.5V
			—	5	10	ns	VDD > 2.5V
DI35	TINP	INTx Pin High or Low Time	10	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TSYSCLK	—

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

FIGURE 32-25: PARALLEL SLAVE PORT TIMING

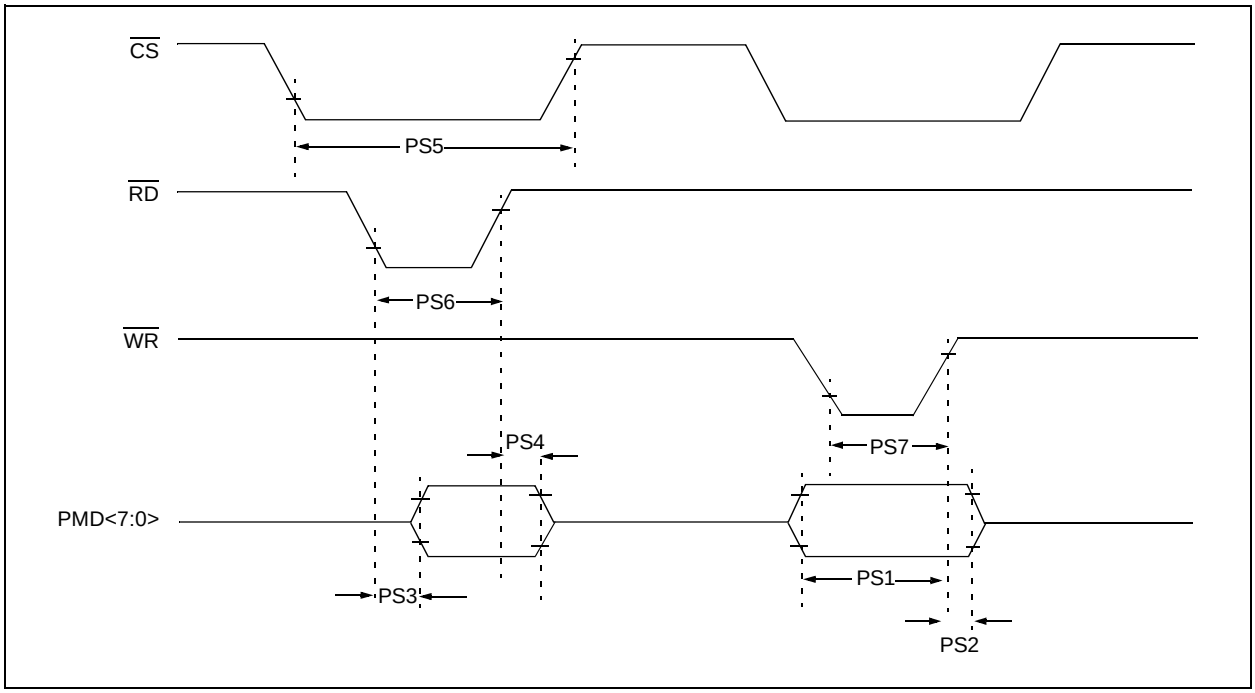


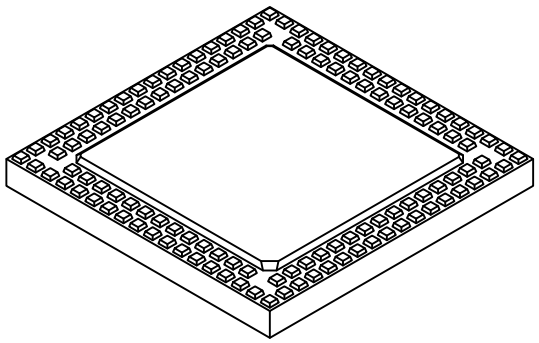
TABLE 32-39: PARALLEL SLAVE PORT REQUIREMENTS

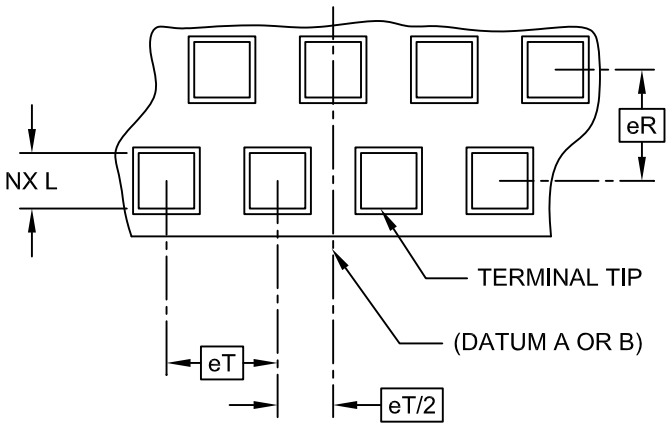
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtI	$\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid	—	—	60	ns	—
PS4	TrdH2dtI	$\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{CS}$ Active Time	TPB + 40	—	—	ns	—
PS6	TWR	$\overline{WR}$ Active Time	TPB + 25	—	—	ns	—
PS7	TRD	$\overline{RD}$ Active Time	TPB + 25	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

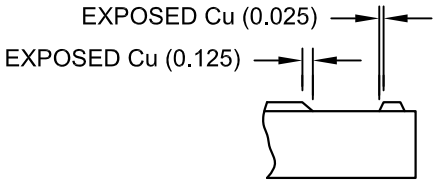
124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A



SECTION B-B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		124	
Pitch	eT		0.50 BSC	
Pitch (Inner to outer terminal ring)	eR		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	-	0.05
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	6.40	6.55	6.70
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	6.40	6.55	6.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2

TABLE B-4: SECTION UPDATES (CONTINUED)

Section Name	Update Description
7.0 "Interrupt Controller"	• Updated the following Interrupt Sources in Table 7-1: - Changed IC2AM – I2C4 Master Event to: IC4M – I2C4 Master Event - Changed IC3AM – I2C5 Master Event to: IC5M – I2C4 Master Event - Changed U1E – UART1A Error to: U1E – UART1 Error - Changed U4E – UART1B Error to: U4E – UART4 Error - Changed U1RX – UART1A Receiver to: U1RX – UART1 Receiver - Changed U4RX – UART1B Receiver to: U4RX – UART4 Receiver - Changed U1TX – UART1A Transmitter to: U1TX – UART1 Transmitter - Changed U4TX – UART1B Transmitter to: U4TX – UART4 Transmitter - Changed U6E – UART2B Error to: U6E – UART6 Error - Changed U6RX – UART2B Receiver to: U6RX – UART6 Receiver - Changed U6TX – UART2B Transmitter to: U6TX – UART6 Transmitter - Changed U5E – UART3B Error to: U5E – UART5 Error - Changed U5RX – UART3B Receiver to: U5RX – UART5 Receiver - Changed U5TX – UART3B Transmitter to: U5TX – UART5 Transmitter
1.0 "Oscillator Configuration"	Updated Figure 1-1
1.0 "Output Compare"	Updated Figure 1-1
1.0 "Ethernet Controller"	Added a note on using the Ethernet controller pins (see note above Table 1-3)
1.0 "Comparator Voltage Reference (CV_{REF})"	Updated the note in Figure 1-1
1.0 "Special Features"	Updated the bit description for bit 10 in Register 1-2 Added notes 1 and 2 to Register 1-4
1.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings: • Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} < 2.3V - 0.3V to +3.6V was updated • Voltage on V_{BUS} with respect to V_{SS} - 0.3V to +5.5V was added Updated the maximum value of DC16 as 2.1 in Table 1-4 Updated the Typical values for the following parameters: DC20b, DC20c, DC21c, DC22c and DC23c (see Table 1-5) Updated Table 1-11: • Removed the following DC Characteristics: Programming temperature 0°C ≤ TA ≤ +70°C (25°C recommended) • Updated the Minimum value for the Parameter number D131 as 2.3 • Removed the Conditions for the following Parameter numbers: D130, D131, D132, D135, D136 and D137 • Updated the condition for the parameter number D130a and D132a Updated the Minimum, Typical and Maximum values for parameter D305 in Table 1-13 Added note 2 to Table 1-18 Updated the Minimum and Maximum values for parameter F20b (see Table 1-19) Updated the following figures: • Figure 1-4 • Figure 1-9 • Figure 1-22 • Figure 1-23
Appendix A: "Migrating from PIC32MX3XX/4XX to PIC32MX5XX/ 6XX/7XX Devices"	Removed the A.3 Pin Assignments sub-section.

TABLE B-7: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
32.0 “Electrical Characteristics”	Note 4 in the Operating Current specification was updated (see Table 32-5). Note 3 in the Idle Current specification was updated (see Table 32-6). Note 6 references in the Power-Down Current specification were updated (see Table 32-7). The Program Memory parameters, D135, D136, and D137, and Note 4 were updated (see Table 32-11). The Voltage Reference Specifications were updated (see Table 32-14). Parameter DO50 (Cosco) was added to the Capacitive Loading Requirements on Output Pins (see Table 32-16). The EJTAG Timing Characteristics were updated (see Figure 32-28). The maximum value for parameters ET13 and ET14 were updated in the Ethernet Module Specifications (see Table 32-35). Parameter PM7 (TDHOLD) was updated (see Table 32-40).
34.0 “Packaging Information”	Packaging diagrams were updated.
Product Identification System	The Speed and Program Memory Size were updated and Note 1 was added.