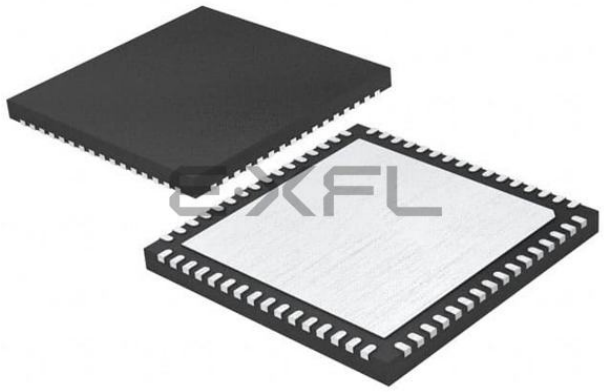

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-VQFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx534f064ht-i-mr |

**TABLE 6: PIN NAMES FOR 64-PIN USB, ETHERNET, AND CAN DEVICES**

**64-PIN QFN(3) AND TQFP (TOP VIEW)**

**PIC32MX764F128H**
**PIC32MX775F256H**
**PIC32MX775F512H**
**PIC32MX795F512H**

64 1

**QFN(3)** 64 1 **TQFP**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | ETXEN/PMD5/RE5 | 33 | USBID/RF3 |
| 2 | ETXD0/PMD6/RE6 | 34 | VBUS |
| 3 | ETXD1/PMD7/RE7 | 35 | VUSB3V3 |
| 4 | SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | 36 | D-/RG3 |
| 5 | SDA4/SDI2/U3RX/PMA4/CN9/RG7 | 37 | D+/RG2 |
| 6 | SCL4/SDO2/U3TX/PMA3/CN10/RG8 | 38 | VDD |
| 7 | MCLR | 39 | OSC1/CLKI/RC12 |
| 8 | SS2/U6RX/U3CTS/PMA2/CN11/RG9 | 40 | OSC2/CLKO/RC15 |
| 9 | VSS | 41 | Vss |
| 10 | VDD | 42 | RTCC/AERXD1/ETXD3/IC1/INT1/RD8 |
| 11 | AN5/C1IN+/VBUSON/CN7/RB5 | 43 | AERXD0/ETXD2/SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 |
| 12 | AN4/C1IN-/CN6/RB4 | 44 | ECOL/AECRSDV/SCL1/IC3/PMCS2/PMA15/INT3/RD10 |
| 13 | AN3/C2IN+/CN5/RB3 | 45 | ECRS/AEREFCLK/IC4/PMCS1/PMA14/INT4/RD11 |
| 14 | AN2/C2IN-/CN4/RB2 | 46 | OC1/INT0/RD0 |
| 15 | PGEC1/AN1/VREF-/CVREF-/CN3/RB1 | 47 | SOSCI/CN1/RC13 |
| 16 | PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0 | 48 | SOSCO/T1CK/CN0/RC14 |
| 17 | PGEC2/AN6/OCFA/RB6 | 49 | EMDIO/AEMDIO/SCK3/U4TX/U1RTS/OC2/RD1 |
| 18 | PGED2/AN7/RB7 | 50 | SDA3/SDI3/U1RX/OC3/RD2 |
| 19 | AVDD | 51 | SCL3/SDO3/U1TX/OC4/RD3 |
| 20 | AVSS | 52 | OC5/IC5/PMWR/CN13/RD4 |
| 21 | AN8/C2TX(2)/SS4/U5RX/U2CTS/C1OUT/RB8 | 53 | PMRD/CN14/RD5 |
| 22 | AN9/C2OUT/PMA7/RB9 | 54 | AETXEN/ETXERR/CN15/RD6 |
| 23 | TMS/AN10/CVREFOUT/PMA13/RB10 | 55 | ETXCLK/AERXERR/CN16/RD7 |
| 24 | TDO/AN11/PMA12/RB11 | 56 | VCAP |
| 25 | VSS | 57 | VDD |
| 26 | VDD | 58 | C1RX/AETXD1/ERXD3/RF0 |
| 27 | TCK/AN12/PMA11/RB12 | 59 | C1TX/AETXD0/ERXD2/RF1 |
| 28 | TDI/AN13/PMA10/RB13 | 60 | ERXD1/PMD0/RE0 |
| 29 | AN14/C2RX(2)/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14 | 61 | ERXD0/PMD1/RE1 |
| 30 | AN15/EMDC/AEMDC/OCFB/PMALL/PMA0/CN12/RB15 | 62 | ERXDV/ECRSDV/PMD2/RE2 |
| 31 | AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4 | 63 | ERXCLK/EREFCLKPMD3/RE3 |
| 32 | AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5 | 64 | ERXERR/PMD4/RE4 |

**Note 1:** Shaded pins are 5V tolerant.
**2:** This pin is not available on PIC32MX765F128H devices.
**3:** The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to VSS externally.

**TABLE 12: PIN NAMES FOR USB, ETHERNET, AND CAN DEVICES (CONTINUED)**

**121-PIN TFBGA (BOTTOM VIEW)**

L11

L1

A11

**PIC32MX764F128L**
**PIC32MX775F256L**
**PIC32MX775F512L**
**PIC32MX795F512L**

**Note:** The TFBGA package skips from row "H" to row "J" and has no "I" row.

A1

| Pin # | Full Pin Name |
|---|---|
| J3 | PGED2/AN7/RB7 |
| J4 | AVDD |
| J5 | AN11/ERXERR/AETXERR/PMA12/RB11 |
| J6 | TCK/RA1 |
| J7 | AN12/ERXD0/AECRS/PMA11/RB12 |
| J8 | No Connect (NC) |
| J9 | No Connect (NC) |
| J10 | SCL3/SDO3/U1TX/RF8 |
| J11 | D-/RG3 |
| K1 | PGEC1/AN1/CN3/RB1 |
| K2 | PGED1/AN0/CN2/RB0 |
| K3 | VREF+/CVREF+/AERXD3/PMA6/RA10 |
| K4 | AN8/C1OUT/RB8 |
| K5 | No Connect (NC) |
| K6 | AC1RX/SS4/U5RX/U2CTS/RF12 |
| K7 | AN14/ERXD2/AETXD3/PMALH/PMA1/RB14 |
| K8 | VDD |
| K9 | AETXD1/SCK3/U4TX/U1RTS/CN21/RD15 |
| K10 | USBID/RF3 |
| K11 | SDA3/SDI3/U1RX/RF2 |
| L1 | PGEC2/AN6/OCFA/RB6 |
| L2 | VREF-/CVREF-/AERXD2/PMA7/RA9 |
| L3 | AVSS |
| L4 | AN9/C2OUT/RB9 |
| L5 | AN10/CVREFOUT/PMA13/RB10 |
| L6 | AC1TX/SCK4/U5TX/U2RTS/RF13 |
| L7 | AN13/ERXD1/AECOL/PMA10/RB13 |
| L8 | AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15 |
| L9 | AETXD0/SS3/U4RX/U1CTS/CN20/RD14 |
| L10 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| L11 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 |

**Note 1:** This pin is not available on PIC32MX764F128L devices.
**2:** Shaded pins are 5V tolerant.

**TABLE 4-1: SFR MEMORY MAP**

| Peripheral | Virtual Address | |
|---|---|---|
| | Base | Offset Start |
| Watchdog Timer | 0xBF80 | 0x0000 |
| RTCC | | 0x0200 |
| Timer1-Timer5 | | 0x0600 |
| Input Capture 1-5 | | 0x2000 |
| Output Compare 1-5 | | 0x3000 |
| I2C1-I2C5 | | 0x5000 |
| SPI1-SPI4 | | 0x5800 |
| UART1-UART6 | | 0x6000 |
| PMP | | 0x7000 |
| ADC | | 0x9000 |
| CVREF | | 0x9800 |
| Comparator | | 0xA000 |
| Oscillator | | 0xF000 |
| Device and Revision ID | | 0xF200 |
| Flash Controller | | 0xF400 |
| Reset | | 0xF600 |
| Interrupts | 0xBF88 | 0x1000 |
| Bus Matrix | | 0x2000 |
| DMA | | 0x3000 |
| Prefetch | | 0x4000 |
| USB | | 0x5040 |
| PORTA-PORTG | | 0x6000 |
| Ethernet | | 0x9000 |
| Configuration | 0xBFC0 | 0x2FF0 |

## 7.0 INTERRUPT CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupts"** (DS60001108) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

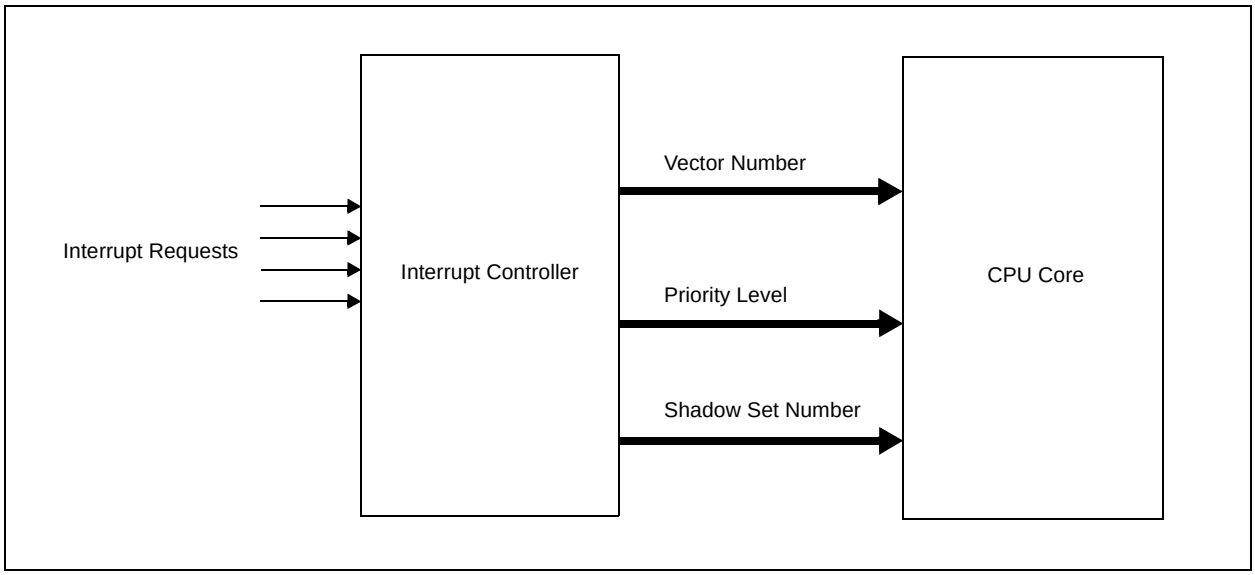
PIC32MX5XX/6XX/7XX devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The Interrupt Controller module includes the following features:

- Up to 96 interrupt sources
- Up to 64 interrupt vectors
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable sub-priority levels within each priority
- Dedicated shadow set for user-selectable priority level
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

A simplified block diagram of the Interrupt Controller module is illustrated in Figure 7-1.

**FIGURE 7-1: INTERRUPT CONTROLLER MODULE**



**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 2 **UFRCEN:** USB FRC Clock Enable bit
- 1 = Enable FRC as the clock source for the USB clock source
- 0 = Use the Primary Oscillator or USB PLL as the USB clock source

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Enable Secondary Oscillator
- 0 = Disable Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
- 1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
- 0 = Oscillator switch is complete

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

## 9.2 Control Registers

**TABLE 9-1: PREFETCH REGISTER MAP**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 4000 | CHECON(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CHECOH | 0000 |
| | | 15:0 | — | — | — | — | — | — | DCSZ<1:0> | | — | — | PREFEN<1:0> | | — | PFMWS<2:0> | | | 0007 |
| 4010 | CHEACC(1) | 31:16 | CHEWEN | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | CHEIDX<3:0> | | | | 0000 |
| 4020 | CHETAG(1) | 31:16 | LTAGBOOT | — | — | — | — | — | — | — | LTAG<23:16> | | | | | | | | 00xx |
| | | 15:0 | LTAG<15:4> | | | | | | | | | | | | LVALID | LLOCK | LTYPE | — | xxx2 |
| 4030 | CHEMSK(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LMASK<15:5> | | | | | | | | | | | — | — | — | — | — | 0000 |
| 4040 | CHEW0 | 31:16 | CHEW0<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4050 | CHEW1 | 31:16 | CHEW1<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4060 | CHEW2 | 31:16 | CHEW2<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4070 | CHEW3 | 31:16 | CHEW3<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4080 | CHELRU | 31:16 | — | — | — | — | — | — | — | CHELRU<24:16> | | | | | | | | | 0000 |
| | | 15:0 | CHELRU<15:0> | | | | | | | | | | | | | | | | 0000 |
| 4090 | CHEHIT | 31:16 | CHEHIT<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 40A0 | CHEMIS | 31:16 | CHEMIS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 40C0 | CHEPFABT | 31:16 | CHEPFABT<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset value is dependent on DEVCFGx configuration.

**REGISTER 10-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | CHAIRQ<7:0>(1) | | | | | | | |
| 15:8 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | CHSIRQ<7:0>(1) | | | | | | | |
| 7:0 | S-0 | S-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — |

| Legend: | S = Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
•
•
•
00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)

11111111 = Interrupt 255 will initiate a DMA transfer
•
•
•
00000001 = Interrupt 1 will initiate a DMA transfer
00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'
0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'
0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match
0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** See **Table 7-1: "Interrupt IRQ, Vector and Bit Location"** for the list of available interrupt IRQ sources.

## 13.2 Control Registers

**TABLE 13-1: TIMER1 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0600 | T1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | TWDIS | TWIP | — | — | — | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — | 0000 |
| 0610 | TMR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR1<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0620 | PR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR1<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

## 16.0 INPUT CAPTURE

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

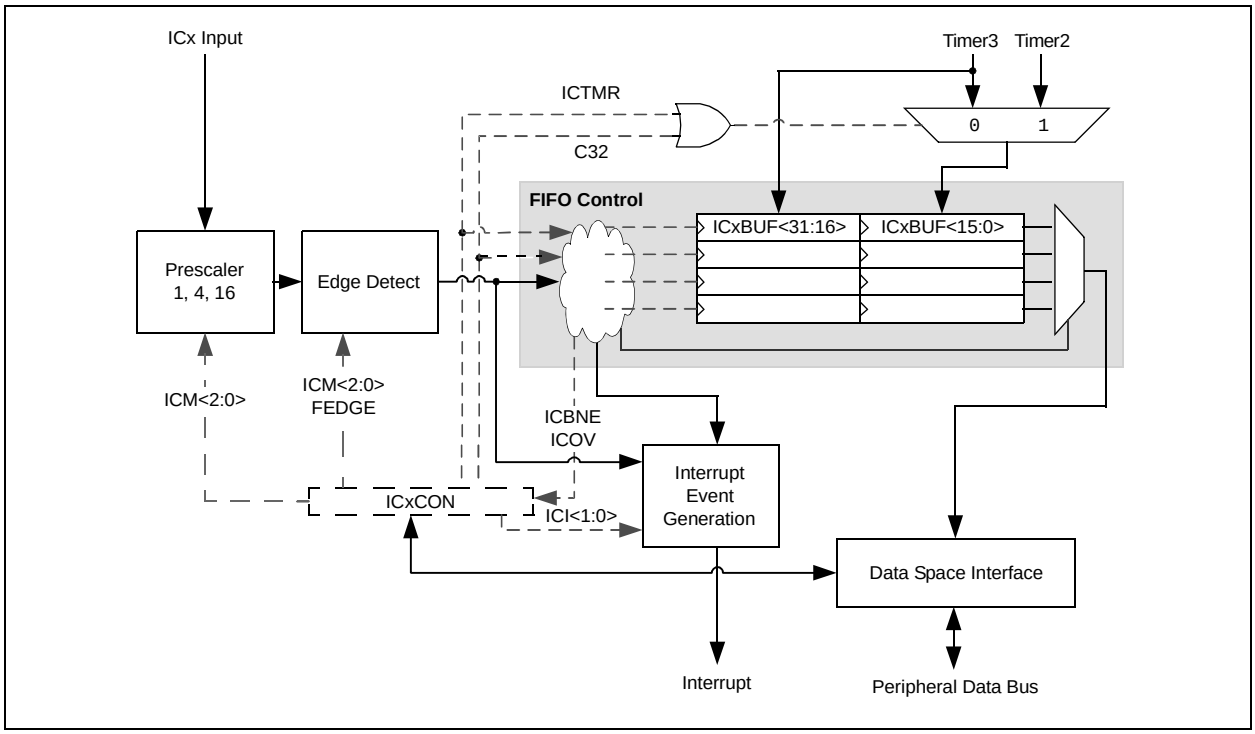
- Simple capture event modes:
  - Capture timer value on every falling edge of input at ICx pin
  - Capture timer value on every rising edge of input at ICx pin
- Capture timer value on every edge (rising and falling)
- Capture timer value on every edge (rising and falling), specified edge first.
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
  Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input Capture module can also be used to provide additional sources of external interrupts

**FIGURE 16-1: INPUT CAPTURE BLOCK DIAGRAM**



## 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

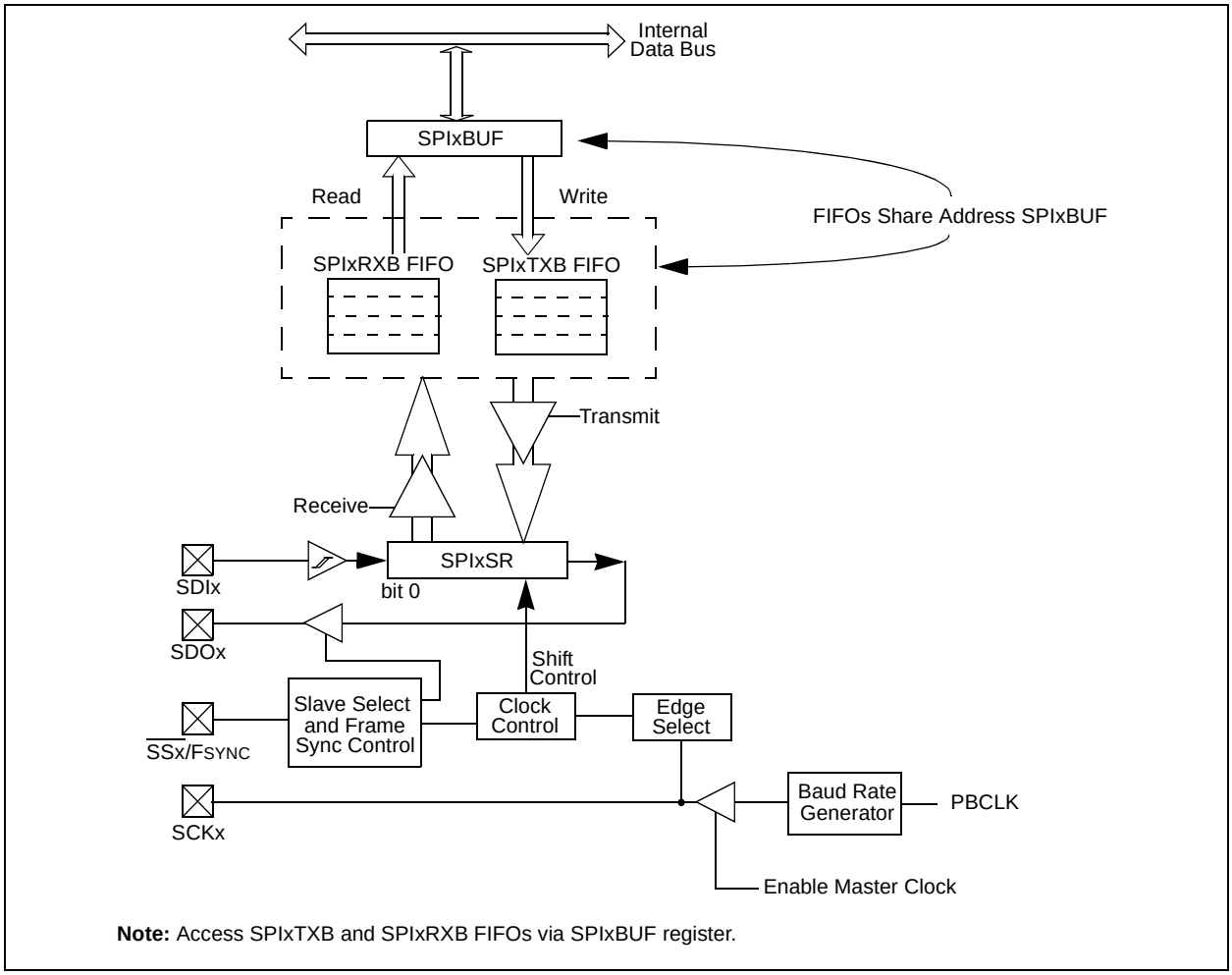
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters, etc. The PIC32 SPI module is compatible with Motorola® SPI and SIOP interfaces.

The following are some of the key features of the SPI module:

- Master mode and Slave mode support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

**FIGURE 18-1: SPI MODULE BLOCK DIAGRAM**




**Note:** Access SPIxTXB and SPIxRXB FIFOs via SPIxBUF register.

**REGISTER 19-2: I2CxSTAT: I$^2$C STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| 7:0 | R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |

| **Legend:** | HS = Set by hardware | HSC = Hardware set/cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | C = Clearable bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I$^2$C master, applicable to master transmit operation)
This bit is set or cleared by hardware at the end of a slave Acknowledge.
1 = NACK received from slave
0 = ACK received from slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I$^2$C master, applicable to master transmit operation)
This bit is set by hardware at the beginning of a master transmission, and is cleared by hardware at the end of a slave Acknowledge.
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
This bit is set by hardware at the detection of a bus collision.
1 = A bus collision has been detected during a master operation
0 = No collision

bit 9 **GCSTAT:** General Call Status bit
This bit is set by hardware when the address matches the general call address, and is cleared by hardware clear at a Stop detection.
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-bit Address Status bit
This bit is set by hardware upon a match of the 2nd byte of the matched 10-bit address, and is cleared by hardware at a Stop detection.
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** Write Collision Detect bit
This bit is set by hardware at the occurrence of a write to I2CxTRN while busy (cleared by software).
1 = An attempt to write the I2CxTRN register failed because the I$^2$C module is busy
0 = No collision

bit 6 **I2COV:** Receive Overflow Flag bit
This bit is set by hardware at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow

**REGISTER 22-5: ALRMTIME: ALARM TIME VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | HR10<3:0> | | | | HR01<3:0> | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MIN10<3:0> | | | | MIN01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | SEC10<3:0> | | | | SEC01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **HR10<3:0>:** Binary Coded Decimal value of hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary Coded Decimal value of minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary Coded Decimal value of seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

## 24.1 Control Registers

**TABLE 24-1: CAN1 REGISTER SUMMARY FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| B000 | C1CON | 31:16 | — | — | — | — | ABAT | REQOP<2:0> | | | OPMOD<2:0> | | | CANCAP | — | — | — | — | 0480 |
| | | 15:0 | ON | — | SIDLE | — | CANBUSY | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| B010 | C1CFG | 31:16 | — | — | — | — | — | — | — | — | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | 0000 |
| | | 15:0 | SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | | SJW<1:0> | | BRP<5:0> | | | | | 0000 |
| B020 | C1INT | 31:16 | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE | 0000 |
| | | 15:0 | IVRIF | WAKIF | CERRIF | SERRIF | RBOVIF | — | — | — | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF | 0000 |
| B030 | C1VEC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 |
| B040 | C1TREC | 31:16 | — | — | — | — | — | — | — | — | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN | 0000 |
| | | 15:0 | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| B050 | C1FSTAT | 31:16 | FIFOIP31 | FIFOIP30 | FIFOIP29 | FIFOIP28 | FIFOIP27 | FIFOIP26 | FIFOIP25 | FIFOIP24 | FIFOIP23 | FIFOIP22 | FIFOIP21 | FIFOIP20 | FIFOIP19 | FIFOIP18 | FIFOIP17 | FIFOIP16 | 0000 |
| | | 15:0 | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 | 0000 |
| B060 | C1RXOVF | 31:16 | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 | 0000 |
| | | 15:0 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| B070 | C1TMR | 31:16 | CANTS<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | CANTSPRE<15:0> | | | | | | | | | | | | | | | | 0000 |
| B080 | C1RXM0 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B090 | C1RXM1 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0A0 | C1RXM2 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0B0 | C1RXM3 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0C0 | C1FLTCON0 | 31:16 | FLTEN3 | MSEL3<1:0> | | FSEL3<4:0> | | | | | FLTEN2 | MSEL2<1:0> | | FSEL2<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN1 | MSEL1<1:0> | | FSEL1<4:0> | | | | | FLTEN0 | MSEL0<1:0> | | FSEL0<4:0> | | | | | 0000 |
| B0D0 | C1FLTCON1 | 31:16 | FLTEN7 | MSEL7<1:0> | | FSEL7<4:0> | | | | | FLTEN6 | MSEL6<1:0> | | FSEL6<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN5 | MSEL5<1:0> | | FSEL5<4:0> | | | | | FLTEN4 | MSEL4<1:0> | | FSEL4<4:0> | | | | | 0000 |
| B0E0 | C1FLTCON2 | 31:16 | FLTEN11 | MSEL11<1:0> | | FSEL11<4:0> | | | | | FLTEN10 | MSEL10<1:0> | | FSEL10<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN9 | MSEL9<1:0> | | FSEL9<4:0> | | | | | FLTEN8 | MSEL8<1:0> | | FSEL8<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**REGISTER 25-3: ETHTXST: ETHERNET CONTROLLER TX PACKET DESCRIPTOR START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | TXSTADDR<7:2> | | | | | | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **TXSTADDR<31:2>:** Starting Address of First Transmit Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for TX operations.
**2:** This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

**REGISTER 25-4: ETHRXST: ETHERNET CONTROLLER RX PACKET DESCRIPTOR START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | RXSTADDR<7:2> | | | | | | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **RXSTADDR<31:2>:** Starting Address of First Receive Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for RX operations.
**2:** This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

**REGISTER 27-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-1 |
| | ON(1) | — | — | — | — | VREFSEL(2) | BGSEL<1:0>(2) | |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | CVROE | CVRR | CVRSS | CVR<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit(1)
Setting or clearing this bit does not affect the other bits in this register.
1 = Module is enabled
0 = Module is disabled and does not consume current

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Voltage Reference Select bit(2)
1 = $CV_{REF} = V_{REF+}$
0 = $CV_{REF}$ is generated by the resistor network

bit 9-8 **BGSEL<1:0>:** Band Gap Reference Source bits(2)
11 = $IV_{REF} = V_{REF+}$
10 = Reserved
01 = $IV_{REF}$ = 0.6V (nominal, default)
00 = $IV_{REF}$ = 1.2V (nominal)

bit 7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** $CV_{REFOUT}$ Enable bit
1 = Voltage level is output on $CV_{REFOUT}$ pin
0 = Voltage level is disconnected from $CV_{REFOUT}$ pin

bit 5 **CVRR:** $CV_{REF}$ Range Selection bit
1 = 0 to 0.625 $CV_{RSRC}$, with $CV_{RSRC}$/24 step size
0 = 0.25 $CV_{RSRC}$ to 0.719 $CV_{RSRC}$, with $CV_{RSRC}$/32 step size

bit 4 **CVRSS:** $CV_{REF}$ Source Selection bit
1 = Comparator voltage reference source, $CV_{RSRC} = (V_{REF+}) – (V_{REF-})$
0 = Comparator voltage reference source, $CV_{RSRC} = AV_{DD} – AV_{SS}$

bit 3-0 **CVR<3:0>:** $CV_{REF}$ Value Selection $0 \le CVR<3:0> \le 15$ bits
When CVRR = 1:
$CV_{REF} = (CVR<3:0>/24) \bullet (CV_{RSRC})$
When CVRR = 0:
$CV_{REF} = 1/4 \bullet (CV_{RSRC}) + (CVR<3:0>/32) \bullet (CV_{RSRC})$

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

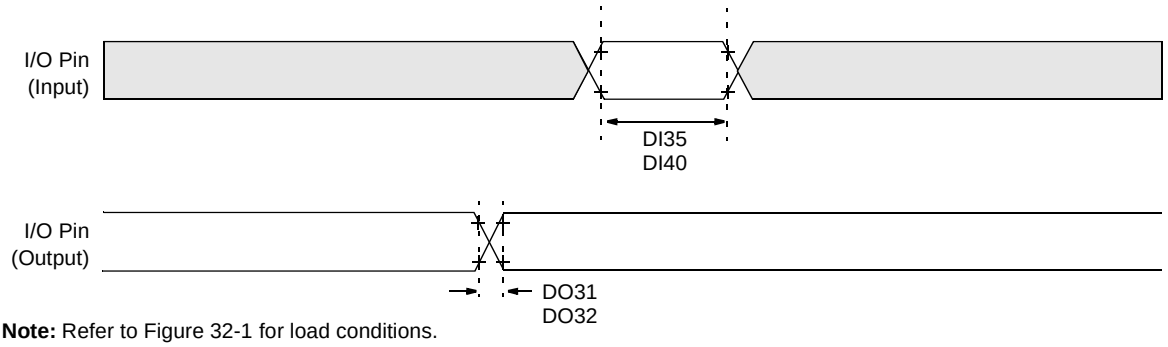
**2:** These bits are not available on PIC32MX575/675/775/795 devices. On these devices, the reset value for CVRON is '0000'.

**TABLE 32-20: INTERNAL RC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **LPRC @ 31.25 kHz(1)** | | | | | | |
| F21 | LPRC | -15 | — | +15 | % | — |

**Note 1:** Change of LPRC frequency as VDD changes.

**FIGURE 32-3: I/O TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-21: I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| DO31 | TIOR | Port Output Rise Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DO32 | TIOF | Port Output Fall Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DI35 | TINP | INTx Pin High or Low Time | 10 | — | — | ns | — |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | TSYSCLK | — |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

**2:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 32-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**

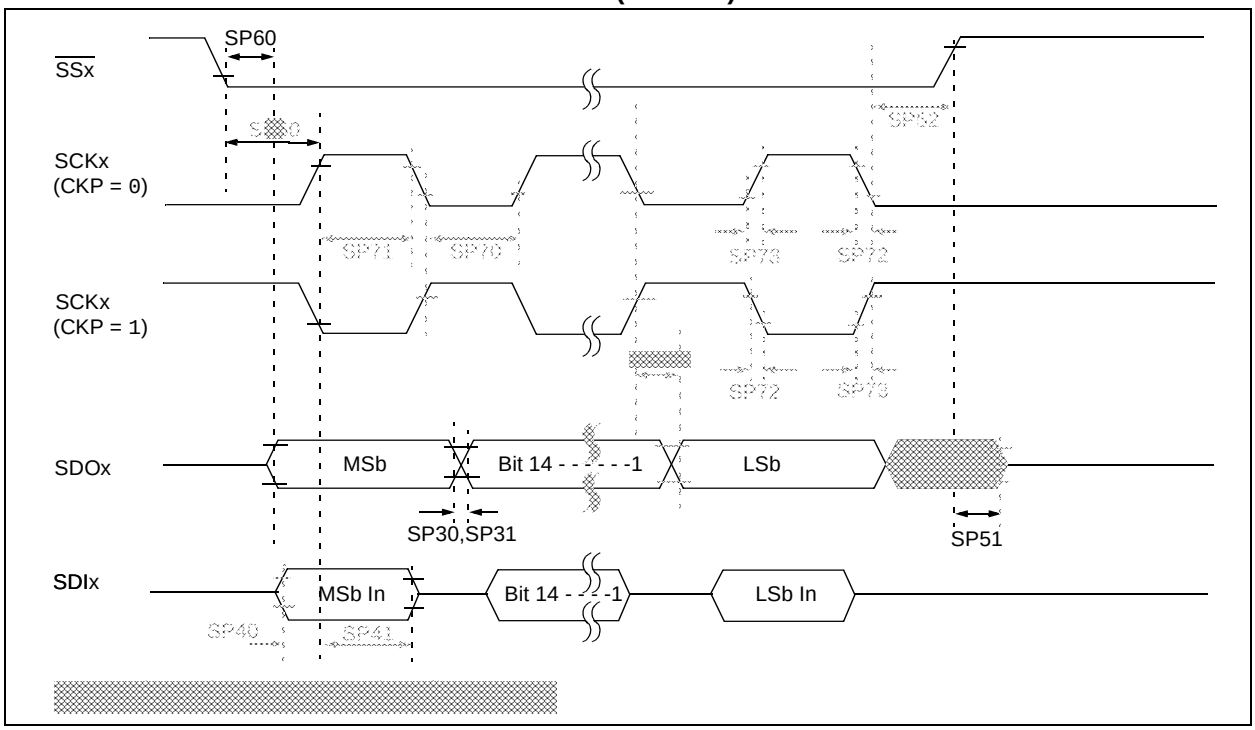



**TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time(3) | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time(3) | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | 5 | 10 | ns | — |
| SP73 | TscR | SCKx Input Rise Time | — | 5 | 10 | ns | — |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 20 | ns | VDD > 2.7V |
| | | | — | — | 30 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input | 175 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-25: PARALLEL SLAVE PORT TIMING**

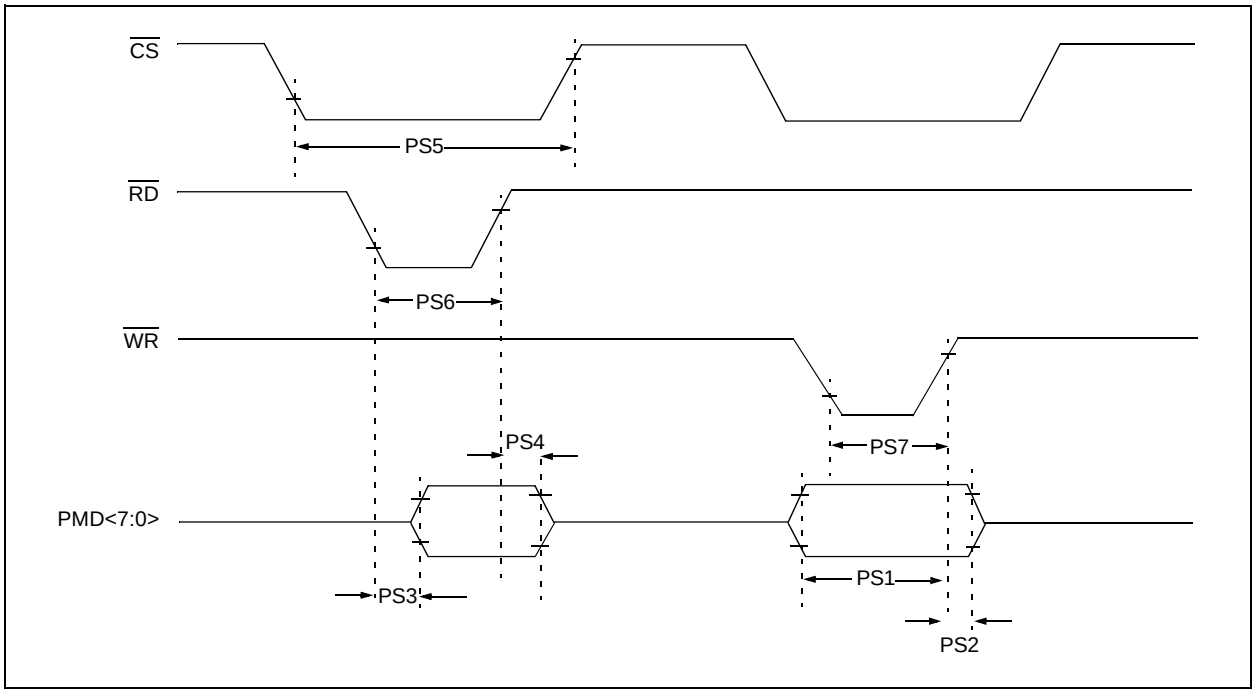


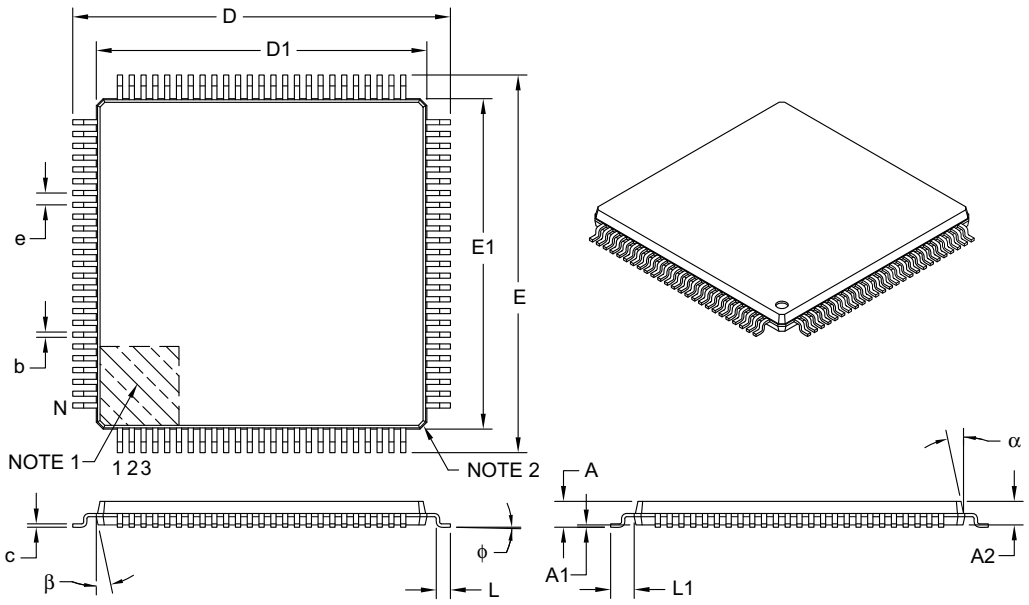

**TABLE 32-39: PARALLEL SLAVE PORT REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| PS1 | TdtV2wrH | Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time) | 20 | — | — | ns | — |
| PS2 | TwrH2dtI | $\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time) | 40 | — | — | ns | — |
| PS3 | TrdL2dtV | $\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid | — | — | 60 | ns | — |
| PS4 | TrdH2dtI | $\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid | 0 | — | 10 | ns | — |
| PS5 | Tcs | $\overline{CS}$ Active Time | TPB + 40 | — | — | ns | — |
| PS6 | TWR | $\overline{WR}$ Active Time | TPB + 25 | — | — | ns | — |
| PS7 | TRD | $\overline{RD}$ Active Time | TPB + 25 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

### 100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 16.00 BSC | |
| Overall Length | D | | 16.00 BSC | |
| Molded Package Width | E1 | | 14.00 BSC | |
| Molded Package Length | D1 | | 14.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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**TABLE B-7: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **32.0 “Electrical Characteristics”** | Note 4 in the Operating Current specification was updated (see Table 32-5).<br>Note 3 in the Idle Current specification was updated (see Table 32-6).<br>Note 6 references in the Power-Down Current specification were updated (see Table 32-7).<br>The Program Memory parameters, D135, D136, and D137, and Note 4 were updated (see Table 32-11).<br>The Voltage Reference Specifications were updated (see Table 32-14).<br>Parameter DO50 (Cosco) was added to the Capacitive Loading Requirements on Output Pins (see Table 32-16).<br>The EJTAG Timing Characteristics were updated (see Figure 32-28).<br>The maximum value for parameters ET13 and ET14 were updated in the Ethernet Module Specifications (see Table 32-35).<br>Parameter PM7 (TDHOLD) was updated (see Table 32-40). |
| **34.0 “Packaging Information”** | Packaging diagrams were updated. |
| **Product Identification System** | The Speed and Program Memory Size were updated and Note 1 was added. |