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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K × 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx534f064ht-v-mr

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIN NAMES FOR 100-PIN USB, ETHERNET, AND CAN DEVICES TABLE 9:

100-PIN TQFP (TOP VIEW)

PIC32MX764F128L PIC32MX775F256L PIC32MX775F512L PIC32MX795F512L

100

Pin #	Full Pin Name
1	AERXERR/RG15
2	VDD
3	PMD5/RE5
4	PMD6/RE6
5	PMD7/RE7
6	T2CK/RC1
7	T3CK/AC2TX ⁽¹⁾ /RC2
8	T4CK/AC2RX ⁽¹⁾ /RC3
9	T5CK/SDI1/RC4
10	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6
11	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7
12	ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8
13	MCLR
14	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9
15	Vss
16	VDD
17	TMS/RA0
18	AERXD0/INT1/RE8
19	AERXD1/INT2/RE9
20	AN5/C1IN+/VBUSON/CN7/RB5
21	AN4/C1IN-/CN6/RB4
22	AN3/C2IN+/CN5/RB3
23	AN2/C2IN-/CN4/RB2
24	PGEC1/AN1/CN3/RB1
25	PGED1/AN0/CN2/RB0
26	PGEC2/AN6/OCFA/RB6
27	PGED2/AN7/RB7
28	Vref-/CVref-/AERXD2/PMA7/RA9
29	VREF+/CVREF+/AERXD3/PMA6/RA10
30	AVdd
31	AVss
32	AN8/C1OUT/RB8
33	AN9/C2OUT/RB9
34	AN10/CVREFOUT/PMA13/RB10
35	AN11/ERXERR/AETXERR/PMA12/RB11
Note	1. This pin is not available on PIC32MX764E128L devices

Pin #	Full Pin Name
36	Vss
37	Vdd
38	TCK/RA1
39	AC1TX/SCK4/U5TX/U2RTS/RF13
40	AC1RX/SS4/U5RX/U2CTS/RF12
41	AN12/ERXD0/AECRS/PMA11/RB12
42	AN13/ERXD1/AECOL/PMA10/RB13
43	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14
44	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
45	Vss
46	Vdd
47	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
48	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
51	USBID/RF3
52	SDA3/SDI3/U1RX/RF2
53	SCL3/SDO3/U1TX/RF8
54	VBUS
55	VUSB3V3
56	D-/RG3
57	D+/RG2
58	SCL2/RA2
59	SDA2/RA3
60	TDI/RA4
61	TDO/RA5
62	Vdd
63	OSC1/CLKI/RC12
64	OSC2/CLKO/RC15
65	Vss
66	AETXCLK/SCL1/INT3/RA14
67	AETXEN/SDA1/INT4/RA15
68	RTCC/EMDIO/AEMDIO/IC1/RD8
69	SS1/IC2/RD9
70	SCK1/IC3/PMCS2/PMA15/RD10

1

This pin is not available on PIC32MX764F128L devices. 1:

2: Shaded pins are 5V tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

		Pin Nun	nber ⁽¹⁾	-	D	Duff			
Pin Name	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA	Pin Type	Buffer Type	Description		
RG0	_	90	A5	A61	I/O	ST	PORTG is a bidirectional I/O port		
RG1	—	89	E6	B50	I/O	ST			
RG6	4	10	E3	A7	I/O	ST			
RG7	5	11	F4	B6	I/O	ST			
RG8	6	12	F2	A8	I/O	ST			
RG9	8	14	F3	A9	I/O	ST			
RG12	—	96	C3	A65	I/O	ST			
RG13	—	97	A3	B55	I/O	ST			
RG14	—	95	C4	B54	I/O	ST			
RG15	—	1	B2	A2	I/O	ST			
RG2	37	57	H10	B31	I	ST	PORTG input pins		
RG3	36	56	J11	A38	I	ST			
T1CK	48	74	B11	B40	I	ST	Timer1 external clock input		
T2CK	—	6	D1	A5	I	ST	Timer2 external clock input		
T3CK	—	7	E4	B4	I	ST	Timer3 external clock input		
T4CK	—	8	E2	A6	I	ST	Timer4 external clock input		
T5CK	—	9	E1	B5	I	ST	Timer5 external clock input		
U1CTS	43	47	L9	B26	I	ST	UART1 clear to send		
U1RTS	49	48	K9	A31	0	—	UART1 ready to send		
U1RX	50	52	K11	A36	I	ST	UART1 receive		
U1TX	51	53	J10	B29	0	_	UART1 transmit		
U3CTS	8	14	F3	A9	I	ST	UART3 clear to send		
U3RTS	4	10	E3	A7	0		UART3 ready to send		
U3RX	5	11	F4	B6	I	ST	UART3 receive		
U3TX	6	12	F2	A8	0		UART3 transmit		
U2CTS	21	40	K6	A27	I	ST	UART2 clear to send		
U2RTS	29	39	L6	B22	0	—	UART2 ready to send		
U2RX	31	49	L10	B27	I	ST	UART2 receive		
U2TX	32	50	L11	A32	0		UART2 transmit		
U4RX	43	47	L9	B26	I	ST	UART4 receive		
U4TX	49	48	K9	A31	0	—	UART4 transmit		
U6RX	8	14	F3	A9	I	ST	UART6 receive		
U6TX	4	10	E3	A7	0	—	UART6 transmit		
U5RX	21	40	K6	A27	I	ST	UART5 receive		
U5TX	29	39	L6	B22	0		UART5 transmit		
SCK1	_	70	D11	B38	I/O	ST	Synchronous serial clock input/output for SPI1		
Legend: C	Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power ST = Schmitt Trigger input with CMOS levels O = Output I = Input TTI = TTI input buffer TTI = TTI input buffer I = Input								

Note 1: Pin numbers are only provided for reference. See the "Device Pin Tables" section for device pin availability.

2: See 25.0 "Ethernet Controller" for more information.

FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX575F512H, PIC32MX575F512L, PIC32MX675F512H, PIC32MX675F512L, PIC32MX775F512H AND PIC32MX775F512L DEVICES



(DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	_	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—		—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0			
15:8		BMXDKPBA<15:8>									
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
				BMXDK	PBA<7:0>						

REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** DRM Kernel Program Base Address Read-Only bits Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

Bit

Bit

Bit

Range	31/23/15/7	30/22/14/6	29/21/13/5	28/20/12/4	27/19/11/3	26/18/10/2	25/17/9/1	24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_				_		—
23.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
20.10	—	—	—	—	—	—	—	
15:8	R/W-0, HC	R/W-0	R-0, HS	R-0, HS	R-0, HSC	U-0	U-0	U-0
	WR	WREN	WRERR	LVDERR	LVDSTAT			—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	_	—	_			NVMOR	2<3:0>	
l egend:		II – Unimple	mented hit r	ad as '0'		HSC - Set an	d Cleared by	hardware
R - Read	able bit	W – Writable	≏ hit	HS – Set by	hardware	HC – Cleared	by hardware	naraware
-n = Value		'1' = Rit is so	ot	(0) = Bit is of	ared	x = Bit is upkr		
		1 – Dit 13 30	51		ealeu		101011	
bit 31-16	Unimpleme	nted: Read a	IS '0'					
bit 15	WR: Write C	ontrol bit						
DIC 10	This bit is wr	itable when V	VREN = 1 and	d the unlock	sequence is fo	llowed.		
	1 = Initiate a	Flash operat	tion Hardwar	e clears this h	nit when the o	neration compl	etes	
	0 = Flash op	eration comp	lete or inactiv	e			0.00	
hit 14	WREN. Write	e Enable bit		•				
	1 = Enable v	vrites to WR I	bit and enable	s LVD circuit				
	0 = Disable	writes to WR	bit and disabl	es LVD circu	it			
	Note:	This is the on	lv hit in this re	aister that is	reset by a dev	vice Reset		
hit 13	WRERR: W	rite Error bit(1)	gister that is		100 110301.		
DIL 15	This bit is rea	ad-only and is	s automaticall	v set by hard	ware			
	1 – Program	or erase sec	wence did no	t complete si	iccessfully			
	0 = Program	or erase sec	uence compl	eted normally	/			
bit 12		w-Voltage D	etect Error bit	(IVD circuit)	must be enabl	ed)(1)		
	This bit is rea	ad-only and is	s automaticall	y set by hard	ware.			
	1 = Low-volt	age detected	(possible dat	a corruption.	if WRERR is	set)		
	0 = Voltage I	evel is accep	table for prog	ramming	-	7		
bit 11	LVDSTAT: L	ow-Voltage D	etect Status b	oit (LVD circu	it must be ena	bled) ⁽¹⁾		
	This bit is rea	ad-only and is	s automaticall	y set, and cle	eared, by hard	ware.		
	1 = Low-volt	age event is a	active					
	0 = Low-volt	age event is i	not active					
bit 10-4	Unimpleme	nted: Read a	is '0'					
bit 3-0	NVMOP<3:0	>: NVM Ope	ration bits					
	These bits a	re writable wł	nen WREN =	0.				
	1111 = Rese	erved						
	•							
	•							
	0111 = Rese	erved						
	0110 = No c	peration						
	0101 = Prog	ıram Flash (P	PFM) erase op	eration: eras	es PFM if all p	ages are not v	vrite-protected	t
	0100 = Page	e erase opera	ation: erases p	bage selected	by NVMADD	R if it is not wr	ite-protected	
	0011 = Row	program ope	eration: progra	ams row sele	cted by NVMA	DDR if it is not	t write-protect	ed
	0010 = NOC	peration	oration: progr	ame word as	lacted by NV/		ot write prote	atod
	0001 = 0000	peration	eration, progr	anis woru se		אואטטיא וו ונ וא f	ior while-prote	CIEU

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit

Bit

Bit

Bit

Bit

Bit

Note 1: This bit is cleared by setting NVMOP == 0000b, and initiating a Flash operation (i.e., WR).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15.9	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS09	IFS08
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	IFS07	IFS06	IFS05	IFS04	IFS03	IFS02	IFS01	IFS00

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Legend:

= Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-0 IFS31-IFS00: Interrupt Flag Status bits

- 1 = Interrupt request has occurred
- 0 = Interrupt request has not occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC09	IEC08
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	IEC07	IEC06	IEC05	IEC04	IEC03	IEC02	IEC01	IEC00

Legend:

0						
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-0 IEC31-IEC00: Interrupt Enable bits

1 = Interrupt is enabled

0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 11-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24		—		—		—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	_	—	_	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	-	—	-	—	—	—
7.0	R/WC-0, HS	U-0	R/WC-0, HS					
1.0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	_	VBUSVDIF

Legend:	WC = Write '1' to clear	HS = Hardware Settable b	it
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 IDIF: ID State Change Indicator bit
 - 1 = Change in ID state detected
 - 0 = No change in ID state detected

bit 6 T1MSECIF: 1 Millisecond Timer bit

- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired
- bit 5 LSTATEIF: Line State Stable Indicator bit
 - 1 = USB line state has been stable for 1 ms, but different from last time
 - 0 = USB line state has not been stable for 1 ms

bit 4 ACTVIF: Bus Activity Indicator bit

- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected
- bit 3 SESVDIF: Session Valid Change Indicator bit
 - 1 = VBUS voltage has dropped below the session end level
 - 0 = VBUS voltage has not dropped below the session end level

bit 2 SESENDIF: B-Device VBUS Change Indicator bit

- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 Unimplemented: Read as '0'

- bit 0 VBUSVDIF: A-Device VBUS Change Indicator bit
 - 1 = Change on the session valid input detected
 - 0 = No change on the session valid input detected

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
7:0						FRMH<2:0>		

REGISTER 11-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 Unimplemented: Read as '0'

bit 2-0 **FRMH<2:0>:** Upper 3 bits of the Frame Numbers bits These register bits are updated with the current frame number whenever a SOF TOKEN is received.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		PID<	<3:0>			EP<	3:0>	

REGISTER 11-15: U1TOK: USB TOKEN REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-4 PID<3:0>: Token Type Indicator bits⁽¹⁾ 1101 = SETUP (TX) token type transaction 1001 = IN (RX) token type transaction 0001 = OUT (TX) token type transaction Note: All other values not listed, are Reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits The four bit value must specify a valid endpoint.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	_	—	—
45.0	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

REGISTER 19-1: I2CxCON: I²C CONTROL REGISTER

Legend:	HC = Cleared by hardwar	е	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** I²C Enable bit⁽¹⁾
 - 1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins
 - 0 = Disables the I²C module; all I²C pins are controlled by PORT functions
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation when device enters Idle mode
- bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
 - 1 = Release SCLx clock

0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (software can write '0' to initiate stretch and write '1' to release clock). Cleared by hardware at the beginning of a slave transmission and at the end of slave reception.

If STREN = 0:

Bit is R/S (software can only write '1' to release clock). Cleared by hardware at the beginning of slave transmission.

- bit 11 STRICT: Strict I²C Reserved Address Rule Enable bit
 - 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
 - 0 = Strict I²C reserved address rule is not enabled
- bit 10 A10M: 10-bit Slave Address bit
 - 1 = I2CxADD is a 10-bit slave address
 - 0 = I2CxADD is a 7-bit slave address
- bit 9 DISSLW: Disable Slew Rate Control bit
 - 1 = Slew rate control is disabled
 - 0 = Slew rate control is enabled
- bit 8 SMEN: SMBus Input Levels bit
 - 1 = Enable I/O pin thresholds compliant with SMBus specification
 - 0 = Disable SMBus input thresholds
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
45.0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
15:8	BUSY	IRQM<1:0>		INCM	<1:0>	—	MODE	=<1:0>
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB	<1:0> ⁽¹⁾		WAITM<3:0> ⁽¹⁾			WAITE	<1:0> ⁽¹⁾

REGISTER 21-2: PMMODE: PARALLEL PORT MODE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **BUSY:** Busy bit (only Master mode)
 - 1 = Port is busy
 - 0 = Port is not busy
- bit 14-13 IRQM<1:0>: Interrupt Request Mode bits
 - 11 = Reserved
 - 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (only Addressable Slave mode)
 - 01 = Interrupt generated at the end of the read/write cycle
 - 00 = Interrupt is not generated
- bit 12-11 INCM<1:0>: Increment Mode bits
 - 11 = Slave mode read and write buffers auto-increment (only PMMODE<1:0> = 00)
 - 10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾
 - 01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾
 - 00 = No increment or decrement of address

bit 10 Unimplemented: Read as '0'

- bit 9-8 MODE<1:0>: Parallel Port Mode Select bits
 - 11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)
 - 10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)
 - 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
 - 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)

bit 7-6 WAITB<1:0>: Data Setup to Read/Write Strobe Wait States bits⁽¹⁾

- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)
- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
22.16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
23.10	—	WAKFIL	—	—	—	SEG	SEG2PH<2:0> ^(1,4)		
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
10.0	SEG2PHTS ⁽¹⁾	SAM ⁽²⁾	:	SEG1PH<2:0>			RSEG<2:0>		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	SJW<1:	0> ⁽³⁾		BRP<5:0>					

REGISTER 24-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 Unimplemented: Read as '0'

- bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit 1 = Use CAN bus line filter for wake-up 0 = CAN bus line filter is not used for wake-up
- bit 21-19 Unimplemented: Read as '0'

bit 18-16	SEG2PH<2:0>: Phase Buffer Segment 2 bits ^(1,4)
	111 = Length is 8 x TQ
	•
	•
	•
	000 = Length is 1 x Tq
bit 15	SEG2PHTS: Phase Segment 2 Time Select bit ⁽¹⁾
	1 = Freely programmable
	0 = Maximum of SEG1PH or Information Processing Time, whichever is greater
bit 14	SAM: Sample of the CAN Bus Line bit ⁽²⁾
	1 = Bus line is sampled three times at the sample point0 = Bus line is sampled once at the sample point
bit 13-11	SEG1PH<2:0>: Phase Buffer Segment 1 bits ⁽⁴⁾
	111 = Length is 8 x TQ
	•
	•
	•
	000 = Length is 1 x TQ
Note 1:	SEG2PH \leq SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2:	3 Time bit sampling is not allowed for BRP < 2.
3:	$SJW \leq SEG2PH.$
4:	The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

U-0

U-0

U-0

U-0

U-0

U-0

KE01311	_1\ 24-21.		III. CAN I				- 0 1111000	311 31)
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
31:24								

R/W-0

RXOVFLIE

U-0

R/W-0

TXNFULLIE

R/W-0

RXFULLIE

R-0

TXNFULLIF⁽¹⁾

R-0

TXHALFIE

R/W-0

RXHALFIE

R-0

TXHALFIF

R-0

TXEMPTYIE

R/W-0

RXNEMPTYIE

R-0

TXEMPTYIF⁽¹⁾

R-0

REGISTER 24-21: CIFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)

U-0

U-0

U-0

	—	—	—	—	RXOVELIE	RXFULLIF	RXHALFIF'''	RXNEMPT	YIE
Legend:									
R = Read	lable bit	W = Writabl	le bit	U = Unimpl	emented bit,	read as '0'			
-n = Value	e at POR	'1' = Bit is s	set	'0' = Bit is c	leared	x = Bit is unkno	own		

bit 31-27 Unimplemented: Read as '0'

U-0

U-0

U-0

23:16

15:8

7:0

bit 26	TXNFULLIE: Transmit FIFO Not Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO not full
	0 = Interrupt disabled for FIFO not full
bit 25	TXHALFIE: Transmit FIFO Half Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO half full
	0 = Interrupt disabled for FIFO half full
bit 24	TXEMPTYIE: Transmit FIFO Empty Interrupt Enable bit
	1 = Interrupt enabled for FIFO empty
	0 = Interrupt disabled for FIFO empty
bit 23-20	Unimplemented: Read as '0'
bit 19	RXOVFLIE: Overflow Interrupt Enable bit
	1 = Interrupt enabled for overflow event
	0 = Interrupt disabled for overflow event
bit 18	RXFULLIE: Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO full
	0 = Interrupt disabled for FIFO full
bit 17	RXHALFIE: FIFO Half Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO half full
	0 = Interrupt disabled for FIFO half full
bit 16	RXNEMPTYIE: Empty Interrupt Enable bit
	1 = Interrupt enabled for FIFO not empty
	0 = Interrupt disabled for FIFO not empty
bit 15-11	Unimplemented: Read as '0'
bit 10	TXNFULLIF: Transmit FIFO Not Full Interrupt Flag bit ⁽¹⁾
	<u>TXEN = 1:</u> (FIFO configured as a transmit buffer)
	1 = FIFO is not full
	0 = FIFO is full
	<u>TXEN = 0:</u> (FIFO configured as a receive buffer)
	Unused reads '0'

Note 1: This bit is read-only and reflects the status of the FIFO.

REGISTER 25-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)

- bit 7 **AUTOFC:** Automatic Flow Control bit
 - 1 = Automatic Flow Control is enabled
 - 0 = Automatic Flow Control is disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 Unimplemented: Read as '0'

bit 4 MANFC: Manual Flow Control bit

- 1 = Manual Flow Control is enabled
- 0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every 128 * PTV<15:0>/2 TX clock cycles until the bit is cleared.

Note: For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 Unimplemented: Read as '0'

bit 0 BUFCDEC: Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

This bit is only used for RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

REGISTER 25-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	—	—	_	_	_		—	
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—		_	_		—	
15.9	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	HTEN	MPEN	_	NOTPM		PMMODE	<3:0>	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	CRCERREN	CRCOKEN	RUNTERREN	RUNTEN	UCEN	NOTMEEN	MCEN	BCEN

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **HTEN:** Enable Hash Table Filtering bit
 - 1 = Enable Hash Table Filtering
 - 0 = Disable Hash Table Filtering
- bit 14 **MPEN:** Magic Packet[™] Enable bit 1 = Enable Magic Packet Filtering 0 = Disable Magic Packet Filtering
- bit 13 Unimplemented: Read as '0'
- bit 12 **NOTPM:** Pattern Match Inversion bit
 - 1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
 - 0 = The Pattern Match Checksum must match for a successful Pattern Match to occur

This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

- bit 11-8 PMMODE<3:0>: Pattern Match Mode bits
 - 1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)^(1,3)
 - 1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)^(1,2)
 - 0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)⁽¹⁾
 - 0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)⁽¹⁾
 - 0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)⁽¹⁾
 - 0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)⁽¹⁾
 - 0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)⁽¹⁾
 - 0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)⁽¹⁾
 - 0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)⁽¹⁾
 - 0000 = Pattern Match is disabled; pattern match is always unsuccessful

Note 1: XOR = True when either one or the other conditions are true, but not both.

- 2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
- 3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	-	—		—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	-	—		—
15.0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
10.0	—	TXBUSE	RXBUSE	—	-	—	EWMARK	FWMARK
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	RXDONE	PKTPEND	RXACT		TXDONE	TXABORT	RXBUFNA	RXOVFLW

REGISTER 25-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15	Unimplemented: Read as '0'
bit 14	TXBUSE: Transmit BVCI Bus Error Interrupt bit
	1 = BVCI Bus Error has occurred 0 = BVCI Bus Error has not occurred
	This bit is set when the TX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.
bit 13	RXBUSE: Receive BVCI Bus Error Interrupt bit
	 1 = BVCI Bus Error has occurred 0 = BVCI Bus Error has not occurred
	This bit is set when the RX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.
bit 12-10	Unimplemented: Read as '0'
bit 9	EWMARK: Empty Watermark Interrupt bit
	1 = Empty Watermark pointer reached0 = No interrupt pending
	This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a '0' or a '1' has no effect.
bit 8	FWMARK: Full Watermark Interrupt bit
	1 = Full Watermark pointer reached0 = No interrupt pending
	This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.
bit 7	RXDONE: Receive Done Interrupt bit
	 1 = RX packet was successfully received 0 = No interrupt pending
	This bit is set whenever an RX packet is successfully received. It is cleared by either a Reset or CPU write of a '1' to the CLR register.
Note:	It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-21: ETHFCSERR: ETHERNET CONTROLLER FRAME CHECK SEQUENCE ERROR STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—		—	—	-	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	_	—	—	—	—
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0				FCSERRCN	IT<15:8>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0				FCSERRCI	NT<7:0>			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 **FCSERRCNT<15:0>:** FCS Error Count bits Increment count for frames received with FCS error and the frame length in bits is an integral multiple of 8 bits.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

REGISTER 29-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

- bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
 - 111 = 12x divider
 - 110 = 10x divider
 - 101 = 6x divider
 - 100 = 5x divider
 - 011 = 4x divider
 - 010 = 3x divider
 - 001 = 2x divider
 - 000 = 1x divider



TABLE 32-22: RESETS TIMING

AC CHA	RACTERI	ISTICS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-Temp						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions		
SY00	Τρυ	Power-up Period Internal Voltage Regulator Enabled	_	400	600	μS	-40°C to +85°C		
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.		1 μs + 8 SYSCLK cycles		_	-40°C to +85°C		
SY20	TMCLR	MCLR Pulse Width (low)	_	2	_	μS	-40°C to +85°C		
SY30	TBOR	BOR Pulse Width (low)	_	1	_	μS	-40°C to +85°C		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

NOTES:

APPENDIX B: REVISION HISTORY

Revision A (August 2009)

This is the initial released version of this document.

Revision B (November 2009)

The revision includes the following global update:

Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits.

Other major changes are referenced by their respective chapter/section in Table B-1.

Section Name	Update Description
"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"	Added the following devices: - PIC32MX575F256L - PIC32MX695F512L - PIC32MX695F512H
	The 100-pin TQFP pin diagrams have been updated to reflect the current pin name locations (see the " Pin Diagrams " section).
	Added the 121-pin Ball Grid Array (XBGA) pin diagram.
	Updated Table 1: "PIC32 USB and CAN – Features"
	Added the following tables:
	 Table 4: "Pin Names: PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L and PIC32MX575F512L Devices"
	 Table 5: "Pin Names: PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L and PIC32MX695F512L Devices"
	 Table 6: "Pin Names: PIC32MX775F256L, PIC32MX775F512L and PIC32MX795F512L Devices"
	Updated the following pins as 5V tolerant:
	- 64-pin QFN: Pin 36 (D-/RG3) and Pin 37 (D+/RG2)
	- 64-pin TQFP: Pin 36 (D-/RG3) and Pin 37 (D+/RG2)
	- 100-pin TQFP: Pin 56 (D-/RG3) and Pin 57 (D+/RG2)
1.0 "Guidelines for Getting Started	Removed the last sentence of 1.3.1 "Internal Regulator Mode".
with 52-bit Microcontrollers"	Removed Section 2.3.2 "External Regulator Mode"

TABLE B-1: MAJOR SECTION UPDATES