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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx534f064l-i-bg

PIC32MX5XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
AC2TX	—	7	E4	B4	O	—	Alternate CAN2 bus transmit pin
ERXD0	61	41	J7	B23	I	ST	Ethernet Receive Data 0[2]
ERXD1	60	42	L7	A28	I	ST	Ethernet Receive Data 1[2]
ERXD2	59	43	K7	B24	I	ST	Ethernet Receive Data 2[2]
ERXD3	58	44	L8	A29	I	ST	Ethernet Receive Data 3[2]
ERXERR	64	35	J5	B20	I	ST	Ethernet receive error input[2]
ERXDV	62	12	F2	A8	I	ST	Ethernet receive data valid[2]
ECRSDV	62	12	F2	A8	I	ST	Ethernet carrier sense data valid[2]
ERXCLK	63	14	F3	A9	I	ST	Ethernet receive clock[2]
EREFCLK	63	14	F3	A9	I	ST	Ethernet reference clock[2]
ETXD0	2	88	A6	A60	O	—	Ethernet Transmit Data 0[2]
ETXD1	3	87	B6	B49	O	—	Ethernet Transmit Data 1[2]
ETXD2	43	79	A9	B43	O	—	Ethernet Transmit Data 2[2]
ETXD3	42	80	D8	A54	O	—	Ethernet Transmit Data 3[2]
ETXERR	54	89	E6	B50	O	—	Ethernet transmit error[2]
ETXEN	1	83	D7	B45	O	—	Ethernet transmit enable[2]
ETXCLK	55	84	C7	A56	I	ST	Ethernet transmit clock[2]
ECOL	44	10	E3	A7	I	ST	Ethernet collision detect[2]
ECRS	45	11	F4	B6	I	ST	Ethernet carrier sense[2]
EMDC	30	71	C11	A46	O	—	Ethernet management data clock[2]
EMDIO	49	68	E9	B37	I/O	—	Ethernet management data[2]
AERXD0	43	18	G1	A11	I	ST	Alternate Ethernet Receive Data 0[2]
AERXD1	42	19	G2	B10	I	ST	Alternate Ethernet Receive Data 1[2]
AERXD2	—	28	L2	A21	I	ST	Alternate Ethernet Receive Data 2[2]
AERXD3	—	29	K3	B17	I	ST	Alternate Ethernet Receive Data 3[2]
AERXERR	55	1	B2	A2	I	ST	Alternate Ethernet receive error input[2]
AERXDV	—	12	F2	A8	I	ST	Alternate Ethernet receive data valid[2]
AECRSDV	44	12	F2	A8	I	ST	Alternate Ethernet carrier sense data valid[2]
AERXCLK	—	14	F3	A9	I	ST	Alternate Ethernet receive clock[2]
AEREFCLK	45	14	F3	A9	I	ST	Alternate Ethernet reference clock[2]
AETXD0	59	47	L9	B26	O	—	Alternate Ethernet Transmit Data 0[2]
AETXD1	58	48	K9	A31	O	—	Alternate Ethernet Transmit Data 1[2]
AETXD2	—	44	L8	A29	O	—	Alternate Ethernet Transmit Data 2[2]
AETXD3	—	43	K7	B24	O	—	Alternate Ethernet Transmit Data 3[2]
AETXERR	—	35	J5	B20	O	—	Alternate Ethernet transmit error[2]
AETXEN	54	67	E8	A44	O	—	Alternate Ethernet transmit enable[2]
AETXCLK	—	66	E11	B36	I	ST	Alternate Ethernet transmit clock[2]
AECOL	—	42	L7	A28	I	ST	Alternate Ethernet collision detect[2]

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   P = Power
ST = Schmitt Trigger input with CMOS levels   O = Output   I = Input
TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

2: See **25.0 "Ethernet Controller"** for more information.

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUS

> **Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX5XX/6XX/7XX family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All V$_{DD}$ and V$_{SS}$ pins (see **2.2 "Decoupling Capacitors"**)
- All AV$_{DD}$ and AV$_{SS}$ pins even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- V$_{CAP}$ pin (see **2.3 "Capacitor on Internal Voltage Regulator (V$_{CAP}$)"**)
- MCLR pin (see **2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **2.8 "External Oscillator Pins"**)

The following pin may be required, as well: V$_{REF}$+/ V$_{REF}$- pins used when external voltage reference for ADC module is implemented.

> **Note:** The AV$_{DD}$ and AV$_{SS}$ pins must be connected, regardless of the ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as V$_{DD}$, V$_{SS}$, AV$_{DD}$ and AV$_{SS}$ is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

3.0 CPU

> **Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS60001113) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). Resources for the MIPS32® M4K® Processor Core are available at http://www.imgtec.com.

The MIPS32® M4K® Processor core is the heart of the PIC32MX5XX/6XX/7XX family processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2)
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - WAIT instruction
  - Conditional move instructions (MOVN, MOVZ)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions

- MIPS16e® code compression
  - 16-bit encoding of 32-bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
  - Improved support for handling 8-bit and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- Simple dual bus interface
  - Independent 32-bit address and data busses
  - Transactions can be aborted to improve interrupt latency
- Autonomous multiply/divide unit
  - Maximum issue rate of one 32x16 multiply per clock
  - Maximum issue rate of one 32x32 multiply every other clock
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (*rs*) sign extension-dependent)
- Power control
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by WAIT instruction)
  - Extensive use of local gated clocks
- EJTAG debug and instruction trace
  - Support for single stepping
  - Virtual instruction and data address/value
  - Breakpoints
  - PC tracing with trace compression

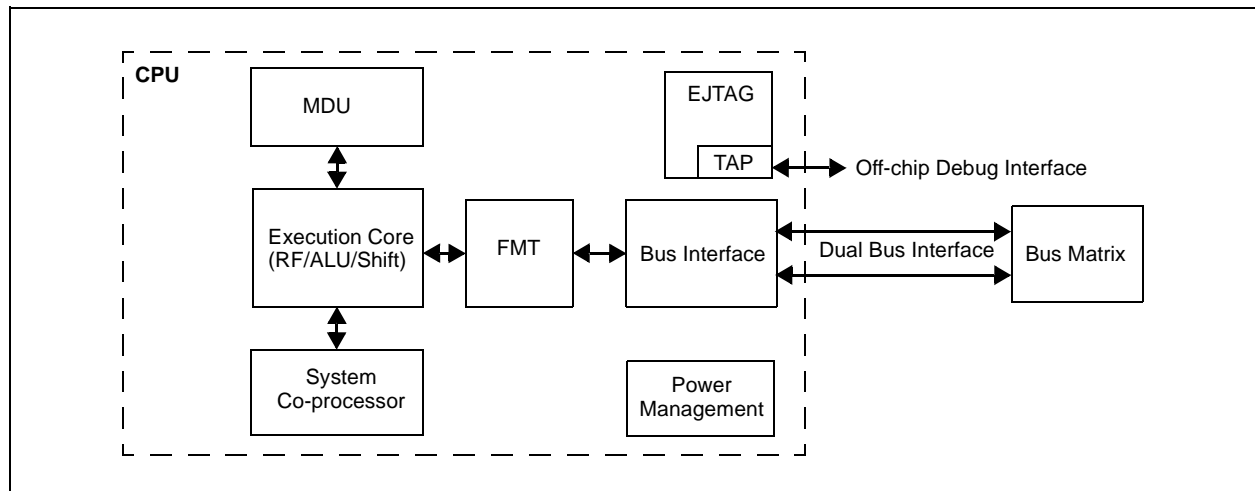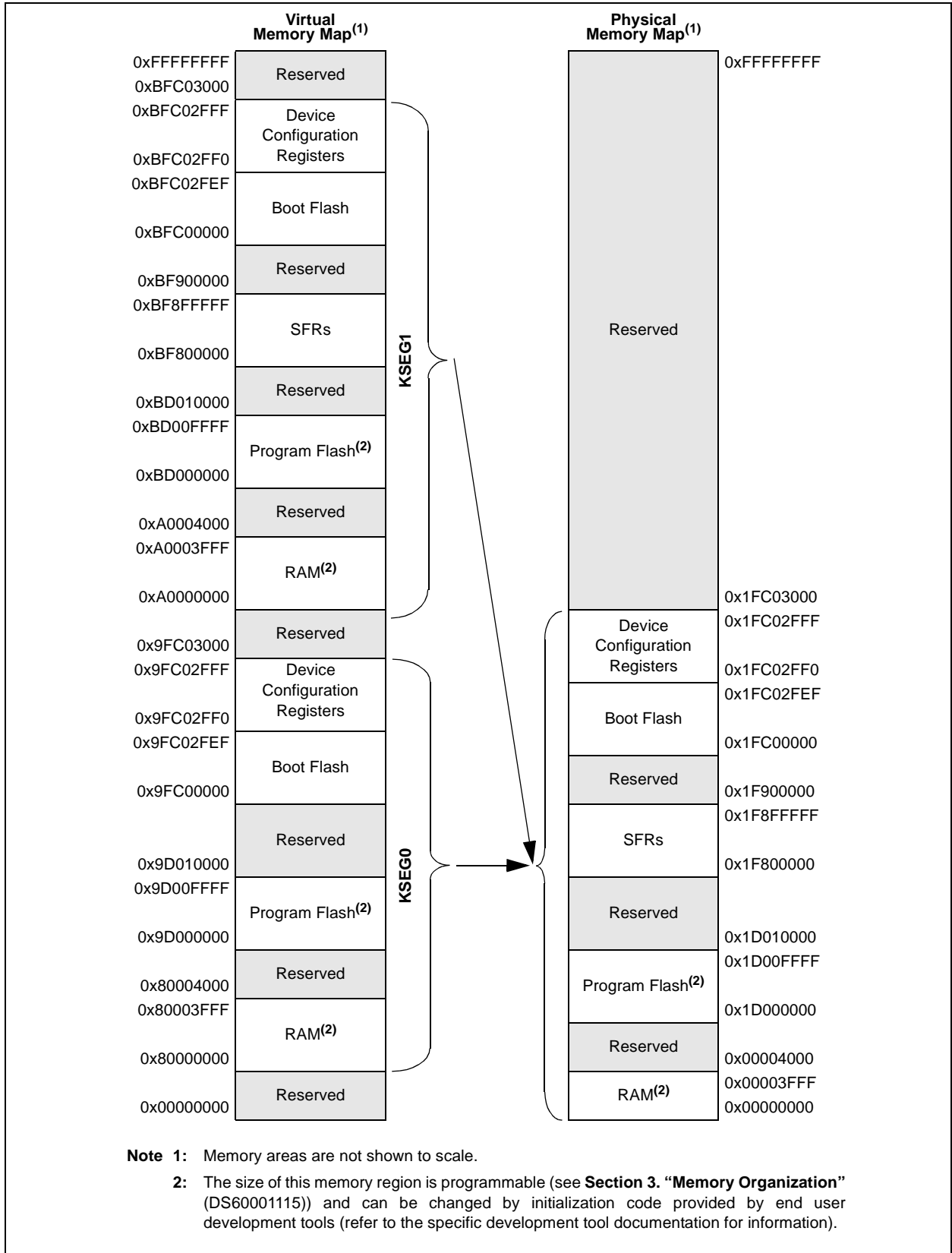**FIGURE 3-1:** **MIPS32® M4K® PROCESSOR CORE BLOCK DIAGRAM**

FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX534F064H AND PIC32MX534F064L DEVICES

Virtual Memory Map[1]

Address	Region
0xFFFFFFFF	Reserved
0xBFC03000	
0xBFC02FFF	Device Configuration Registers
0xBFC02FF0	
0xBFC02FEF	Boot Flash
0xBFC00000	
0xBF900000	Reserved
0xBF8FFFFF	SFRs
0xBF800000	
0xBD010000	Reserved
0xBD00FFFF	Program Flash[2]
0xBD000000	
0xA0004000	Reserved
0xA0003FFF	RAM[2]
0xA0000000	
0x9FC03000	Reserved
0x9FC02FFF	Device Configuration Registers
0x9FC02FF0	
0x9FC02FEF	Boot Flash
0x9FC00000	
0x9D010000	Reserved
0x9D00FFFF	Program Flash[2]
0x9D000000	
0x80004000	Reserved
0x80003FFF	RAM[2]
0x80000000	
0x00000000	Reserved

KSEG1, KSEG0

Physical Memory Map[1]

Address	Region
0xFFFFFFFF	Reserved
0x1FC03000	
0x1FC02FFF	Device Configuration Registers
0x1FC02FF0	
0x1FC02FEF	Boot Flash
0x1FC00000	
0x1F900000	Reserved
0x1F8FFFFF	SFRs
0x1F800000	
0x1D010000	Reserved
0x1D00FFFF	Program Flash[2]
0x1D000000	
0x00004000	Reserved
0x00003FFF	RAM[2]
0x00000000	

Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
	—	—	—	—	—	—	CMR	VREGS
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR[1]	POR[1]

Legend:		HS = Set by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = Configuration mismatch Reset has occurred
0 = Configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
1 = Regulator is enabled and is on during Sleep mode
0 = Regulator is set to Stand-by Tracking mode

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit[1]
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit[1]
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view the next detection.

REGISTER 10-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size
- •
- •
- •

0000000000000010 = 2 byte source size
0000000000000001 = 1 byte source size
0000000000000000 = 65,536 byte source size

REGISTER 10-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size
- •
- •
- •

0000000000000010 = 2 byte destination size
0000000000000001 = 1 byte destination size
0000000000000000 = 65,536 byte destination size

11.0 USB ON-THE-GO (OTG)

Note:	This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded Host, full-speed Device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The USB module includes the following features:

- USB Full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note:	The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

PIC32MX5XX/6XX/7XX

REGISTER 11-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE[1]	URSTIE[2] / DETACHIE[3]

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit

1 = STALL interrupt is enabled
0 = STALL interrupt is disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit

1 = ATTACH interrupt is enabled
0 = ATTACH interrupt is disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit

1 = RESUME interrupt is enabled
0 = RESUME interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit

1 = Idle interrupt is enabled
0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit

1 = TRNIF interrupt is enabled
0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit

1 = SOFIF interrupt is enabled
0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit[1]

1 = USB Error interrupt is enabled
0 = USB Error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit[2]

1 = URSTIF interrupt is enabled
0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit[3]

1 = DATTCHIF interrupt is enabled
0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.
   2: Device mode.
   3: Host mode.

REGISTER 21-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits[1]

`1111` = Wait of 16 T_{PB}

-
-
-

`0001` = Wait of 2 T_{PB}
`0000` = Wait of 1 T_{PB} (default)

bit 1-0 **WAITE<1:0>:** Data Hold After Read/Write Strobe Wait States bits[1]

`11` = Wait of 4 T_{PB}
`10` = Wait of 3 T_{PB}
`01` = Wait of 2 T_{PB}
`00` = Wait of 1 T_{PB} (default)

For Read operations:
`11` = Wait of 3 T_{PB}
`10` = Wait of 2 T_{PB}
`01` = Wait of 1 T_{PB}
`00` = Wait of 0 T_{PB} (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 T_{PBCLK} cycle for a write operation; WAITB = `1` T_{PBCLK} cycle, WAITE = `0` T_{PBCLK} cycles for a read operation.

2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

REGISTER 21-5:   PMSTAT: PARALLEL PORT STATUS REGISTER (ONLY SLAVE MODES)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:

HS = Set by Hardware   SC = Cleared by software
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as '0'
-n = Value at POR   '1' = Bit is set   '0' = Bit is cleared   x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable input buffer registers are full
0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
0 = An overflow has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits
1 = Input buffer contains data that has not been read (reading buffer will clear this bit)
0 = Input buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable output buffer registers are empty
0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty output byte buffer (must be cleared in software)
0 = An underflow has not occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains data that has not been transmitted

24.0 CONTROLLER AREA NETWORK (CAN)

> **Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Controller Area Network (CAN) module supports the following key features:

• Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
• Message Reception and Transmission:
  - 32 message FIFOs
  - Each FIFO can have up to 32 messages for a total of 1024 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 32 acceptance filters for message filtering
  - Four acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
• Additional Features:
  - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus master on the PIC32 system bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 24-1 illustrates the general structure of the CAN module.

FIGURE 24-1: PIC32 CAN MODULE BLOCK DIAGRAM
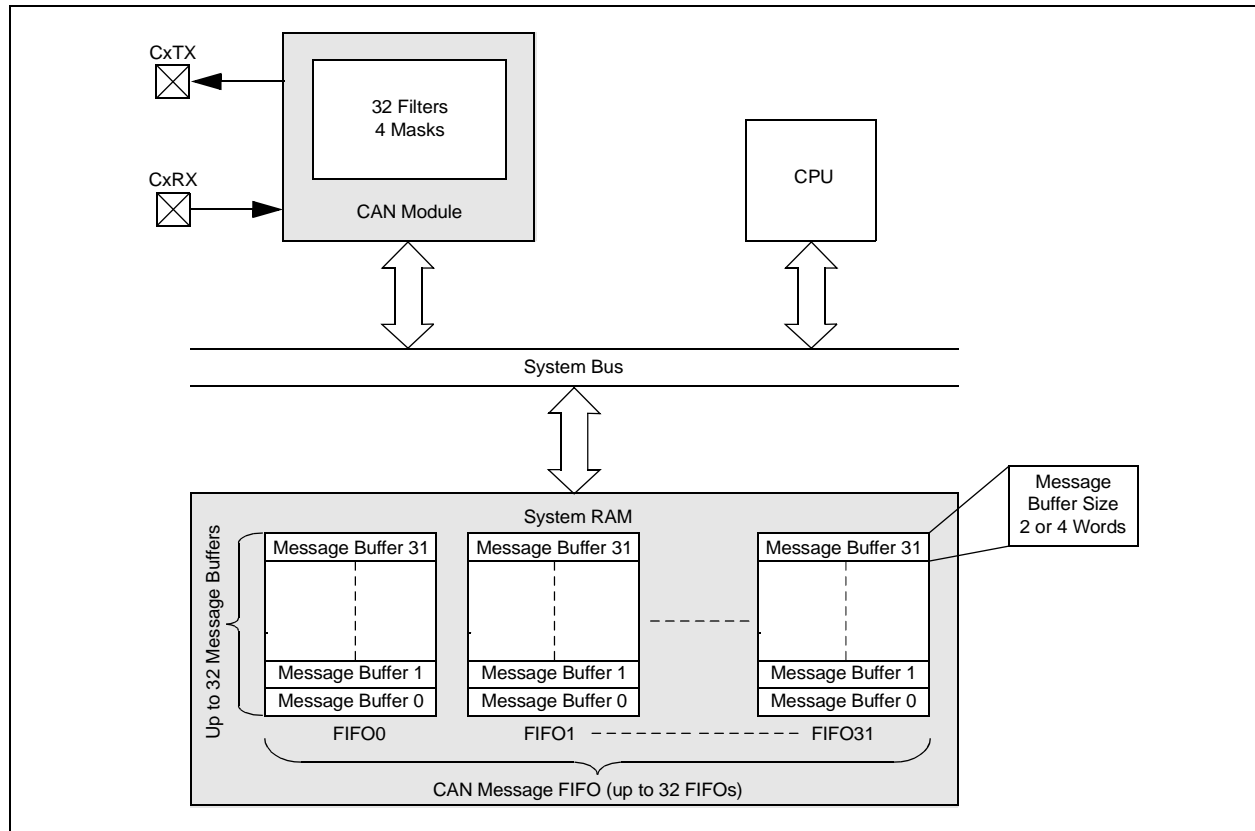
REGISTER 25-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16   **Unimplemented:** Read as '0'

bit 15-0   **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

Note 1:	This register is only used for RX operations.
2:	This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.
3:	It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-21: ETHFCSERR: ETHERNET CONTROLLER FRAME CHECK SEQUENCE ERROR STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FCSERRCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FCSERRCNT<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FCSERRCNT<15:0>:** FCS Error Count bits

Increment count for frames received with FCS error and the frame length in bits is an integral multiple of 8 bits.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

REGISTER 25-27: EMAC1CLRT: ETHERNET CONTROLLER MAC COLLISION WINDOW/RETRY LIMIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	CWINDOW<5:0>					
7:0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	—	RETX<3:0>			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13-8 **CWINDOW<5:0>:** Collision Window bits

This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RETX<3:0>:** Retransmission Maximum bits

This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts (attemptLimit) to be 0xF (15d). Its default is '0xF'.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 25-37:   EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR6<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR5<7:0>							

Legend:		P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16   **Unimplemented:** Read as '0'

bit 15-8   **STNADDR6<7:0>:** Station Address Octet 6 bits
These bits hold the sixth transmitted octet of the station address.

bit 7-0   **STNADDR5<7:0>:** Station Address Octet 5 bits
These bits hold the fifth transmitted octet of the station address.

Note 1:	Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.
2:	This register is loaded at reset from the factory preprogrammed station address.

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TABLE 29-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2FF0	DEVCFG3	31:16	FVBUSONIO	FUSBIDIO	—	—	—	FCANIO	FETHIO	FMIIEN	—	—	—	—	—	FSRSSEL<2:0>			xxxx
		15:0	USERID<15:0>																xxxx
2FF4	DEVCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>			xxxx
		15:0	UPLLEN	—	—	—	—	UPLLIDIV<2:0>			—	FPLLMUL<2:0>			—	FPLLIDIV<2:0>			xxxx
2FF8	DEVCFG1	31:16	—	—	—	—	—	—	—	—	FWDTEN	—	—	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>		IESO	—	FSOSCEN	—	—	FNOSC<2:0>			xxxx
2FFC	DEVCFG0	31:16	—	—	—	CP	—	—	—	BWP	—	—	—	—	PWP<7:4>				xxxx
		15:0	PWP<3:0>				—	—	—	—	—	—	—	—	ICESEL	—	DEBUG<1:0>		xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 29-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets[1]
F200	DDPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	JTAGEN	TROEN	—	TDOEN	0008
F220	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx
F230	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: Reset values are dependent on the device variant. Refer to *"PIC32MX5XX/6XX/7XX Family Silicon Errata and Data Sheet Clarification"* (DS80000480) for more information.

NOTES:

32.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX5XX/6XX/7XX AC characteristics and timing parameters.

FIGURE 32-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

Load Condition 1 – for all pins except OSC2   Load Condition 2 – for OSC2

$V_{DD}/2$

R_L

Pin

C_L

V_{SS}

Pin

C_L

V_{SS}

$R_L = 464\Omega$
$C_L = 50$ pF for all pins
        50 pF for OSC2 pin (EC mode)
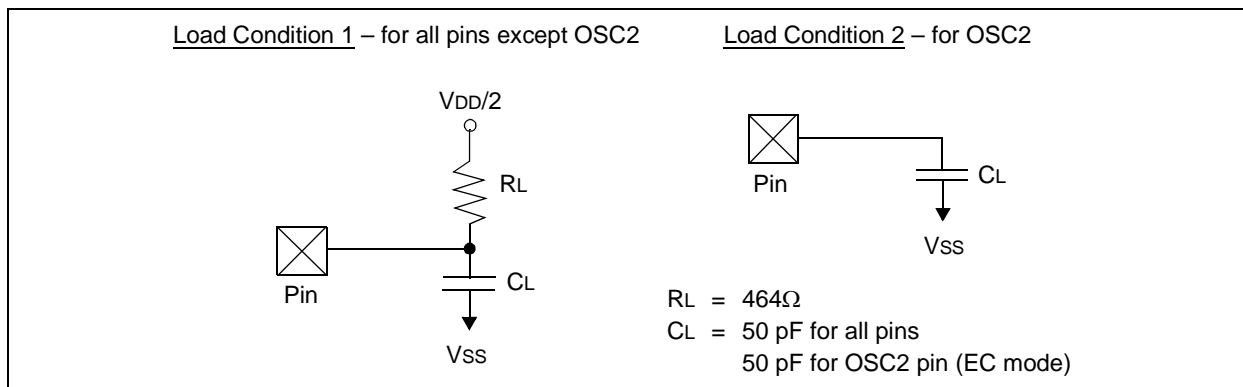
TABLE 32-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40°C \le T_A \le +85°C$ for Industrial $-40°C \le T_A \le +105°C$ for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical[1]	Max.	Units	Conditions
DO50	Cosco	OSC2 pin	—	—	15	pF	In XT and HS modes when an external crystal is used to drive OSC1
DO56	C_{IO}	All I/O pins and OSC2	—	—	50	pF	In EC mode
DO58	C_B	SCLx, SDAx	—	—	400	pF	In I²C mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 32-2: EXTERNAL CLOCK TIMING

OSC1

OS20

OS30

OS31

OS30

OS31
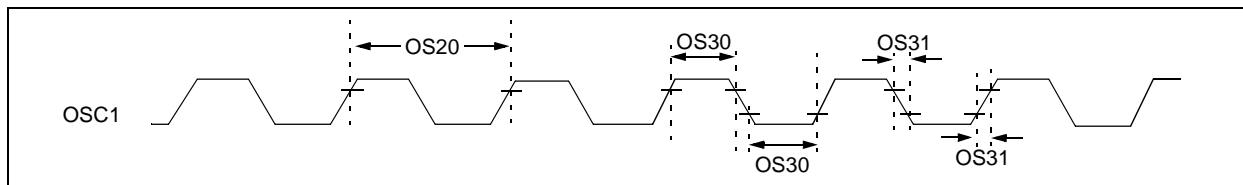
TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics[1]	Min.	Typical[2]	Max.	Units	Conditions
SP51	$T_{SSH2DOZ}$	$\overline{SSx}$ ↑ to SDOx Output High-Impedance[4]	5	—	25	ns	—
SP52	$T_{SCH2SSH}$ $T_{SCL2SSH}$	$\overline{SSx}$ ↑ after SCKx Edge	T_{SCK} + 20	—	—	ns	—
SP60	$T_{SSL2DOV}$	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	25	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

    2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

    3: The minimum clock period for SCKx is 40 ns.

    4: Assumes 50 pF load on all SPIx pins.

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