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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I <sup>2</sup> C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx534f064l-v-bg">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx534f064l-v-bg</a>

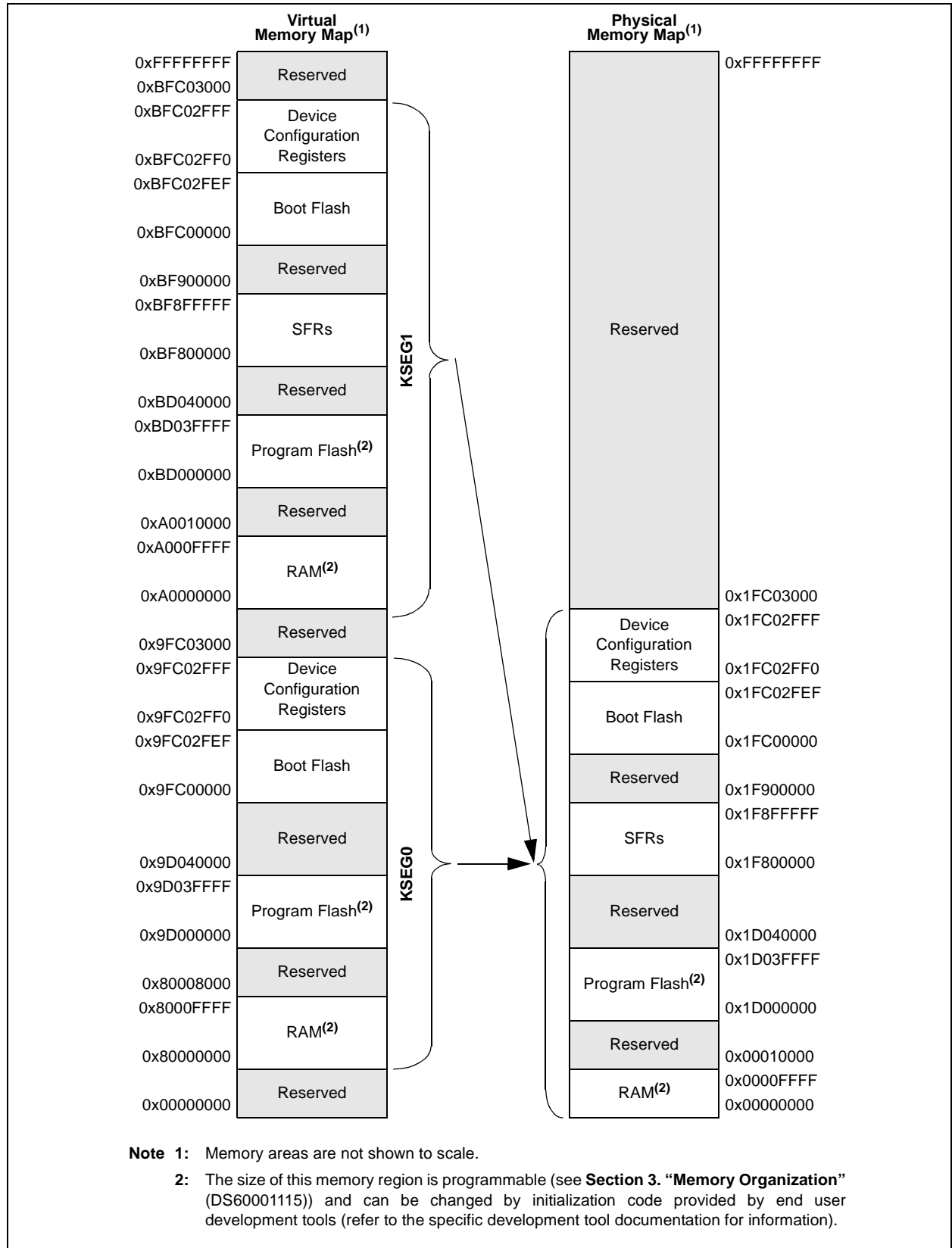
# PIC32MX5XX/6XX/7XX

**TABLE 7: PIN NAMES FOR 100-PIN USB AND CAN DEVICES**

100-PIN TQFP (TOP VIEW)			
<b>PIC32MX534F064L</b> <b>PIC32MX564F064L</b> <b>PIC32MX564F128L</b> <b>PIC32MX575F512L</b> <b>PIC32MX575F256L</b>		100 1	
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RG15	36	Vss
2	VDD	37	VDD
3	PMD5/RE5	38	TCK/RA1
4	PMD6/RE6	39	AC1TX/SCK4/U5TX/U2RTS/RF13
5	PMD7/RE7	40	AC1RX/SS4/U5RX/U2CTS/RF12
6	T2CK/RC1	41	AN12/PMA11/RB12
7	T3CK/RC2	42	AN13/PMA10/RB13
8	T4CK/RC3	43	AN14/PMALH/PMA1/RB14
9	T5CK/SDI1/RC4	44	AN15/OCFB/PMALL/PMA0/CN12/RB15
10	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	45	Vss
11	SDA4/SDI2/U3RX/PMA4/CN9/RG7	46	VDD
12	SCL4/SDO2/U3TX/PMA3/CN10/RG8	47	SS3/U4RX/U1CTS/CN20/RD14
13	MCLR	48	SCK3/U4TX/U1RTS/CN21/RD15
14	SS2/U6RX/U3CTS/PMA2/CN11/RG9	49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
15	Vss	50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
16	VDD	51	USBID/RF3
17	TMS/RA0	52	SDA3/SDI3/U1RX/RF2
18	INT1/RE8	53	SCL3/SDO3/U1TX/RF8
19	INT2/RE9	54	VBUS
20	AN5/C1IN+/VBUSON/CN7/RB5	55	VUSB3V3
21	AN4/C1IN-/CN6/RB4	56	D-/RG3
22	AN3/C2IN+/CN5/RB3	57	D+/RG2
23	AN2/C2IN-/CN4/RB2	58	SCL2/RA2
24	PGEC1/AN1/CN3/RB1	59	SDA2/RA3
25	PGED1/AN0/CN2/RB0	60	TDI/RA4
26	PGEC2/AN6/OCFA/RB6	61	TDO/RA5
27	PGED2/AN7/RB7	62	VDD
28	VREF-/CVREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	Vss
31	AVSS	66	SCL1/INT3/RA14
32	AN8/C1OUT/RB8	67	SDA1/INT4/RA15
33	AN9/C2OUT/RB9	68	RTCC/IC1/RD8
34	AN10/CVREFOUT/PMA13/RB10	69	SS1/IC2/RD9
35	AN11/PMA12/RB11	70	SCK1/IC3/PMCS2/PMA15/RD10

**Note** 1: Shaded pins are 5V tolerant.

**FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX575F256H, PIC32MX575F256L, PIC32MX675F256H, PIC32MX675F256L, PIC32MX775F256H AND PIC32MX775F256L DEVICES**



## REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
	—	—	—	—	—	—	CMR	VREGS
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR <sup>(1)</sup>	POR <sup>(1)</sup>

<b>Legend:</b>	HS = Set by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit  
 1 = Configuration mismatch Reset has occurred  
 0 = Configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit  
 1 = Regulator is enabled and is on during Sleep mode  
 0 = Regulator is set to Stand-by Tracking mode

bit 7 **EXTR:** External Reset ( $\overline{\text{MCLR}}$ ) Pin Flag bit  
 1 = Master Clear (pin) Reset has occurred  
 0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit  
 1 = Software Reset was executed  
 0 = Software Reset was not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit  
 1 = WDT Time-out has occurred  
 0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit  
 1 = Device was in Sleep mode  
 0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit  
 1 = Device was in Idle mode  
 0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit<sup>(1)</sup>  
 1 = Brown-out Reset has occurred  
 0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit<sup>(1)</sup>  
 1 = Power-on Reset has occurred  
 0 = Power-on Reset has not occurred

**Note 1:** User software must clear this bit to view the next detection.

**TABLE 7-3: INTERRUPT REGISTER MAP FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H AND PIC32MX695F512H DEVICES**

Virtual Address (BF88..#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000	
		15:0	—	—	—	MVEC	—	TPC<2:0>				—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT <sup>(3)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	SRIPL<2:0>				—	—	VEC<5:0>					0000	
1020	IPTMR	31:16	IPTMR<31:0>																0000	
		15:0																	0000	
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000	
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000	
		31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	—	—	USBIF	FCEIF	DMA7IF <sup>(2)</sup>	DMA6IF <sup>(2)</sup>	DMA5IF <sup>(2)</sup>	DMA4IF <sup>(2)</sup>	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000	
1040	IFS1	15:0	RTCCIF	FSCMIF	—	—	—	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000	
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000	
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000	
		31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	—	—	USBIE	FCEIE	DMA7IE <sup>(2)</sup>	DMA6IE <sup>(2)</sup>	DMA5IE <sup>(2)</sup>	DMA4IE <sup>(2)</sup>	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000	
1070	IEC1	15:0	RTCCIE	FSCMIE	—	—	—	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000	
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	—	—	INT0IP<2:0>	—	—	—	—	—	—	CS1IP<2:0>			—	CS1IS<1:0>	0000
		15:0	—	—	—	—	—	CS0IP<2:0>	—	—	—	—	—	CTIP<2:0>			—	CTIS<1:0>	0000	
10A0	IPC1	31:16	—	—	—	—	—	INT1IP<2:0>	—	—	—	—	—	OC1IP<2:0>			—	OC1IS<1:0>	0000	
		15:0	—	—	—	—	—	IC1IP<2:0>	—	—	—	—	—	T1IP<2:0>			—	T1IS<1:0>	0000	
10B0	IPC2	31:16	—	—	—	—	—	INT2IP<2:0>	—	—	—	—	—	OC2IP<2:0>			—	OC2IS<1:0>	0000	
		15:0	—	—	—	—	—	IC2IP<2:0>	—	—	—	—	—	T2IP<2:0>			—	T2IS<1:0>	0000	
10C0	IPC3	31:16	—	—	—	—	—	INT3IP<2:0>	—	—	—	—	—	OC3IP<2:0>			—	OC3IS<1:0>	0000	
		15:0	—	—	—	—	—	IC3IP<2:0>	—	—	—	—	—	T3IP<2:0>			—	T3IS<1:0>	0000	

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2: These bits are not available on PIC32MX664 devices.
- 3: This register does not have associated CLR, SET, and INV registers.

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**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)**

- bit 2     **UFRGEN:** USB FRC Clock Enable bit  
          1 = Enable FRC as the clock source for the USB clock source  
          0 = Use the Primary Oscillator or USB PLL as the USB clock source
- bit 1     **SOSCEN:** Secondary Oscillator (SOSC) Enable bit  
          1 = Enable Secondary Oscillator  
          0 = Disable Secondary Oscillator
- bit 0     **OSWEN:** Oscillator Switch Enable bit  
          1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits  
          0 = Oscillator switch is complete

<b>Note:</b>	Writes to this register require an unlock sequence. Refer to <b>Section 6. “Oscillator”</b> (DS60001112) in the <i>“PIC32 Family Reference Manual”</i> for details.
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# PIC32MX5XX/6XX/7XX

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## REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

- bit 6      **CRCAPP:** CRC Append Mode bit<sup>(1)</sup>  
1 = The DMA transfers data from the source into the CRC but not to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA  
0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5      **CRCTYP:** CRC Type Selection bit  
1 = The CRC module will calculate an IP header checksum  
0 = The CRC module will calculate a LFSR CRC
- bit 4-3    **Unimplemented:** Read as '0'
- bit 2-0    **CRCCH<2:0>:** CRC Channel Select bits  
111 = CRC is assigned to Channel 7  
110 = CRC is assigned to Channel 6  
101 = CRC is assigned to Channel 5  
100 = CRC is assigned to Channel 4  
011 = CRC is assigned to Channel 3  
010 = CRC is assigned to Channel 2  
001 = CRC is assigned to Channel 1  
000 = CRC is assigned to Channel 0

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.



## 17.0 OUTPUT COMPARE

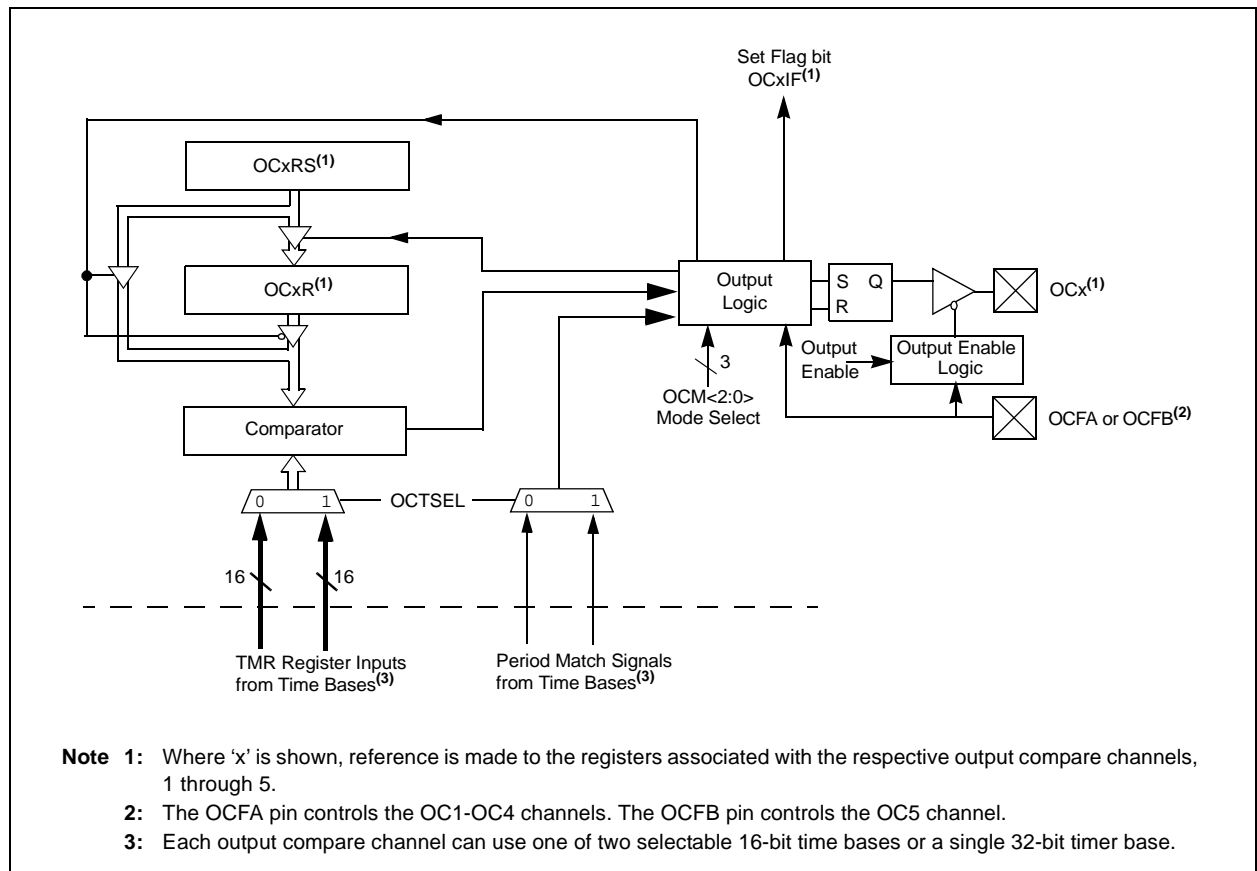
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. “Output Compare”** (DS60001111) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

The Output Compare module is used to generate a single pulse or a series of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

**FIGURE 17-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM**



## 18.1 Control Registers

**TABLE 18-1: SPI1 THROUGH SPI4 REGISTER MAP**

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
5E00	SPI1CON <sup>(2)</sup>	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5E10	SPI1STAT <sup>(2)</sup>	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5E20	SPI1BUF <sup>(2)</sup>	31:16	DATA<31:0>															0000	
		15:0	DATA<31:0>															0000	
5E30	SPI1BRG <sup>(2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5800	SPI3CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5810	SPI3STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5820	SPI3BUF	31:16	DATA<31:0>															0000	
		15:0	DATA<31:0>															0000	
5830	SPI3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5A10	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5A20	SPI2BUF	31:16	DATA<31:0>															0000	
		15:0	DATA<31:0>															0000	
5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5C00	SPI4CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5C10	SPI4STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5C20	SPI4BUF	31:16	DATA<31:0>															0000	
		15:0	DATA<31:0>															0000	
5C30	SPI4BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register is not available on 64-pin devices.

## REGISTER 18-2: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	R-0	R-0	R-0	R-0	R-0
	RXBUFELM<4:0>							
23:16	U-0 —	U-0 —	U-0 —	R-0	R-0	R-0	R-0	R-0
	TXBUFELM<4:0>							
15:8	U-0 —	U-0 —	U-0 —	U-0 —	R-0 SPIBUSY	U-0 —	U-0 —	R-0 SPITUR
7:0	R-0 SRMT	R/W-0 SPIOV	R-0 SPIRBE	U-0 —	R-1 SPITBE	U-0 —	R-0 SPITBF	R-0 SPIRBF

<b>Legend:</b>	C = Clearable bit	HS = Set in hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (only valid when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (only valid when ENHBUF = 1)

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **SPIBUSY:** SPI Activity Status bit

1 = SPI peripheral is currently busy with some transactions

0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit

1 = Transmit buffer has encountered an underrun condition

0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (only valid when ENHBUF = 1)

1 = When SPI module shift register is empty

0 = When SPI module shift register is not empty

bit 6 **SPIOV:** Receive Overflow Flag bit

1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.

0 = No overflow has occurred

This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE:** RX FIFO Empty bit (only valid when ENHBUF = 1)

1 = RX FIFO is empty (CRPTR = SWPTR)

0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit

1 = Transmit buffer, SPIxTXB is empty

0 = Transmit buffer, SPIxTXB is not empty

Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.

Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

# PIC32MX5XX/6XX/7XX

**REGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ADRC	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
ADCS<7:0> <sup>(2)</sup>								

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit

1 = Clock derived from FRC

0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits<sup>(1)</sup>

11111 = 31 TAD

•  
•  
•

00001 = 1 TAD

00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits<sup>(2)</sup>

11111111 =  $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 512 \cdot TPB = TAD$

•  
•  
•

00000001 =  $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 4 \cdot TPB = TAD$

00000000 =  $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 2 \cdot TPB = TAD$

**Note 1:** This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.

**2:** This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

## REGISTER 24-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>**: Propagation Time Segment bits<sup>(4)</sup>

111 = Length is 8 x T<sub>Q</sub>

•  
•  
•

000 = Length is 1 x T<sub>Q</sub>

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits<sup>(3)</sup>

11 = Length is 4 x T<sub>Q</sub>

10 = Length is 3 x T<sub>Q</sub>

01 = Length is 2 x T<sub>Q</sub>

00 = Length is 1 x T<sub>Q</sub>

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

111111 = T<sub>Q</sub> = (2 x 64)/F<sub>SYS</sub>

111110 = T<sub>Q</sub> = (2 x 63)/F<sub>SYS</sub>

•  
•  
•

000001 = T<sub>Q</sub> = (2 x 2)/F<sub>SYS</sub>

000000 = T<sub>Q</sub> = (2 x 1)/F<sub>SYS</sub>

**Note 1:** SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

**2:** 3 Time bit sampling is not allowed for BRP < 2.

**3:** SJW ≤ SEG2PH.

**4:** The Time Quanta per bit must be greater than 7 (that is, T<sub>QBIT</sub> > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

# PIC32MX5XX/6XX/7XX

## REGISTER 24-3: CiINT: CAN INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIF	WAKIF	CERRIF	SERRIF <sup>(1)</sup>	RBOVIF	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 31      **IVRIE:** Invalid Message Received Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 30      **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 29      **CERRIE:** CAN Bus Error Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 28      **SERRIE:** System Error Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 27      **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 26-20      **Unimplemented:** Read as '0'
- bit 19      **MODIE:** Mode Change Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 18      **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 17      **RBIE:** Receive Buffer Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 16      **TBIE:** Transmit Buffer Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 15      **IVRIF:** Invalid Message Received Interrupt Flag bit  
             1 = An invalid messages interrupt has occurred  
             0 = An invalid message interrupt has not occurred

**Note 1:** This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CiCON<15>).

## REGISTER 24-10: C<sub>i</sub>FLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 15	<b>FLTEN1:</b> Filter 1 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 14-13	<b>MSEL1&lt;1:0&gt;:</b> Filter 1 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 12-8	<b>FSEL1&lt;4:0&gt;:</b> FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 • • • 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0
bit 7	<b>FLTEN0:</b> Filter 0 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 6-5	<b>MSEL0&lt;1:0&gt;:</b> Filter 0 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 4-0	<b>FSEL0&lt;4:0&gt;:</b> FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 • • • 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0

<b>Note:</b> The bits in this register can only be modified if the corresponding filter enable (FLTEN <sub>n</sub> ) bit is '0'.
--

# PIC32MX5XX/6XX/7XX

## REGISTER 25-39: EMAC1SA2: ETHERNET CONTROLLER MAC STATION ADDRESS 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR2<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR1<7:0>							

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

P = Programmable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared      x = Bit is unknown

bit 31-16 **Reserved:** Maintain as '0'; ignore read

bit 15-8 **STNADDR2<7:0>:** Station Address Octet 2 bits  
These bits hold the second transmitted octet of the station address.

bit 7-0 **STNADDR1<7:0>:** Station Address Octet 1 bits  
These bits hold the most significant (first transmitted) octet of the station address.

- Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.
- 2:** This register is loaded at reset from the factory preprogrammed station address.

## 26.0 COMPARATOR

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS60001110) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

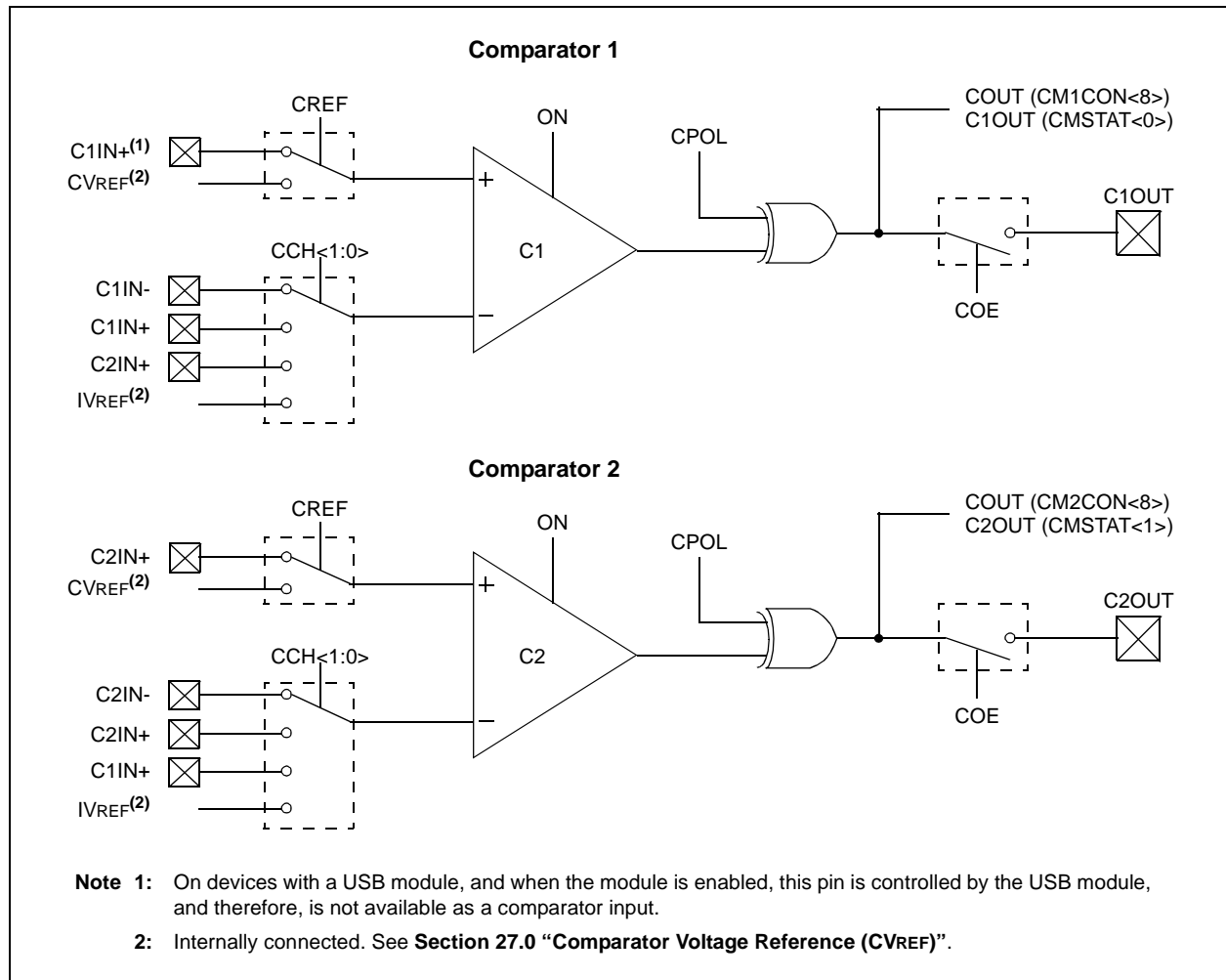
The Comparator module contains two comparators that can be configured in a variety of ways.

Key features of the Comparator module include:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the Comparator module is illustrated in Figure 26-1.

**FIGURE 26-1: COMPARATOR MODULE BLOCK DIAGRAM**



# PIC32MX5XX/6XX/7XX

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## REGISTER 29-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

- bit 13-12 **FPBDIV<1:0>**: Peripheral Bus Clock Divisor Default Value bits  
11 = PBCLK is SYSCLK divided by 8  
10 = PBCLK is SYSCLK divided by 4  
01 = PBCLK is SYSCLK divided by 2  
00 = PBCLK is SYSCLK divided by 1
- bit 11 **Reserved**: Write '1'
- bit 10 **OSCIOFNC**: CLKO Enable Configuration bit  
1 = CLKO output is disabled  
0 = CLKO output signal is active on the OSCO pin; the Primary Oscillator must be disabled or configured for External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)
- bit 9-8 **POSCMOD<1:0>**: Primary Oscillator Configuration bits  
11 = Primary Oscillator is disabled  
10 = HS Oscillator mode is selected  
01 = XT Oscillator mode is selected  
00 = External Clock mode is selected
- bit 7 **IESO**: Internal External Switchover bit  
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)  
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)
- bit 6 **Reserved**: Write '1'
- bit 5 **FSOSCEN**: Secondary Oscillator Enable bit  
1 = Enable the Secondary Oscillator  
0 = Disable the Secondary Oscillator
- bit 4-3 **Reserved**: Write '1'
- bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits  
111 = Fast RC Oscillator with divide-by-N (FRCDIV)  
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler  
101 = Low-Power RC Oscillator (LPRC)  
100 = Secondary Oscillator (Sosc)  
011 = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL)  
010 = Primary Oscillator (XT, HS, EC)<sup>(1)</sup>  
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)  
000 = Fast RC Oscillator (FRC)

**Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

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**REGISTER 29-5: DEVID: DEVICE AND REVISION ID REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0> <sup>(1)</sup>				DEVID<27:24> <sup>(1)</sup>			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16> <sup>(1)</sup>							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8> <sup>(1)</sup>							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0> <sup>(1)</sup>							

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-28 **VER<3:0>**: Revision Identifier bits<sup>(1)</sup>

bit 27-0 **DEVID<27:0>**: Device ID bits<sup>(1)</sup>

**Note 1:** See the “PIC32 Flash Programming Specification” (DS60001145) for a list of Revision and Device ID values.

**REGISTER 29-6: DDPCON: DEBUG DATA PORT CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	U-0	R/W-0
	—	—	—	—	JTAGEN	TROEN	—	TDOEN

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Port Enable bit

1 = Enable the JTAG port  
0 = Disable the JTAG port

bit 2 **TROEN:** Trace Output Enable bit

1 = Enable the trace port  
0 = Disable the trace port

bit 1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG

1 = 2-wire JTAG protocol uses TDO  
0 = 2-wire JTAG protocol does not use TDO

# PIC32MX5XX/6XX/7XX

**TABLE 32-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode <sup>(1)</sup>	0.5	—	μs	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode <sup>(1)</sup>	0.5	—	μs	—
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode <sup>(1)</sup>	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode <sup>(1)</sup>	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode <sup>(1)</sup>	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode <sup>(1)</sup>	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode <sup>(1)</sup>	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode <sup>(1)</sup>	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode <sup>(1)</sup>	600	—	ns	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode <sup>(1)</sup>	250	—	ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode <sup>(1)</sup>	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode <sup>(1)</sup>	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	400	pF	—

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (only for 1 MHz mode).

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