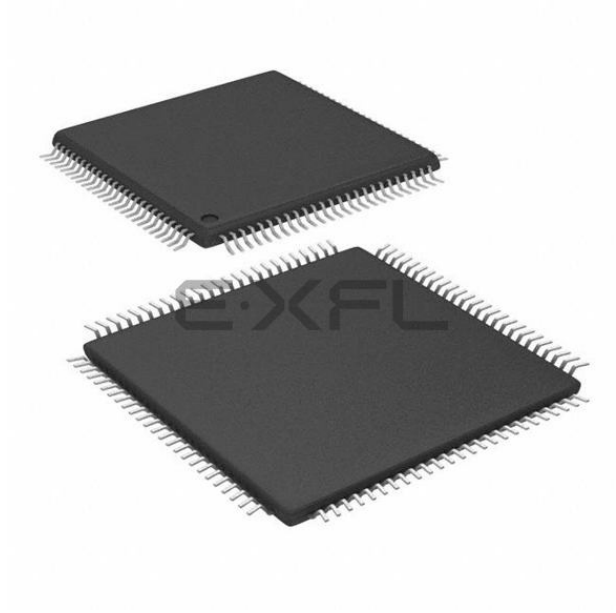
Microchip Technology - PIC32MX534F064LT-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx534f064lt-i-pt

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES

121-PIN TFBGA (BOTTOM VIEW)

L11

PIC32MX664F064L
PIC32MX664F128L
PIC32MX675F256L
PIC32MX675F512L
PIC32MX695F512L

L1

A11

Note: The TFBGA package skips from row "H" to row "J" and has no "I" row.

A1

Pin #	Full Pin Name	Pin #	Full Pin Name
A1	PMD4/RE4	E2	T4CK/RC3
A2	PMD3/RE3	E3	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6
A3	TRD0/RG13	E4	T3CK/RC2
A4	PMD0/RE0	E5	VDD
A5	PMD8/RG0	E6	ETXERR/PMD9/RG1
A6	ETXD0/PMD10/RF1	E7	VSS
A7	VDD	E8	AETXEN/SDA1/INT4/RA15
A8	VSS	E9	RTCC/EMDIO/AEMDIO/IC1/RD8
A9	ETXD2/IC5/PMD12/RD12	E10	SS1/IC2/RD9
A10	OC3/RD2	E11	AETXCLK/SCL1/INT3/RA14
A11	OC2/RD1	F1	MCLR
B1	No Connect (NC)	F2	ERXDV/AERXDV/ECRSDV/AECRSDV//SCL4/SDO2/U3TX/PMA3/CN10/RG8
B2	AERXERR/RG15	F3	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9
B3	PMD2/RE2	F4	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7
B4	PMD1/RE1	F5	VSS
B5	TRD3/RA7	F6	No Connect (NC)
B6	ETXD1/PMD11/RF0	F7	No Connect (NC)
B7	VCAP	F8	VDD
B8	PMRD/CN14/RD5	F9	OSC1/CLKI/RC12
B9	OC4/RD3	F10	VSS
B10	VSS	F11	OSC2/CLKO/RC15
B11	SOSCO/T1CK/CN0/RC14	G1	AERXD0/INT1/RE8
C1	PMD6/RE6	G2	AERXD1/INT2/RE9
C2	VDD	G3	TMS/RA0
C3	TRD1/RG12	G4	No Connect (NC)
C4	TRD2/RG14	G5	VDD
C5	TRCLK/RA6	G6	VSS
C6	No Connect (NC)	G7	VSS
C7	ETXCLK/PMD15/CN16/RD7	G8	No Connect (NC)
C8	OC5/PMWR/CN13/RD4	G9	TDO/RA5
C9	VDD	G10	SDA2/RA3
C10	SOSCI/CN1/RC13	G11	TDI/RA4
C11	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	H1	AN5/C1IN+/VBUSON/CN7/RB5
D1	T2CK/RC1	H2	AN4/C1IN-/CN6/RB4
D2	PMD7/RE7	H3	VSS
D3	PMD5/RE5	H4	VDD
D4	VSS	H5	No Connect (NC)
D5	VSS	H6	VDD
D6	No Connect (NC)	H7	No Connect (NC)
D7	ETXEN/PMD14/CN15/RD6	H8	VBUS
D8	ETXD3/PMD13/CN19/RD13	H9	VUSB3V3
D9	SDO1/OC1/INT0/RD0	H10	D+/RG2
D10	No Connect (NC)	H11	SCL2/RA2
D11	SCK1/IC3/PMCS2/PMA15/RD10	J1	AN3/C2IN+/CN5/RB3
E1	T5CK/SDI1/RC4	J2	AN2/C2IN-/CN4/RB2

Note 1: Shaded pins are 5V tolerant.

TABLE 12: PIN NAMES FOR USB, ETHERNET, AND CAN DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)

L11

L1

A11

PIC32MX764F128L
PIC32MX775F256L
PIC32MX775F512L
PIC32MX795F512L

Note: The TFBGA package skips from row "H" to row "J" and has no "I" row.

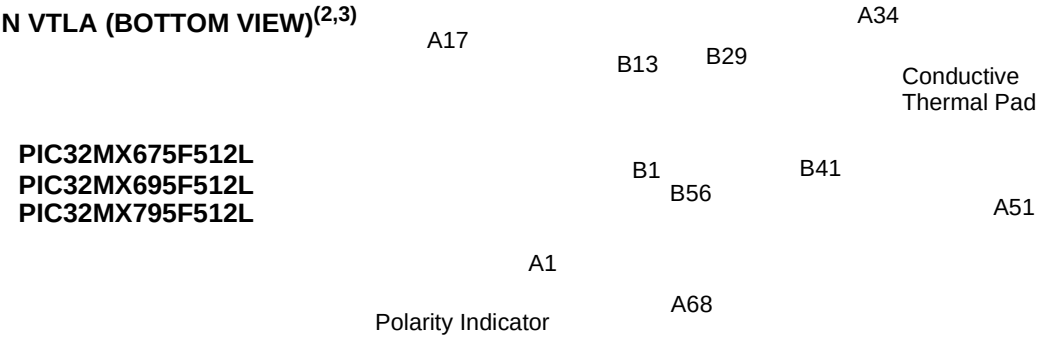
A1

Pin #	Full Pin Name
J3	PGED2/AN7/RB7
J4	AVDD
J5	AN11/ERXERR/AETXERR/PMA12/RB11
J6	TCK/RA1
J7	AN12/ERXD0/AECRS/PMA11/RB12
J8	No Connect (NC)
J9	No Connect (NC)
J10	SCL3/SDO3/U1TX/RF8
J11	D-/RG3
K1	PGEC1/AN1/CN3/RB1
K2	PGED1/AN0/CN2/RB0
K3	VREF+/CVREF+/AERXD3/PMA6/RA10
K4	AN8/C1OUT/RB8
K5	No Connect (NC)
K6	AC1RX/SS4/U5RX/U2CTS/RF12
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14
K8	VDD
K9	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
K10	USBID/RF3
K11	SDA3/SDI3/U1RX/RF2
L1	PGEC2/AN6/OCFA/RB6
L2	VREF-/CVREF-/AERXD2/PMA7/RA9
L3	AVSS
L4	AN9/C2OUT/RB9
L5	AN10/CVREFOUT/PMA13/RB10
L6	AC1TX/SCK4/U5TX/U2RTS/RF13
L7	AN13/ERXD1/AECOL/PMA10/RB13
L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
L9	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5

Note 1: This pin is not available on PIC32MX764F128L devices.
2: Shaded pins are 5V tolerant.

TABLE 13: PIN NAMES FOR 124-PIN USB, ETHERNET, AND CAN DEVICES

124-PIN VTLA (BOTTOM VIEW)(2,3)



Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
A1	No Connect (NC)	A38	D-/RG3
A2	AERXERR/RG15	A39	SCL2/RA2
A3	VSS	A40	TDI/RA4
A4	PMD6/RE6	A41	VDD
A5	T2CK/RC1	A42	OSC2/CLKO/RC15
A6	T4CK/AC2RX(1)/RC3	A43	VSS
A7	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6	A44	AETXEN/SDA1/INT4/RA15
A8	ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8	A45	SS1/IC2/RD9
A9	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9	A46	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11
A10	VDD	A47	SOSCI/CN1/RC13
A11	AERXD0/INT1/RE8	A48	VDD
A12	AN5/C1IN+/VBUSON/CN7/RB5	A49	No Connect (NC)
A13	AN3/C2IN+/CN5/RB3	A50	No Connect (NC)
A14	VDD	A51	No Connect (NC)
A15	PGEC1/AN1/CN3/RB1	A52	OC2/RD1
A16	No Connect (NC)	A53	OC4/RD3
A17	No Connect (NC)	A54	ETXD3/PMD13/CN19/RD13
A18	No Connect (NC)	A55	PMRD/CN14/RD5
A19	No Connect (NC)	A56	ETXCLK/PMD15/CN16/RD7
A20	PGEC2/AN6/OCFA/RB6	A57	No Connect (NC)
A21	VREF-/CVREF-/AERXD2/PMA7/RA9	A58	No Connect (NC)
A22	AVDD	A59	VDD
A23	AN8/C1OUT/RB8	A60	C1TX/ETXD0/PMD10/RF1
A24	AN10/CVREFOUT/PMA13/RB10	A61	C2RX(1)/PMD8/RG0
A25	VSS	A62	TRD3/RA7
A26	TCK/RA1	A63	VSS
A27	AC1RX(1)/SS4/U5RX/U2CTS/RF12	A64	PMD1/RE1
A28	AN13/ERXD1/AECOL/PMA10/RB13	A65	TRD1/RG12
A29	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15	A66	PMD2/RE2
A30	VDD	A67	PMD4/RE4
A31	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15	A68	No Connect (NC)
A32	SCL5/SDO4/U2TX/PMA8/CN18/RF5	B1	VDD
A33	No Connect (NC)	B2	PMD5/RE5
A34	No Connect (NC)	B3	PMD7/RE7
A35	USBID/RF3	B4	T3CK/AC2TX(1)/RC2
A36	SDA3/SDI3/U1RX/RF2	B5	T5CK/SDI1/RC4
A37	VBUS	B6	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7
B7	MCLR	B32	SDA2/RA3

Note 1: This pin is only available on PIC32MX795F512L devices.
2: Shaded package bumps are 5V tolerant.
3: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
RA0	—	17	G3	B9	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	J6	A26	I/O	ST	
RA2	—	58	H11	A39	I/O	ST	
RA3	—	59	G10	B32	I/O	ST	
RA4	—	60	G11	A40	I/O	ST	
RA5	—	61	G9	B33	I/O	ST	
RA6	—	91	C5	B51	I/O	ST	
RA7	—	92	B5	A62	I/O	ST	
RA9	—	28	L2	A21	I/O	ST	
RA10	—	29	K3	B17	I/O	ST	
RA14	—	66	E11	B36	I/O	ST	
RA15	—	67	E8	A44	I/O	ST	
RB0	16	25	K2	B14	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	K1	A15	I/O	ST	
RB2	14	23	J2	B13	I/O	ST	
RB3	13	22	J1	A13	I/O	ST	
RB4	12	21	H2	B11	I/O	ST	
RB5	11	20	H1	A12	I/O	ST	
RB6	17	26	L1	A20	I/O	ST	
RB7	18	27	J3	B16	I/O	ST	
RB8	21	32	K4	A23	I/O	ST	
RB9	22	33	L4	B19	I/O	ST	
RB10	23	34	L5	A24	I/O	ST	
RB11	24	35	J5	B20	I/O	ST	
RB12	27	41	J7	B23	I/O	ST	
RB13	28	42	L7	A28	I/O	ST	
RB14	29	43	K7	B24	I/O	ST	
RB15	30	44	L8	A29	I/O	ST	
RC1	—	6	D1	A5	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	E4	B4	I/O	ST	
RC3	—	8	E2	A6	I/O	ST	
RC4	—	9	E1	B5	I/O	ST	
RC12	39	63	F9	B34	I/O	ST	
RC13	47	73	C10	A47	I/O	ST	
RC14	48	74	B11	B40	I/O	ST	
RC15	40	64	F11	A42	I/O	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

2: See **25.0 "Ethernet Controller"** for more information.

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
	—	—	—	—	—	—	CMR	VREGS
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR(1)	POR(1)

Legend:	HS = Set by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = Configuration mismatch Reset has occurred
0 = Configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
1 = Regulator is enabled and is on during Sleep mode
0 = Regulator is set to Stand-by Tracking mode

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view the next detection.

11.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded Host, full-speed Device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The USB module includes the following features:

- USB Full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

REGISTER 11-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 11-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized

When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit

1 = External clock from TxCKI pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

14.0 TIMER2/3, TIMER4/5

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-bit Timer
- Synchronous Internal 16-bit Gated Timer
- Synchronous External 16-bit Timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

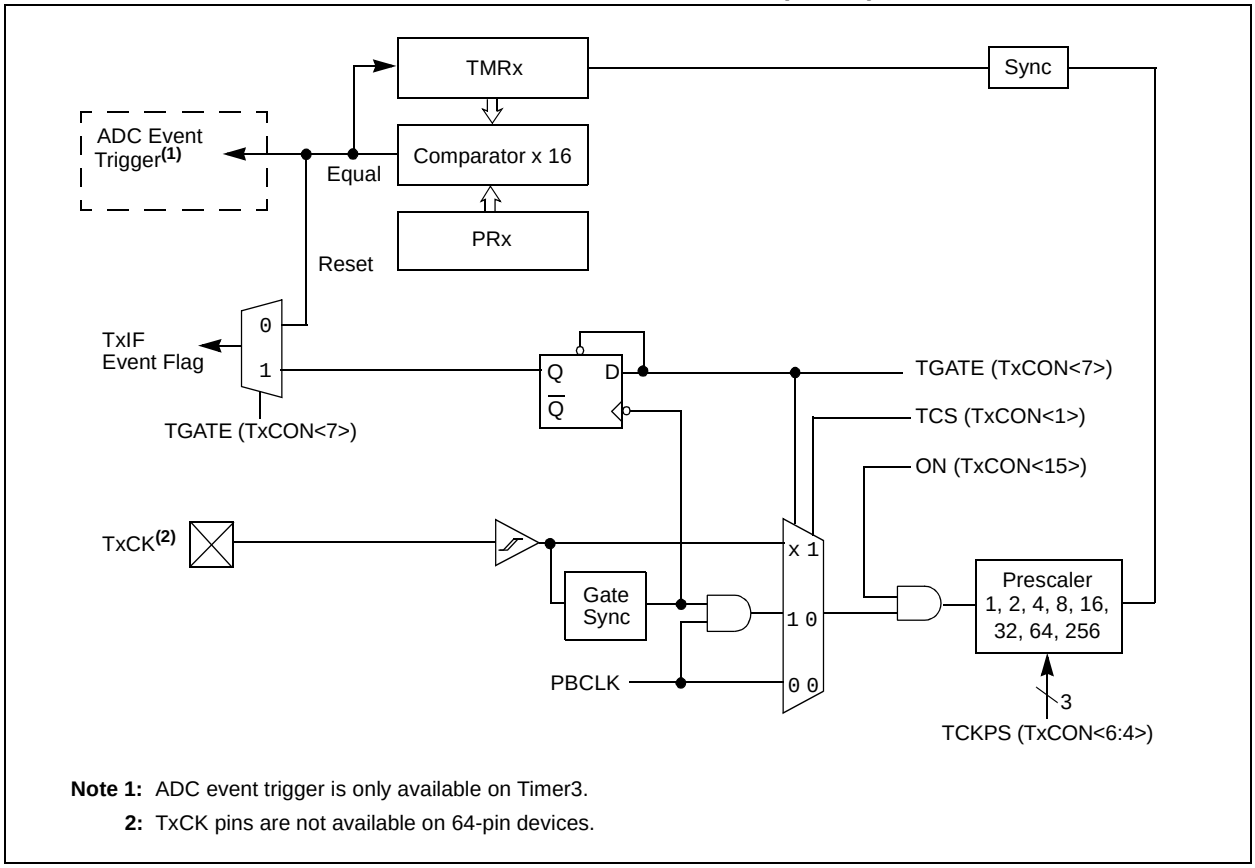
- Synchronous Internal 32-bit Timer
- Synchronous Internal 32-bit Gated Timer
- Synchronous External 32-bit Timer

Note: In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through Timer5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or Timer4; 'y' represents Timer3 or Timer5.

14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (only Timer2 and Timer3)
- ADC event trigger (only Timer3)
- Fast bit manipulation using CLR, SET and INV registers

FIGURE 14-1: TIMER2/3 AND TIMER4/5 BLOCK DIAGRAM (16-BIT)



Note 1: ADC event trigger is only available on Timer3.

2: TxCK pins are not available on 64-pin devices.

FIGURE 19-1: I²C BLOCK DIAGRAM

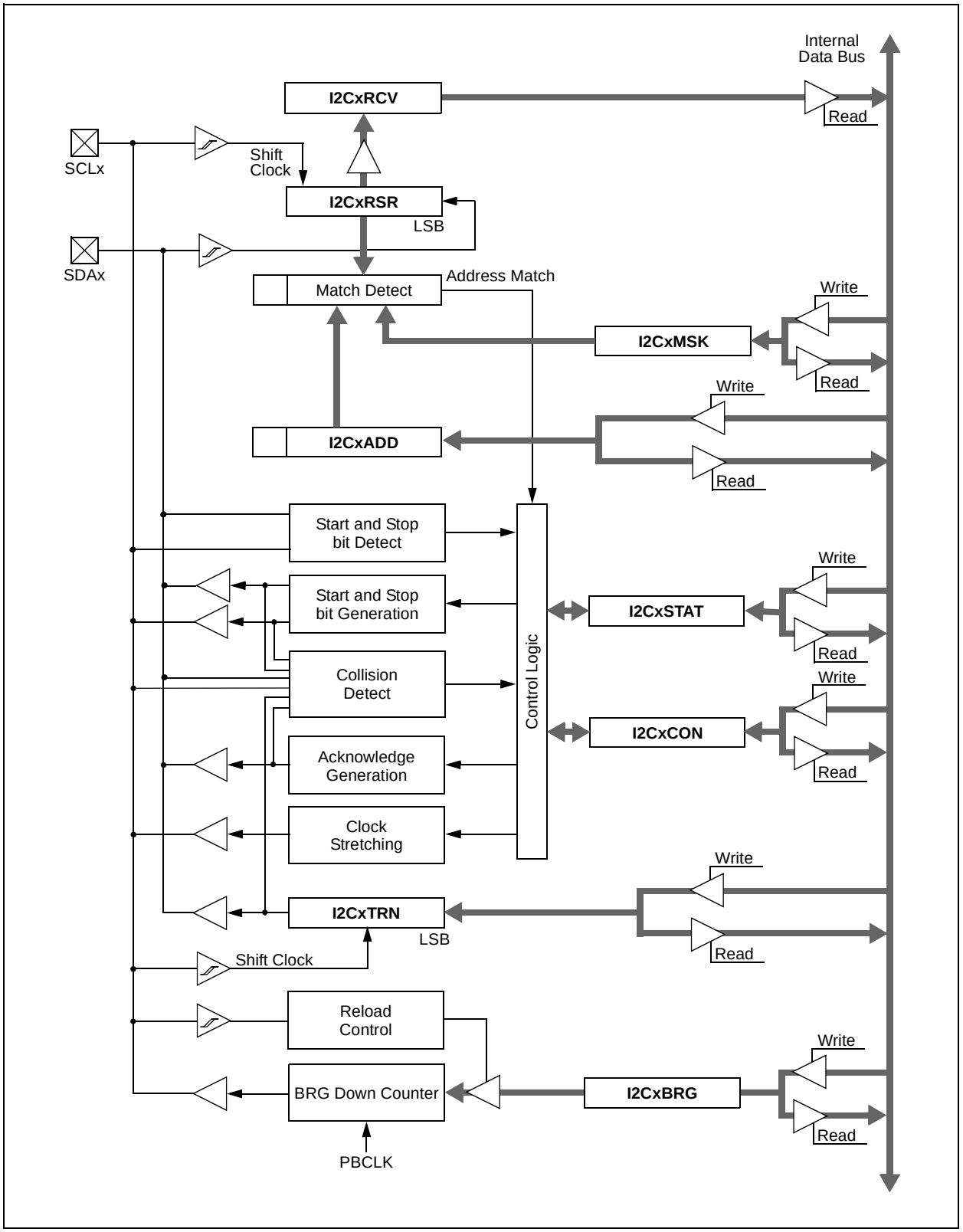
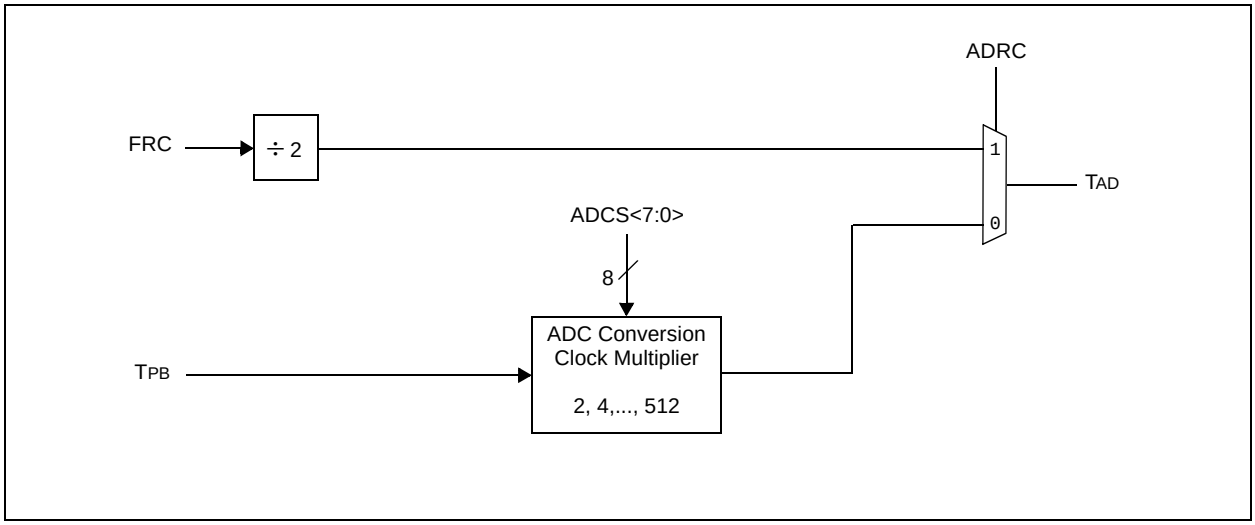


FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



REGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	—	—	SAMC<4:0>(1)				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
	ADCS<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = Clock derived from FRC
0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits(2)
11111111 = TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD
•
•
•
00000001 = TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD
00000000 = TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
2: This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

TABLE 32-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	2.3	—	3.6	V	—
DC12	VDR	**RAM Data Retention Voltage(1)**	1.75	—	—	V	—
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	1.75	—	2.1	V	—
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.00005	—	0.115	V/μs	—

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 32-10 for BOR values.

32.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX5XX/6XX/7XX AC characteristics and timing parameters.

FIGURE 32-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

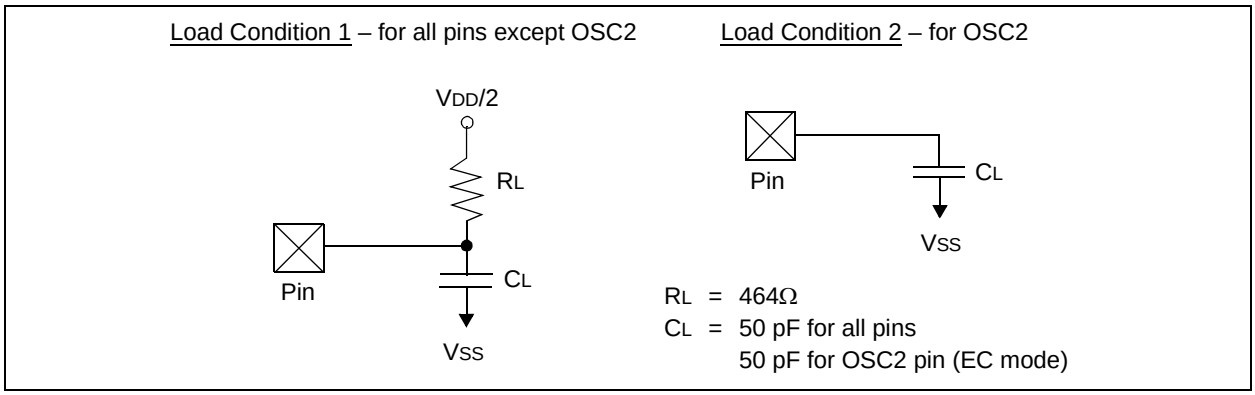


TABLE 32-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO50	Cosco	OSC2 pin	—	—	15	pF	In XT and HS modes when an external crystal is used to drive OSC1
DO56	CIO	All I/O pins and OSC2	—	—	50	pF	In EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 32-2: EXTERNAL CLOCK TIMING

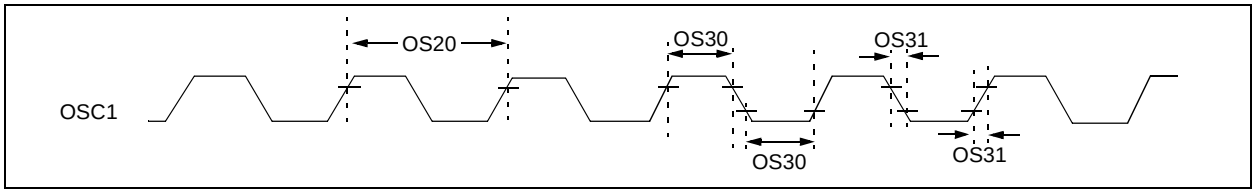


FIGURE 32-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

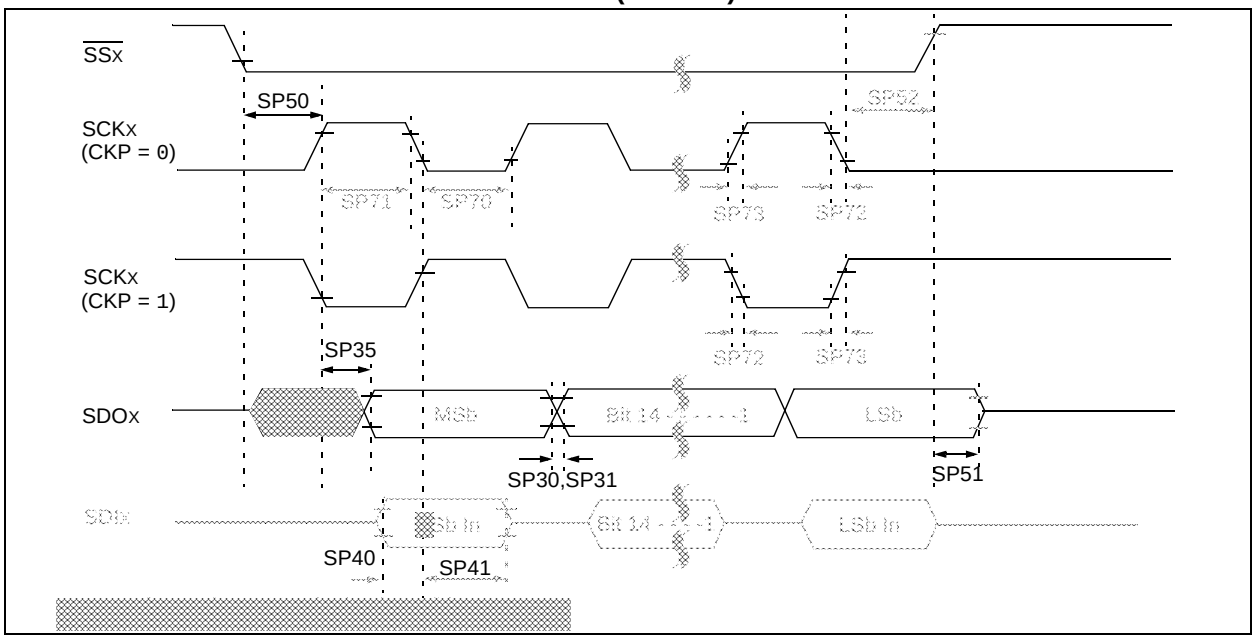


TABLE 32-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	175	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(3)	5	—	25	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	Tsck + 20	—	—	ns	—

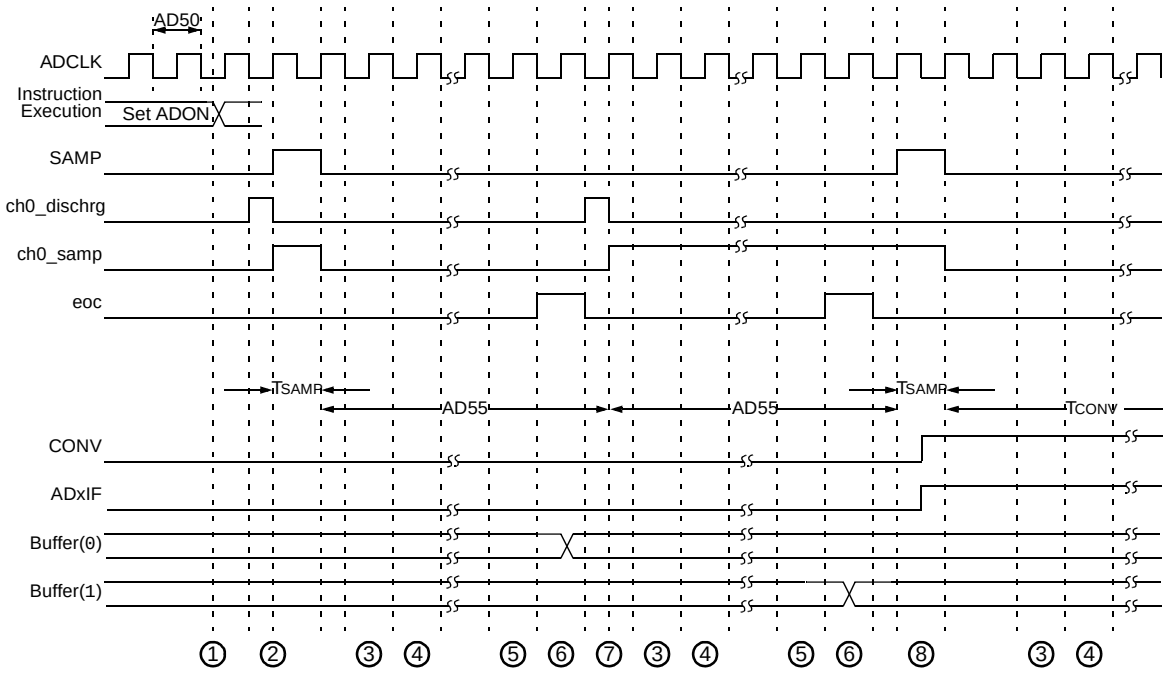
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 32-24: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)



(1) – Software sets ADxCON. ADON to start AD operation.

(2) – Sampling starts after discharge period.
TSAMP is described in Section 17. “10-bit A/D Converter” (DS60001104) of the *“PIC32 Family Reference Manual*.

(3) – Convert bit 9.

(4) – Convert bit 8.

(5) – Convert bit 0.

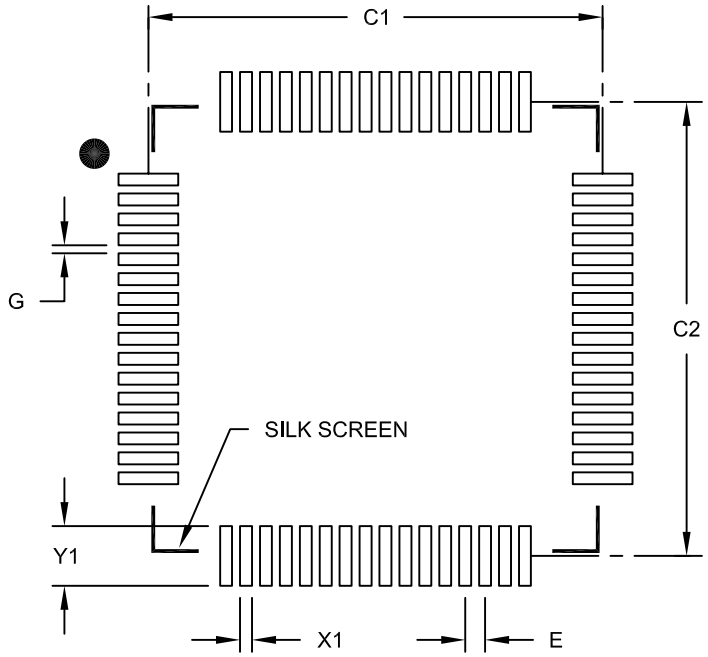
(6) – One TAD for end of conversion.

(7) – Begin conversion of next channel.

(8) – Sample for time specified by SAMC<4:0>.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

APPENDIX B: REVISION HISTORY

Revision A (August 2009)

This is the initial released version of this document.

Revision B (November 2009)

The revision includes the following global update:

Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits.

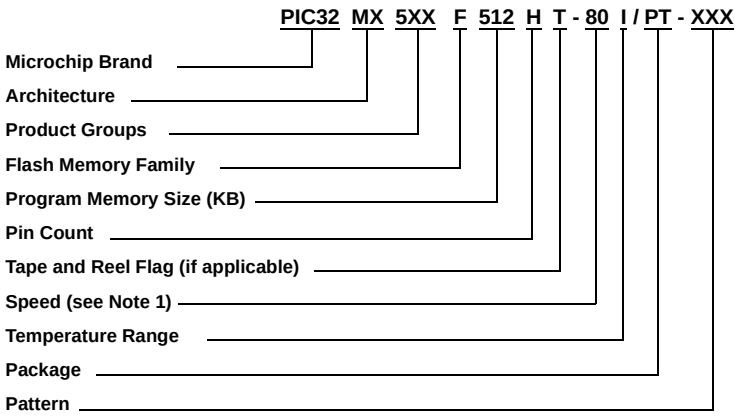
Other major changes are referenced by their respective chapter/section in Table B-1.

TABLE B-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"	Added the following devices: - PIC32MX575F256L - PIC32MX695F512L - PIC32MX695F512H The 100-pin TQFP pin diagrams have been updated to reflect the current pin name locations (see the **"Pin Diagrams"** section). Added the 121-pin Ball Grid Array (XBGA) pin diagram. Updated Table 1: "PIC32 USB and CAN – Features" Added the following tables: - Table 4: "Pin Names: PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L and PIC32MX575F512L Devices" - Table 5: "Pin Names: PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L and PIC32MX695F512L Devices" - Table 6: "Pin Names: PIC32MX775F256L, PIC32MX775F512L and PIC32MX795F512L Devices" Updated the following pins as 5V tolerant: - 64-pin QFN: Pin 36 (D-/RG3) and Pin 37 (D+/RG2) - 64-pin TQFP: Pin 36 (D-/RG3) and Pin 37 (D+/RG2) - 100-pin TQFP: Pin 56 (D-/RG3) and Pin 57 (D+/RG2)
1.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	Removed the last sentence of **1.3.1 "Internal Regulator Mode"**. Removed Section 2.3.2 "External Regulator Mode"

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Example:

PIC32MX575F256H-80I/PT:
General purpose PIC32,
32-bit RISC MCU,
256 KB program memory,
64-pin, Industrial temperature,
TQFP package.

Flash Memory Family

Architecture	MX = 32-bit RISC MCU core
Product Groups	5XX = General purpose microcontroller family 6XX = General purpose microcontroller family 7XX = General purpose microcontroller family
Flash Memory Family	F = Flash program memory
Program Memory Size	**64 = 64K** **128 = 128K** 256 = 256K 512 = 512K
Pin Count	H = 64-pin L = 100-pin, 121-pin, 124-pin
Speed (see **Note 1**)	Blank or 80 = 80 MHz
Temperature Range	I = -40°C to +85°C (Industrial) V = -40°C to +105°C (V-Temp)
Package	PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) PF = 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack) MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat) BG = 121-Lead (10x10x1.1 mm) TFBGA (Plastic Thin Profile Ball Grid Array) TL = 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample

Note 1: This option is not available for PIC32MX534/564/664/764 devices.