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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx534f064lt-v-pf

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)		L11
PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L	L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1

Pin #	Full Pin Name	Pin #	Full Pin Name
J3	PGED2/AN7/RB7	K8	VDD
J4	AVDD	K9	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
J5	AN11/ERXERR/AETXERR/PMA12/RB11	K10	USBID/RF3
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2
J7	AN12/ERXD0/AECRS/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6
J8	No Connect (NC)	L2	VREF-/CVREF-/AERXD2/PMA7/RA9
J9	No Connect (NC)	L3	AVss
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10
K1	PGEC1/AN1/CN3/RB1	L6	SCK4/U5TX/U2RTS/RF13
K2	PGED1/AN0/CN2/RB0	L7	AN13/ERXD1/AECOL/PMA10/RB13
K3	VREF+/CVREF+/AERXD3/PMA6/RA10	L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
K4	AN8/C1OUT/RB8	L9	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
K6	SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14		

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 12: PIN NAMES FOR USB, ETHERNET, AND CAN DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX764F128L PIC32MX775F256L PIC32MX775F512L PIC32MX795F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1	
Pin #	Full Pin Name	Pin #	Full Pin Name
J3	PGED2/AN7/RB7	K8	VDD
J4	AVDD	K9	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
J5	AN11/ERXERR/AETXERR/PMA12/RB11	K10	USBID/RF3
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2
J7	AN12/ERXD0/AECRS/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6
J8	No Connect (NC)	L2	VREF-/CVREF-/AERXD2/PMA7/RA9
J9	No Connect (NC)	L3	AVSS
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10
K1	PGEC1/AN1/CN3/RB1	L6	AC1TX/SCK4/U5TX/U2RTS/RF13
K2	PGED1/AN0/CN2/RB0	L7	AN13/ERXD1/AECOL/PMA10/RB13
K3	VREF+/CVREF+/AERXD3/PMA6/RA10	L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
K4	AN8/C1OUT/RB8	L9	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
K6	AC1RX/SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14		

- Note** 1: This pin is not available on PIC32MX764F128L devices.
 2: Shaded pins are 5V tolerant.

1.0 DEVICE OVERVIEW

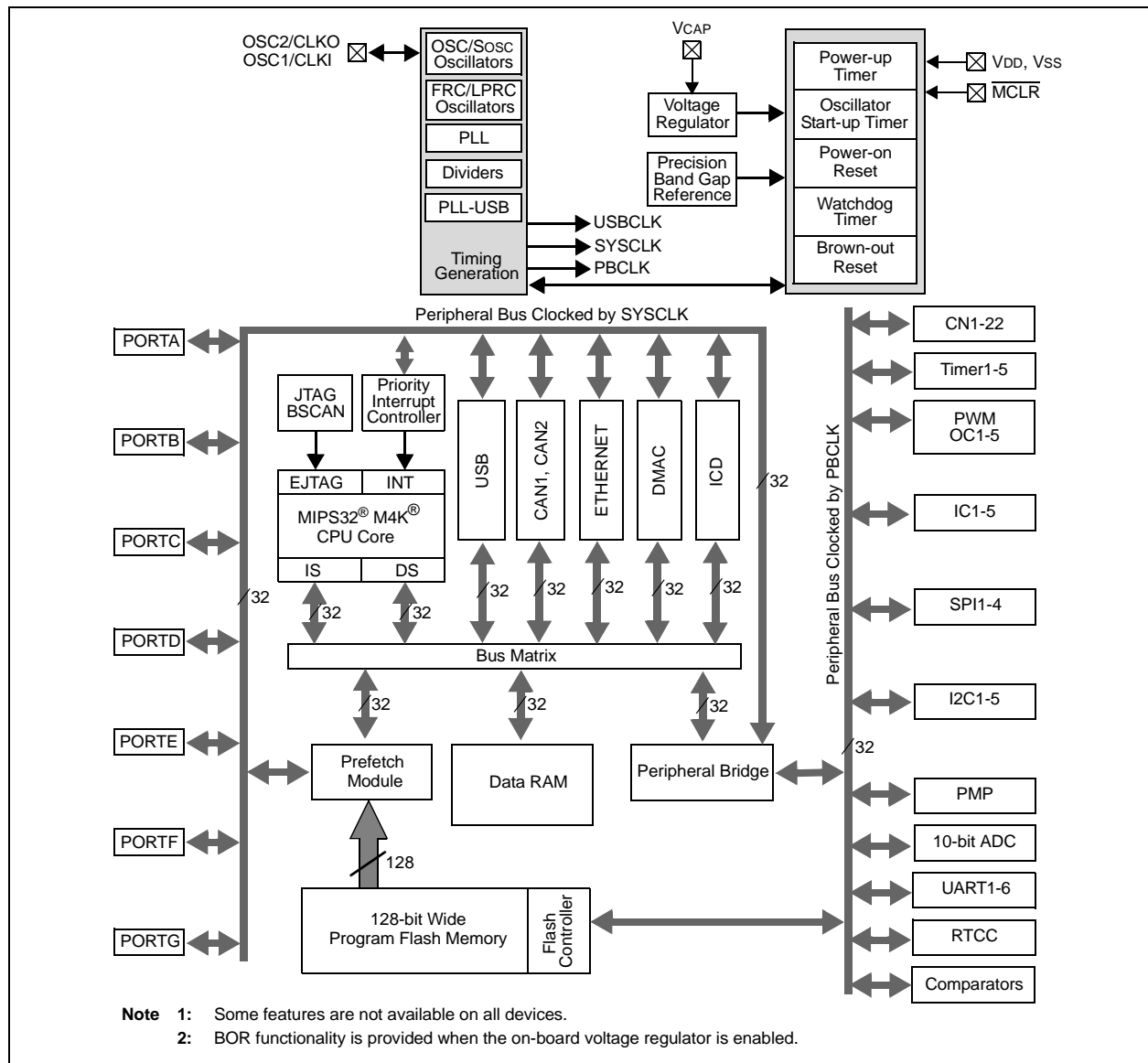
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX5XX/6XX/7XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX5XX/6XX/7XX family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM^(1,2)



3.3 Power Management

The MIPS32 M4K Processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the `WAIT` instruction. For more information on power management, see **Section 28.0 “Power-Saving Features”**.

3.3.2 LOCAL CLOCK GATING

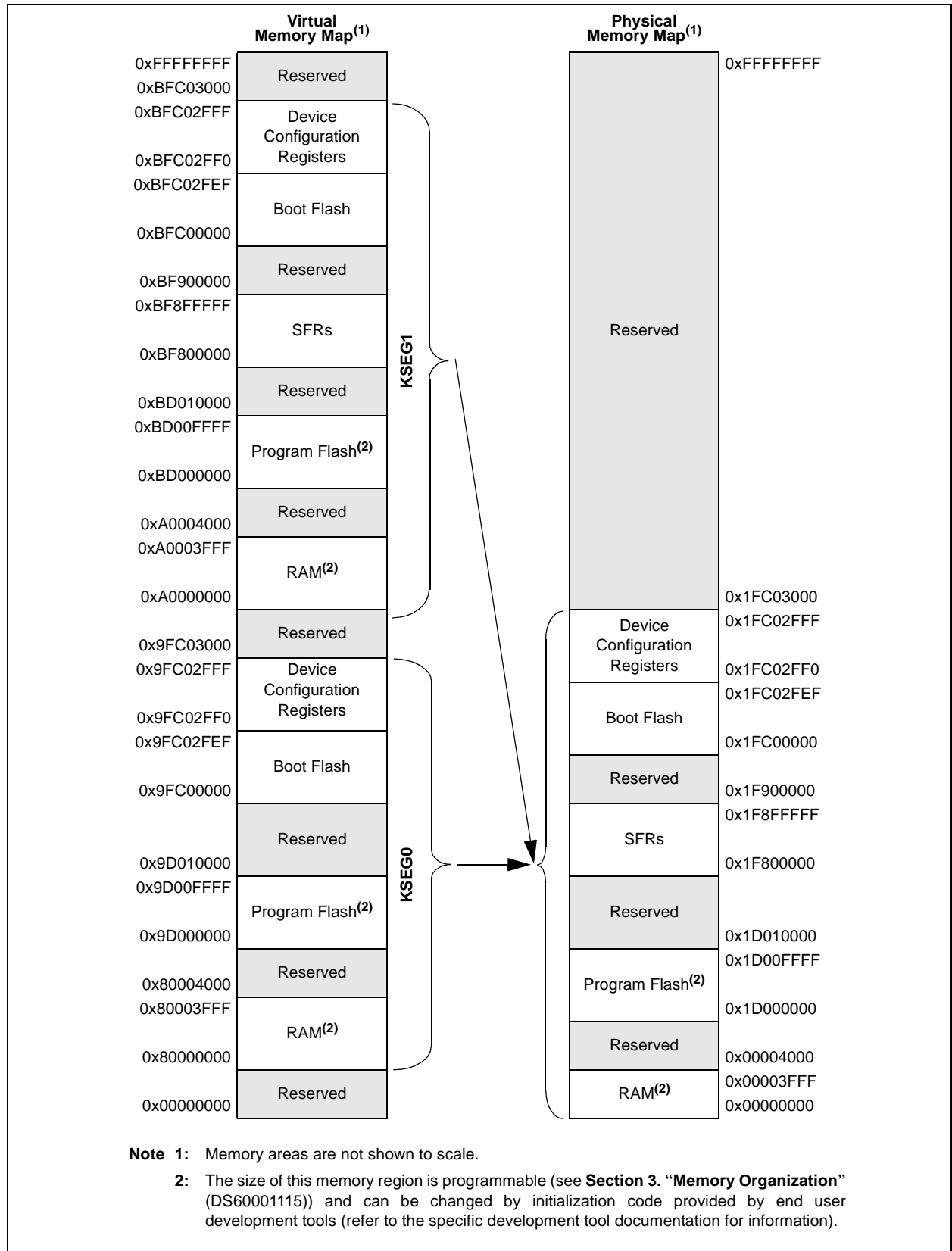
The majority of the power consumed by the PIC32MX-5XX/6XX/7XX family core is in the clock tree and clocking registers. The PIC32 family uses extensive use of local gated clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The MIPS32 M4K Processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the MIPS M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the MIPS32 M4K processor core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX534F064H AND PIC32MX534F064L DEVICES



PIC32MX5XX/6XX/7XX

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	IRQ Number	Vector Number	Interrupt Bit Location			
			Flag	Enable	Priority	Sub-Priority
IC3E – Input Capture 3 Error	63	13	IFS1<31>	IEC1<31>	IPC3<12:10>	IPC3<9:8>
IC4E – Input Capture 4 Error	64	17	IFS2<0>	IEC2<0>	IPC4<12:10>	IPC4<9:8>
IC5E – Input Capture 5 Error	65	21	IFS2<1>	IEC2<1>	IPC5<12:10>	IPC5<9:8>
PMPE – Parallel Master Port Error	66	28	IFS2<2>	IEC2<2>	IPC7<4:2>	IPC7<1:0>
U4E – UART4 Error	67	49	IFS2<3>	IEC2<3>	IPC12<12:10>	IPC12<9:8>
U4RX – UART4 Receiver	68	49	IFS2<4>	IEC2<4>	IPC12<12:10>	IPC12<9:8>
U4TX – UART4 Transmitter	69	49	IFS2<5>	IEC2<5>	IPC12<12:10>	IPC12<9:8>
U6E – UART6 Error	70	50	IFS2<6>	IEC2<6>	IPC12<20:18>	IPC12<17:16>
U6RX – UART6 Receiver	71	50	IFS2<7>	IEC2<7>	IPC12<20:18>	IPC12<17:16>
U6TX – UART6 Transmitter	72	50	IFS2<8>	IEC2<8>	IPC12<20:18>	IPC12<17:16>
U5E – UART5 Error	73	51	IFS2<9>	IEC2<9>	IPC12<28:26>	IPC12<25:24>
U5RX – UART5 Receiver	74	51	IFS2<10>	IEC2<10>	IPC12<28:26>	IPC12<25:24>
U5TX – UART5 Transmitter	75	51	IFS2<11>	IEC2<11>	IPC12<28:26>	IPC12<25:24>
(Reserved)	—	—	—	—	—	—
Lowest Natural Order Priority						

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX5XX USB and CAN Features”**, **TABLE 2: “PIC32MX6XX USB and Ethernet Features”** and **TABLE 3: “PIC32MX7XX USB, Ethernet, and CAN Features”** for the list of available peripherals.

8.0 OSCILLATOR CONFIGURATION

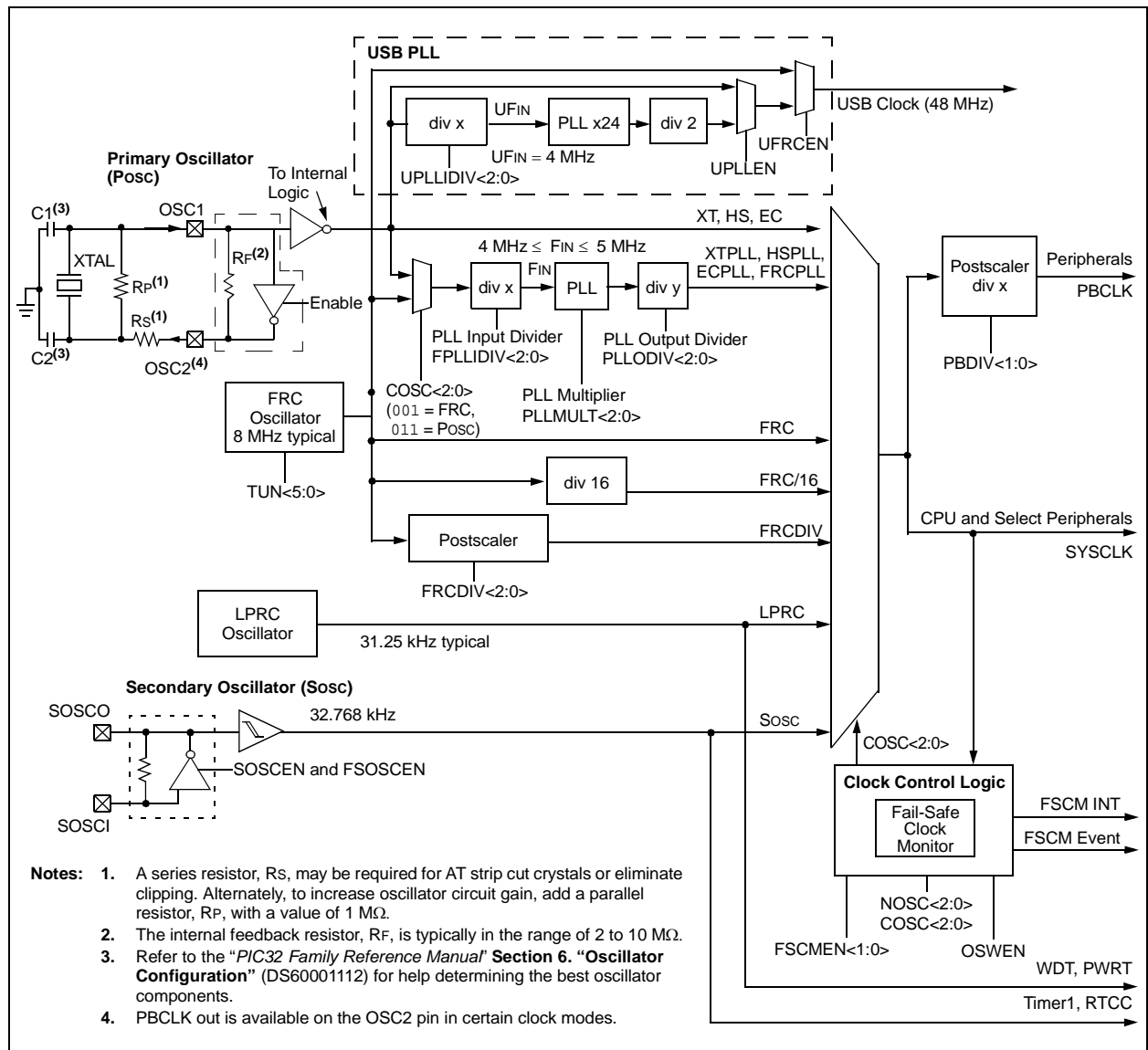
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Oscillator module has the following features:

- A total of four external and internal oscillator options as clock sources
- On-chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

Figure 8-1 shows the Oscillator module block diagram.

FIGURE 8-1: OSCILLATOR BLOCK DIAGRAM



PIC32MX5XX/6XX/7XX

REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits⁽¹⁾

100000 = Center frequency -12.5% for PIC32MX575/595/675/695/775/795 devices

100000 = Center frequency -1.5% for PIC32MX534/564/664/764 devices

100001 =

•

•

•

111111 =

000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)

000001 =

•

•

•

011110 =

011111 = Center frequency +12.5% for PIC32MX575/595/675/695/775/795 devices

011111 = Center frequency +1.5% for PIC32MX534/564/664/764 devices

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the "PIC32 Family Reference Manual" for details.

PIC32MX5XX/6XX/7XX

REGISTER 11-11: U1CON: USB CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	JSTATE	SE0	PKTDIS ⁽⁴⁾ TOKBUSY ^(1,5)	USBRST	HOSTEN ⁽²⁾	RESUME ⁽³⁾	PPBRST	USBEN ⁽⁴⁾ SOFEN ⁽⁵⁾

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit

1 = JSTATE was detected on the USB

0 = JSTATE was not detected

bit 6 **SE0:** Live Single-Ended Zero flag bit

1 = Single-ended zero was detected on the USB

0 = Single-ended zero was not detected

bit 5 **PKTDIS:** Packet Transfer Disable bit⁽⁴⁾

1 = Token and packet processing disabled (set upon SETUP token received)

0 = Token and packet processing enabled

TOKBUSY: Token Busy Indicator bit^(1,5)

1 = Token being executed by the USB module

0 = No token being executed

bit 4 **USBRST:** Module Reset bit⁽⁵⁾

1 = USB reset is generated

0 = USB reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit⁽²⁾

1 = USB host capability is enabled

0 = USB host capability is disabled

bit 2 **RESUME:** RESUME Signaling Enable bit⁽³⁾

1 = RESUME signaling is activated

0 = RESUME signaling is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).

2: All host control logic is reset any time that the value of this bit is toggled.

3: Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.

4: Device mode.

5: Host mode.

PIC32MX5XX/6XX/7XX

REGISTER 11-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	FRMH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** Upper 3 bits of the Frame Numbers bits

These register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 11-15: U1TOK: USB TOKEN REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PID<3:0>				EP<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits⁽¹⁾

1101 = SETUP (TX) token type transaction

1001 = IN (RX) token type transaction

0001 = OUT (TX) token type transaction

Note: All other values not listed, are Reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits

The four bit value must specify a valid endpoint.

PIC32MX5XX/6XX/7XX

REGISTER 14-1: TXCON: TYPE B TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON ^(1,3)	—	SIDL ⁽⁴⁾	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE ⁽³⁾	TCKPS<2:0> ⁽³⁾			T32 ⁽²⁾	—	TCS ⁽³⁾	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit^(1,3)

1 = Module is enabled

0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit⁽⁴⁾

1 = Discontinue operation when device enters Idle mode

0 = Continue operation when device is in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽³⁾

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits⁽³⁾

111 = 1:256 prescale value

110 = 1:64 prescale value

101 = 1:32 prescale value

100 = 1:16 prescale value

011 = 1:8 prescale value

010 = 1:4 prescale value

001 = 1:2 prescale value

000 = 1:1 prescale value

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLOCK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only available on even numbered timers (Timer2 and Timer4).

3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, and Timer5). All timer functions are set through the even numbered timers.

4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit⁽¹⁾

1 = Module is enabled

0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit

1 = Halt in Idle mode

0 = Continue to operate in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)

1 = Capture rising edge first

0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit

1 = 32-bit timer resource capture

0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')

1 = Timer2 is the counter source for capture

0 = Timer3 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits

11 = Interrupt on every fourth capture event

10 = Interrupt on every third capture event

01 = Interrupt on every second capture event

00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)

1 = Input capture overflow is occurred

0 = No input capture overflow is occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)

1 = Input capture buffer is not empty; at least one more capture value can be read

0 = Input capture buffer is empty

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLOCK cycle immediately following the instruction that clears the module's ON bit.

18.1 Control Registers

TABLE 18-1: SPI1 THROUGH SPI4 REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
5E00	SPI1CON ⁽²⁾	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5E10	SPI1STAT ⁽²⁾	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5E20	SPI1BUF ⁽²⁾	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5E30	SPI1BRG ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5800	SPI3CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5810	SPI3STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5820	SPI3BUF	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5830	SPI3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5A10	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5A20	SPI2BUF	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5C00	SPI4CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5C10	SPI4STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5C20	SPI4BUF	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5C30	SPI4BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This register is not available on 64-pin devices.

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Figure 20-2 and Figure 20-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 20-2: UART RECEPTION

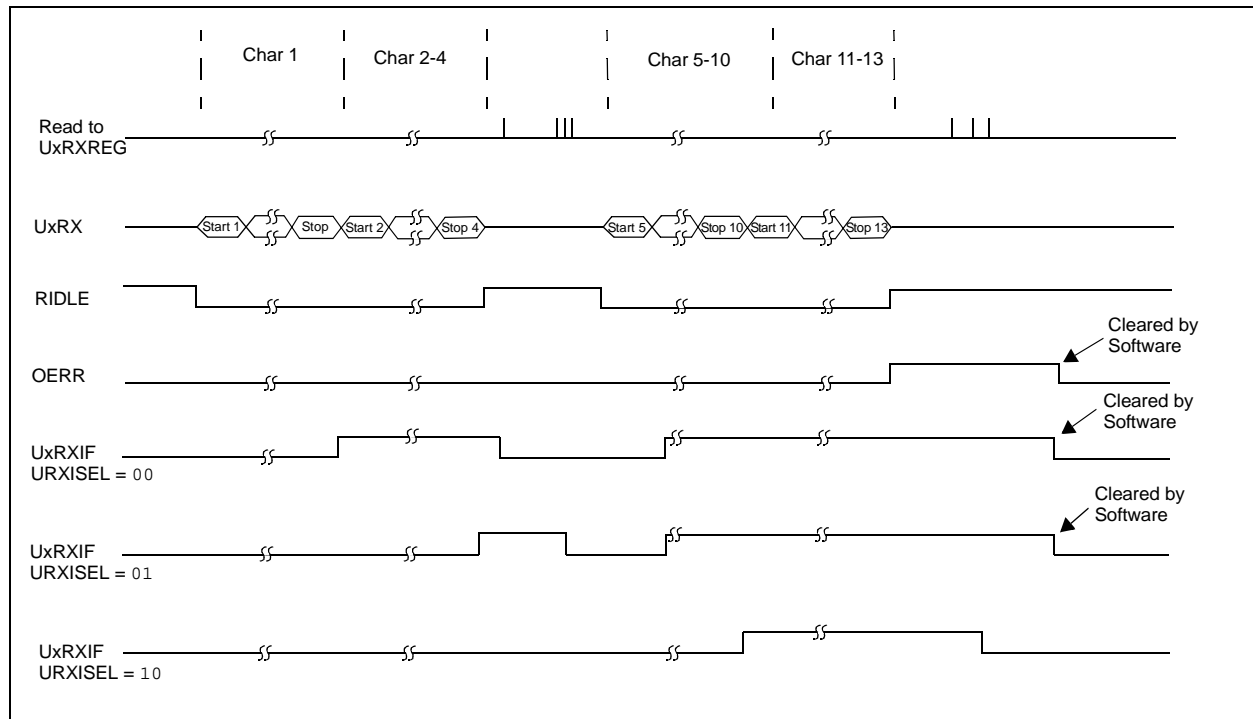
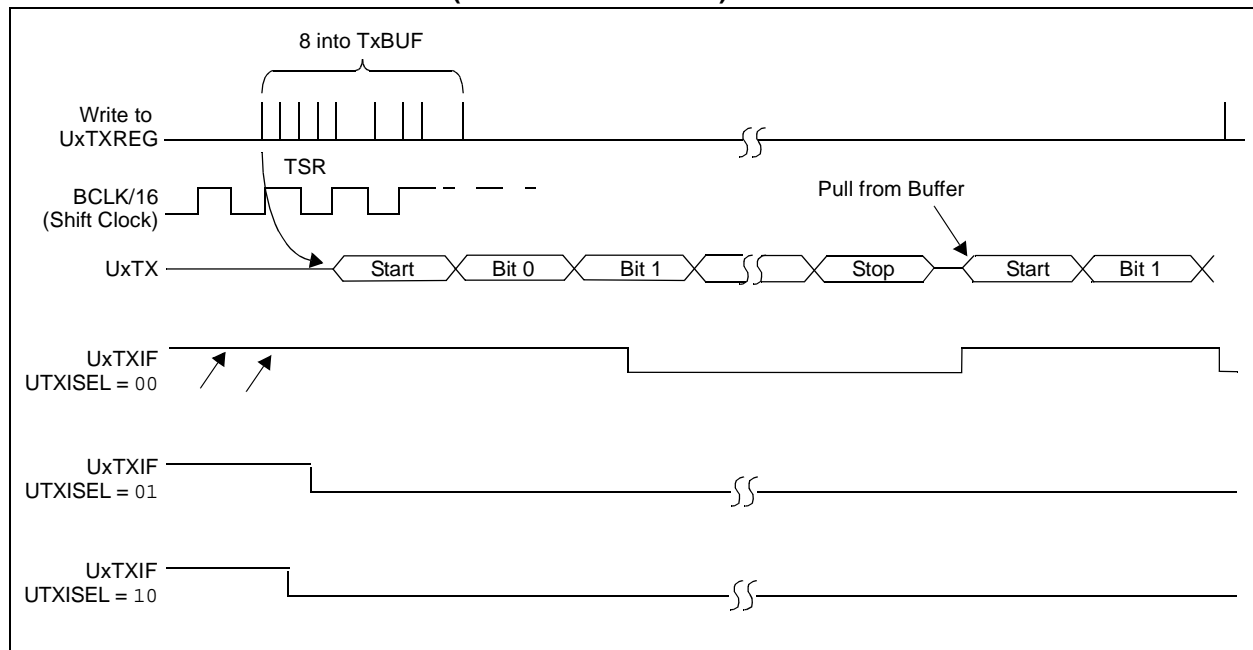


FIGURE 20-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



REGISTER 24-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>**: Propagation Time Segment bits⁽⁴⁾

111 = Length is 8 x T_Q

•
•
•

000 = Length is 1 x T_Q

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits⁽³⁾

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

111111 = T_Q = (2 x 64)/F_{SYS}

111110 = T_Q = (2 x 63)/F_{SYS}

•
•
•

000001 = T_Q = (2 x 2)/F_{SYS}

000000 = T_Q = (2 x 1)/F_{SYS}

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

2: 3 Time bit sampling is not allowed for BRP < 2.

3: SJW ≤ SEG2PH.

4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

REGISTER 24-3: CiINT: CAN INTERRUPT REGISTER (CONTINUED)

- bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred
- bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred
- bit 12 **SERRIF:** System Error Interrupt Flag bit
1 = A system error occurred (typically an illegal address was presented to the system bus)
0 = A system error has not occurred
- bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred
- bit 10-4 **Unimplemented:** Read as '0'
- bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred
- bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred
- bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending
- bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

Note 1: This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CiCON<15>).

27.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. “Comparator Voltage Reference (CVREF)”** (DS60001109) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

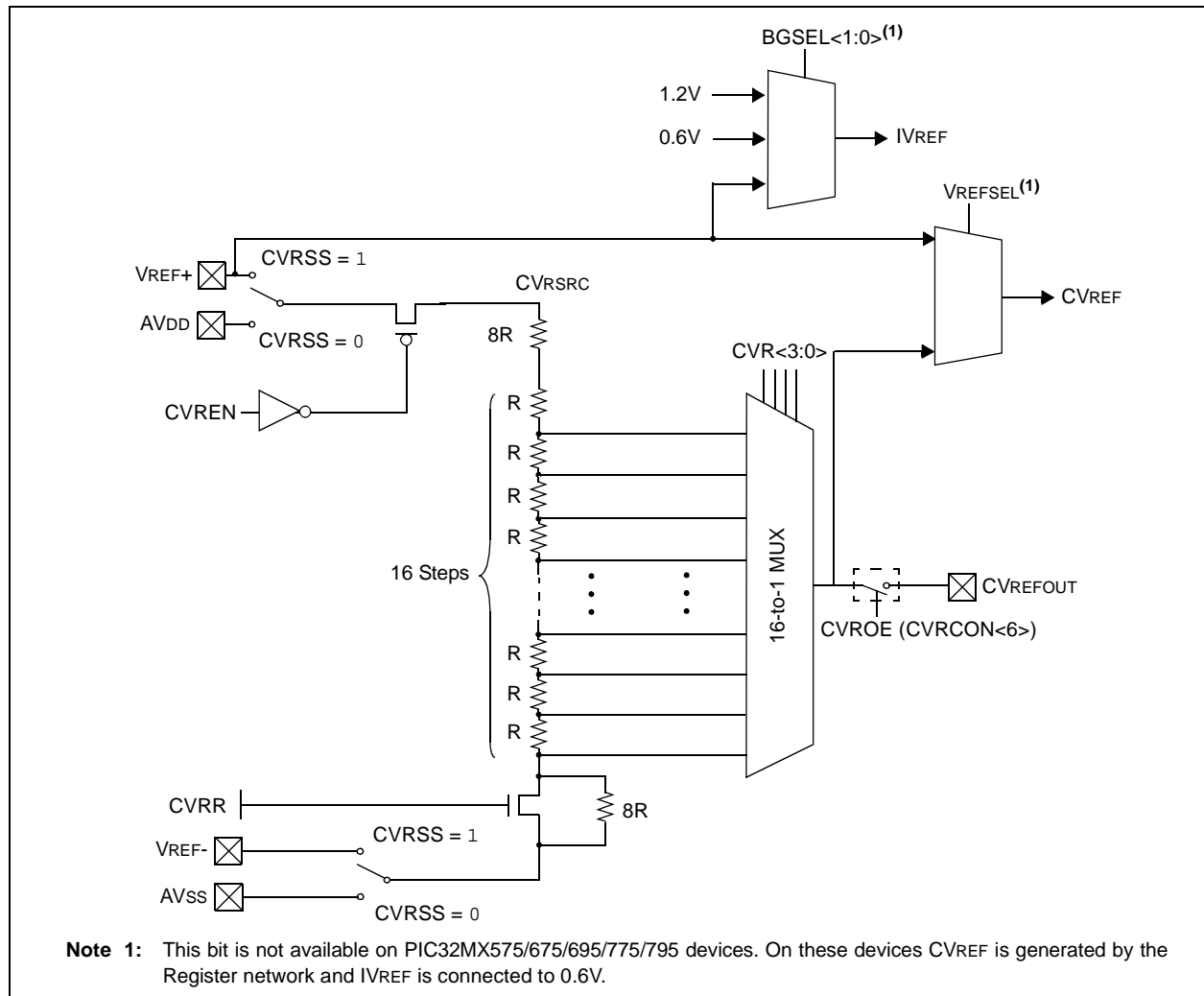
The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is illustrated in Figure 27-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

Key features of the CVREF module include:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

FIGURE 27-1: COMPARATOR VOLTAGE REFERENCE MODULE BLOCK DIAGRAM



32.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX5XX/6XX/7XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX5XX/6XX/7XX devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias.....	-40°C to +105°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3).....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V (Note 3).....	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V (Note 3).....	-0.3V to +3.6V
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin(s)	300 mA
Maximum current into VDD pin(s) (Note 2).....	300 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2).....	200 mA

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

3: See the “**Device Pin Tables**” section for the 5V tolerant pins.

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TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions		
Idle Current (I _{IDLE}) ⁽¹⁾ for PIC32MX534/564/664/764 Family Devices						
DC30a	1.5	5	mA	-40°C, +25°C, +85°C	—	4 MHz
DC30c	3.5	6		+105°C		
DC31a	7	11		-40°C, +25°C, +85°C		
DC32a	13	20	mA	-40°C, +25°C, +85°C	—	25 MHz (Note 3)
DC33a	17	25	mA	-40°C, +25°C, +85°C	—	80 MHz
DC33c	20	27		+105°C		
DC34c	—	40	μA	-40°C	2.3V	LPRC (31 kHz) (Note 3)
DC34d		75		+25°C		
DC34e		800		+85°C		
DC34f		1000		+105°C		
DC35c	30	—	μA	-40°C	3.3V	
DC35d	55			+25°C		
DC35e	230			+85°C		
DC35f	800			+105°C		
DC36c	—	43	μA	-40°C	3.6V	
DC36d		106		+25°C		
DC36e		800		+85°C		
DC36f		1000		+105°C		

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0)
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to V_{SS}
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
- 2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** This parameter is characterized, but not tested in manufacturing.
- 4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

FIGURE 32-5: EXTERNAL RESET TIMING CHARACTERISTICS

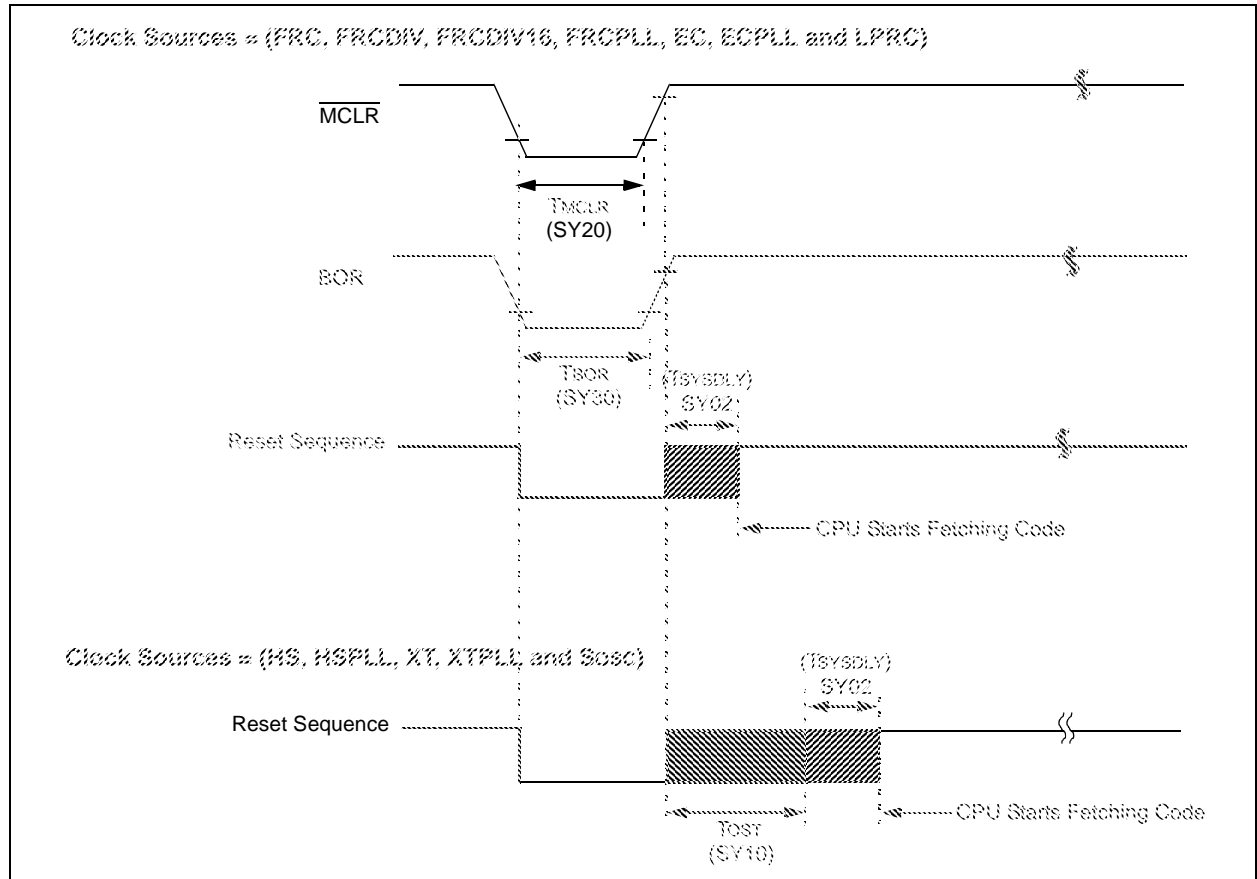


TABLE 32-22: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	-40°C to +85°C
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	—	1 μs + 8 SYSCLK cycles	—	—	-40°C to +85°C
SY20	TMCLR	MCLR Pulse Width (low)	—	2	—	μs	-40°C to +85°C
SY30	TBOR	BOR Pulse Width (low)	—	1	—	μs	-40°C to +85°C

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.