



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx564f064h-i-mr

PIC32MX5XX/6XX/7XX

TABLE 2: PIC32MX6XX USB AND ETHERNET FEATURES

USB and Ethernet																
Device	Pins	Program Memory (KB)	Data Memory (KB)	USB	Ethernet	Timers/Capture/Compare	DMA Channels (Programmable/Dedicated)	UART ^(2,3)	SPI ⁽³⁾	I ² C ⁽³⁾	10-bit 1 Msps ADC (Channels)	Comparators	PMP/PSP	JTAG	Trace	Packages ⁽⁴⁾
PIC32MX664F064H	64	64 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX664F128H	64	128 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX675F256H	64	256 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX675F512H	64	512 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX695F512H	64	512 + 12 ⁽¹⁾	128	1	1	5/5/5	8/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX664F064L	100	64 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX664F128L	100	128 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX675F256L	100	256 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX675F512L	100	512 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG, TL
PIC32MX695F512L	100	512 + 12 ⁽¹⁾	128	1	1	5/5/5	8/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG, TL

Legend: PF, PT = TQFP MR = QFN BG = TFBGA TL = VTLA⁽⁵⁾

Note 1: This device features 12 KB boot Flash memory.

2: CTS and RTS pins may not be available for all UART modules. Refer to the “**Device Pin Tables**” section for more information.

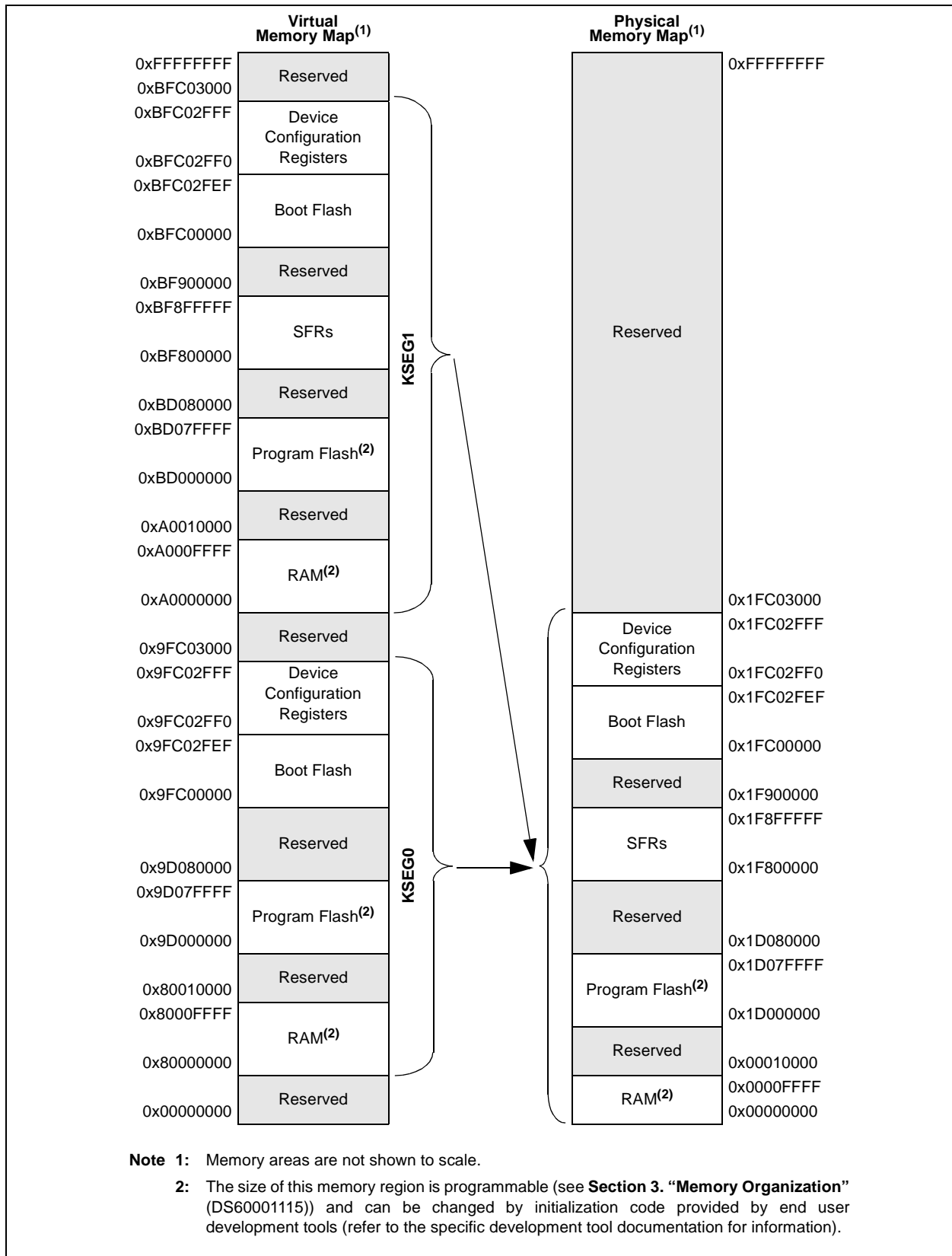
3: Some pins between the UART, SPI and I²C modules may be shared. Refer to the “**Device Pin Tables**” section for more information.

4: Refer to **34.0 “Packaging Information”** for more information.

5: 100-pin devices other than those listed here are available in the VTLA package upon request. Please contact your local Microchip Sales Office for details.

PIC32MX5XX/6XX/7XX

FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX575F512H, PIC32MX575F512L, PIC32MX675F512H, PIC32MX675F512L, PIC32MX775F512H AND PIC32MX775F512L DEVICES



7.0 INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. “Interrupts”** (DS60001108) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX5XX/6XX/7XX devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The Interrupt Controller module includes the following features:

- Up to 96 interrupt sources
- Up to 64 interrupt vectors
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable sub-priority levels within each priority
- Dedicated shadow set for user-selectable priority level
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

A simplified block diagram of the Interrupt Controller module is illustrated in Figure 7-1.

FIGURE 7-1: INTERRUPT CONTROLLER MODULE

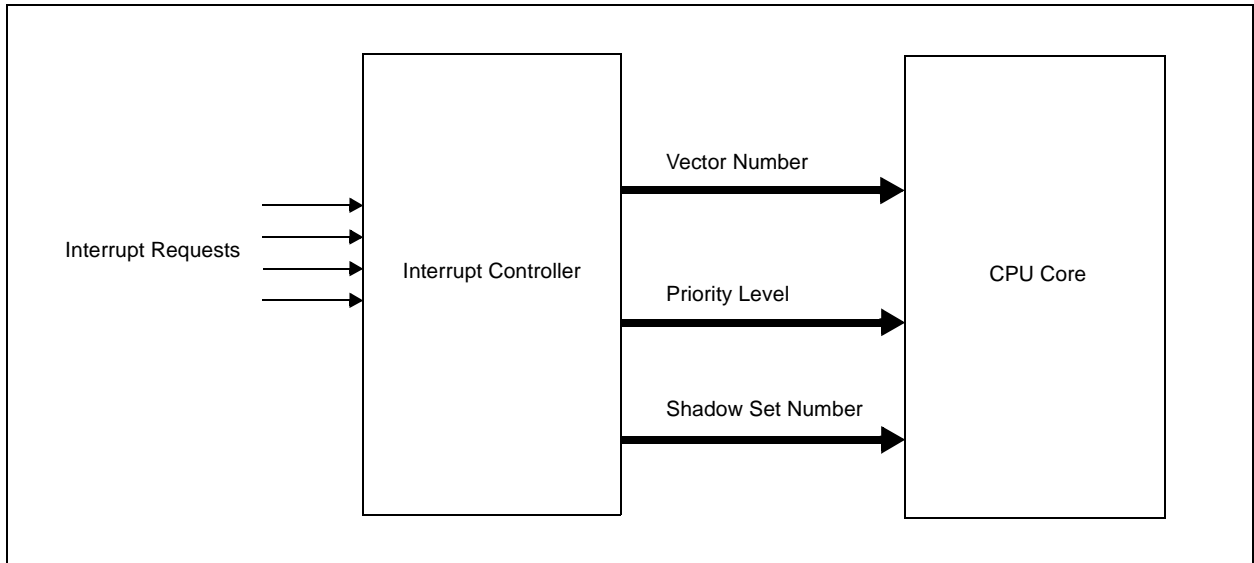


TABLE 7-5: INTERRUPT REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L PIC32MX575F512L AND PIC32MX575F256L DEVICES

Virtual Address (BF88 #)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>				—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
1010	INTSTAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>				—	—	VEC<5:0>					0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	SPI1TXIF	SPI1RXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	IC3EIF	IC2EIF	IC1EIF	—	—	CAN1IF	USBIF	FCEIF	DMA7IF ⁽²⁾	DMA6IF ⁽²⁾	DMA5IF ⁽²⁾	DMA4IF ⁽²⁾	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	U3TXIF	U3RXIF	U3EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
								SPI4TXIF	SPI4RXIF	SPI4EIF	SPI2TXIF	SPI2RXIF	SPI2EIF						
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	SPI1TXIE	SPI1RXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	IC3EIE	IC2EIE	IC1EIE	—	—	CAN1IE	USBIE	FCEIE	DMA7IE ⁽²⁾	DMA6IE ⁽²⁾	DMA5IE ⁽²⁾	DMA4IE ⁽²⁾	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	U3TXIE	U3RXIE	U3EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
								SPI4TXIE	SPI4RXIE	SPI4EIE	SPI2TXIE	SPI2RXIE	SPI2EIE						
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>			—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>			—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>			—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>			—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>			—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>			—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>			—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>			—	—	T3IP<2:0>			T3IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
 - 2: These bits are not available on PIC32MX534/564 devices.
 - 3: This register does not have associated CLR, SET, and INV registers.

PIC32MX5XX/6XX/7XX

REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits⁽¹⁾

100000 = Center frequency -12.5% for PIC32MX575/595/675/695/775/795 devices

100000 = Center frequency -1.5% for PIC32MX534/564/664/764 devices

100001 =

•

•

•

111111 =

000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)

000001 =

•

•

•

011110 =

011111 = Center frequency +12.5% for PIC32MX575/595/675/695/775/795 devices

011111 = Center frequency +1.5% for PIC32MX534/564/664/764 devices

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the "PIC32 Family Reference Manual" for details.

REGISTER 9-1: CHECON: CACHE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	CHECOH
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DCSZ<1:0>	
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	PREFEN<1:0>		—	PFMWS<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-17 **Unimplemented:** Write '0'; ignore read

bit 16 **CHECOH:** Cache Coherency Setting on a PFM Program Cycle bit

1 = Invalidate all data and instruction lines

0 = Invalidate all data lines and instruction lines that are not locked

bit 15-10 **Unimplemented:** Write '0'; ignore read

bit 9-8 **DCSZ<1:0>:** Data Cache Size in Lines bits

Changing these bits causes all lines to be reinitialized to the "invalid" state.

11 = Enable data caching with a size of 4 lines

10 = Enable data caching with a size of 2 lines

01 = Enable data caching with a size of 1 line

00 = Disable data caching

bit 7-6 **Unimplemented:** Write '0'; ignore read

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits

11 = Enable predictive prefetch for both cacheable and non-cacheable regions

10 = Enable predictive prefetch only for non-cacheable regions

01 = Enable predictive prefetch only for cacheable regions

00 = Disable predictive prefetch

bit 3 **Unimplemented:** Write '0'; ignore read

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSLK Wait States bits

111 = Seven Wait states

110 = Six Wait states

101 = Five Wait states

100 = Four Wait states

011 = Three Wait states

010 = Two Wait states

001 = One Wait state

000 = Zero Wait state

REGISTER 11-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
 1 = Reset all Even/Odd buffer pointers to the Even buffer descriptor banks
 0 = Even/Odd buffer pointers are not reset
- bit 0 **USBEN:** USB Module Enable bit⁽⁴⁾
 1 = USB module and supporting circuitry is enabled
 0 = USB module and supporting circuitry is disabled
- SOFEN:** SOF Enable bit⁽⁵⁾
 1 = SOF token is sent every 1 ms
 0 = SOF token is disabled

- Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).
- 2:** All host control logic is reset any time that the value of this bit is toggled.
- 3:** Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
- 4:** Device mode.
- 5:** Host mode.

PIC32MX5XX/6XX/7XX

REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

- bit 3 **CS1P:** Chip Select 0 Polarity bit⁽²⁾
 1 = Active-high (PMCS1)
 0 = Active-low (PMCS1)
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **WRSP:** Write Strobe Polarity bit
 For Slave Modes and Master mode 2 (PMMODE<9:8> = 00,01,10):
 1 = Write strobe active-high (PMWR)
 0 = Write strobe active-low (PMWR)
 For Master mode 1 (PMMODE<9:8> = 11):
 1 = Enable strobe active-high (PMENB)
 0 = Enable strobe active-low (PMENB)
- bit 0 **RDSP:** Read Strobe Polarity bit
 For Slave modes and Master mode 2 (PMMODE<9:8> = 00,01,10):
 1 = Read Strobe active-high (PMRD)
 0 = Read Strobe active-low (PMRD)
 For Master mode 1 (PMMODE<9:8> = 11):
 1 = Read/write strobe active-high (PMRD/PMWR)
 0 = Read/write strobe active-low (PMRD/PMWR)

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 24-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>**: Propagation Time Segment bits⁽⁴⁾

111 = Length is 8 x T_Q

•
•
•

000 = Length is 1 x T_Q

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits⁽³⁾

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

111111 = T_Q = (2 x 64)/F_{SYS}

111110 = T_Q = (2 x 63)/F_{SYS}

•
•
•

000001 = T_Q = (2 x 2)/F_{SYS}

000000 = T_Q = (2 x 1)/F_{SYS}

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

2: 3 Time bit sampling is not allowed for BRP < 2.

3: SJW ≤ SEG2PH.

4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

PIC32MX5XX/6XX/7XX

REGISTER 25-30: EMAC1TEST: ETHERNET CONTROLLER MAC TEST REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TESTBP	TESTPAUSE ⁽¹⁾	SHRTQNTA ⁽¹⁾

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **TESTBP:** Test Backpressure bit

1 = The MAC will assert backpressure on the link. Backpressure causes preamble to be transmitted, raising carrier sense. A transmit packet from the system will be sent during backpressure.

0 = Normal operation

bit 1 **TESTPAUSE:** Test PAUSE bit⁽¹⁾

1 = The MAC Control sub-layer will inhibit transmissions, just as if a PAUSE Receive Control frame with a non-zero pause time parameter was received

0 = Normal operation

bit 0 **SHRTQNTA:** Shortcut PAUSE Quanta bit⁽¹⁾

1 = The MAC reduces the effective PAUSE Quanta from 64 byte-times to 1 byte-time

0 = Normal operation

Note 1: This bit is only for testing purposes.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

PIC32MX5XX/6XX/7XX

REGISTER 25-34: EMAC1MWTD: ETHERNET CONTROLLER MAC MII MANAGEMENT WRITE DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MWTD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MWTD<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MWTD<15:0>:** MII Management Write Data bits

When written, a MII Management write cycle is performed using the 16-bit data and the pre-configured PHY and Register addresses from the EMAC1MADR register.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 25-35: EMAC1MRDD: ETHERNET CONTROLLER MAC MII MANAGEMENT READ DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MRDD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MRDD<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MRDD<15:0>:** MII Management Read Data bits

Following a MII Management Read Cycle, the 16-bit data can be read from this location.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

26.1 Control Registers

TABLE 26-1: COMPARATOR REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

PIC32MX5XX/6XX/7XX

FIGURE 32-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS

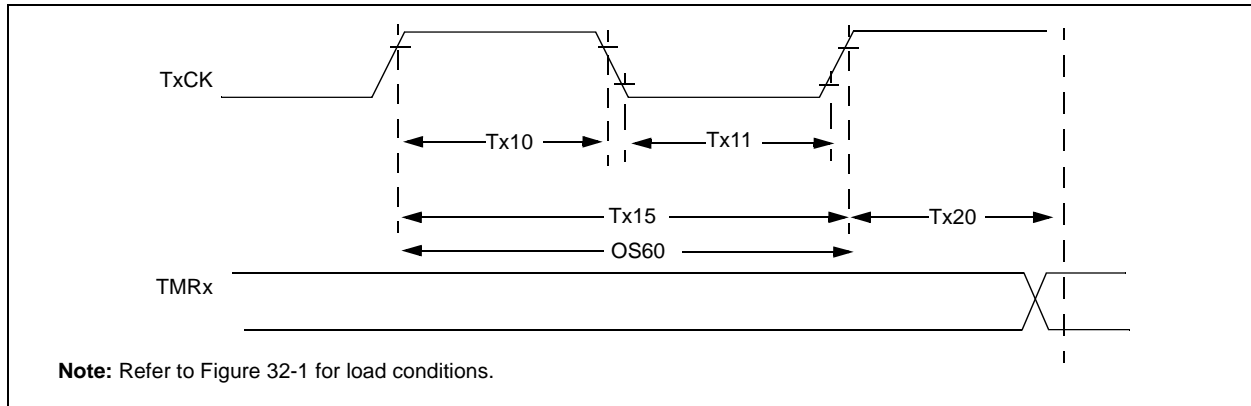


TABLE 32-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽²⁾		Min.	Typical	Max.	Units	Conditions
TA10	TtxH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TtxL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TtxP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 ns or 2 TPB)/N] + 30 ns	—	—	ns	VDD > 2.7V
				[(Greater of 25 ns or 2 TPB)/N] + 50 ns	—	—	ns	VDD < 2.7V
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V (Note 3)
				50	—	—	ns	VDD < 2.7V (Note 3)
OS60	Ft1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	100	kHz	—
TA20	TckEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	—	1	TPB	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

PIC32MX5XX/6XX/7XX

TABLE 32-35: ETHERNET MODULE SPECIFICATIONS

AC CHARACTERISTICS		Standard Operating Conditions (see Note 1): 2.9V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Characteristic	Min.	Typical	Max.	Units	Conditions
MIIM Timing Requirements						
ET1	MDC Duty Cycle	40	—	60	%	—
ET2	MDC Period	400	—	—	ns	—
ET3	MDIO Output Setup and Hold	10	—	10	ns	See Figure 32-19
ET4	MDIO Input Setup and Hold	0	—	300	ns	See Figure 32-20
MII Timing Requirements						
ET5	TX Clock Frequency	—	25	—	MHz	—
ET6	TX Clock Duty Cycle	35	—	65	%	—
ET7	ETXDx, ETEN, ETXERR Output Delay	0	—	25	ns	See Figure 32-21
ET8	RX Clock Frequency	—	25	—	MHz	—
ET9	RX Clock Duty Cycle	35	—	65	%	—
ET10	ERXDx, ERXDV, ERXERR Setup and Hold	10	—	30	ns	See Figure 32-22
RMII Timing Requirements						
ET11	Reference Clock Frequency	—	50	—	MHz	—
ET12	Reference Clock Duty Cycle	35	—	65	%	—
ET13	ETXDx, ETEN, Setup and Hold	2	—	4	ns	—
ET14	ERXDx, ERXDV, ERXERR Setup and Hold	2	—	4	ns	—

Note 1: The Ethernet module is functional at VBORMIN < VDD < 2.9V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 32-19: MDIO SOURCED BY THE PIC32 DEVICE

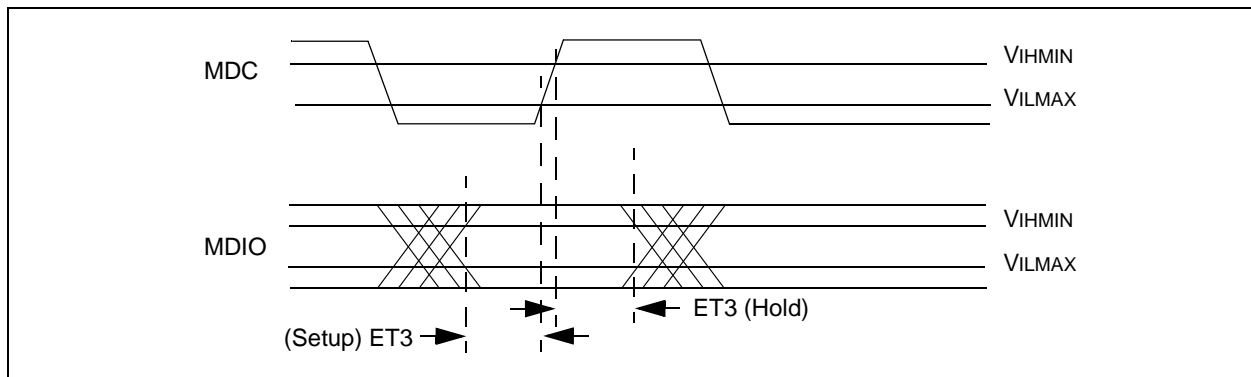


FIGURE 32-20: MDIO SOURCED BY THE PHY

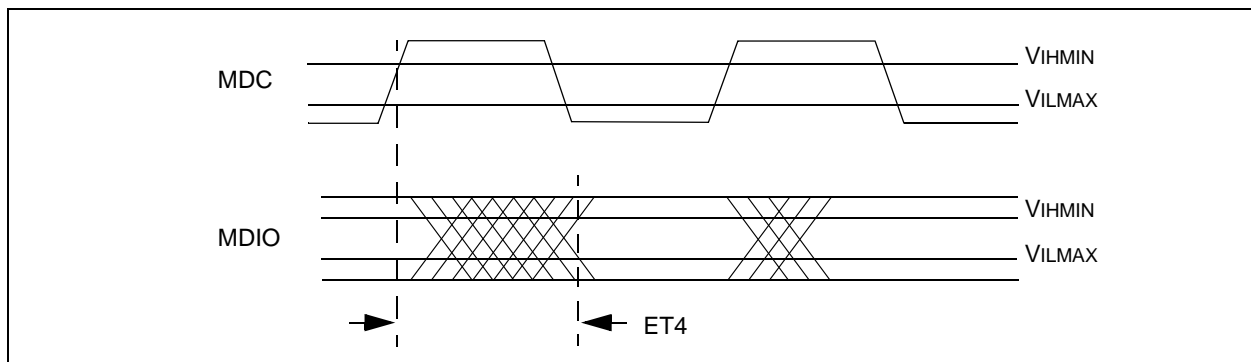


FIGURE 32-21: TRANSMIT SIGNAL TIMING RELATIONSHIPS AT THE MII

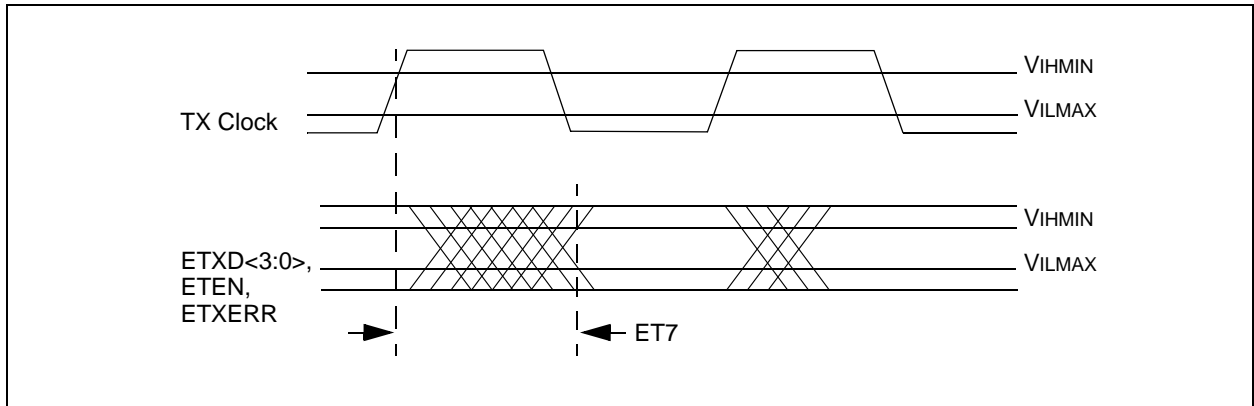
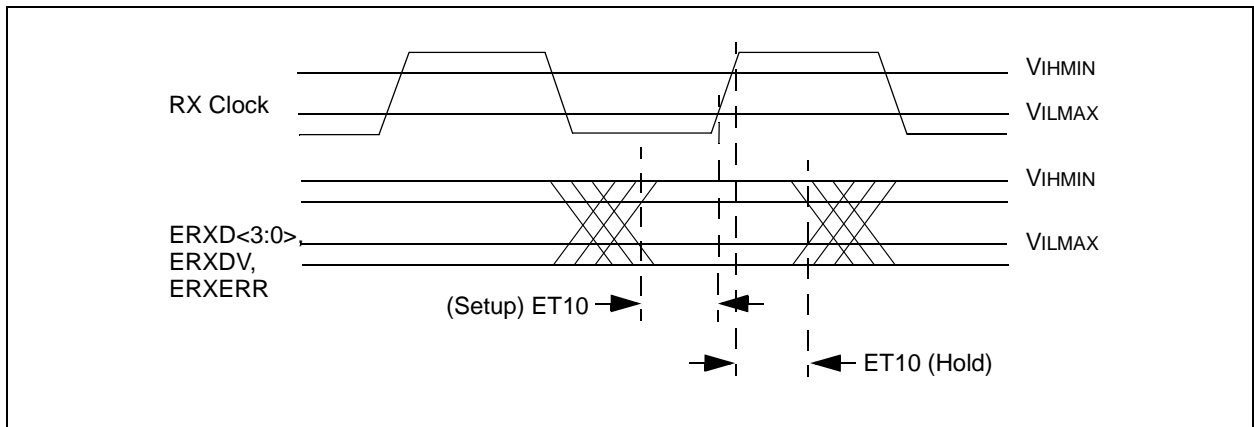


FIGURE 32-22: RECEIVE SIGNAL TIMING RELATIONSHIPS AT THE MII



PIC32MX5XX/6XX/7XX

FIGURE 32-25: PARALLEL SLAVE PORT TIMING

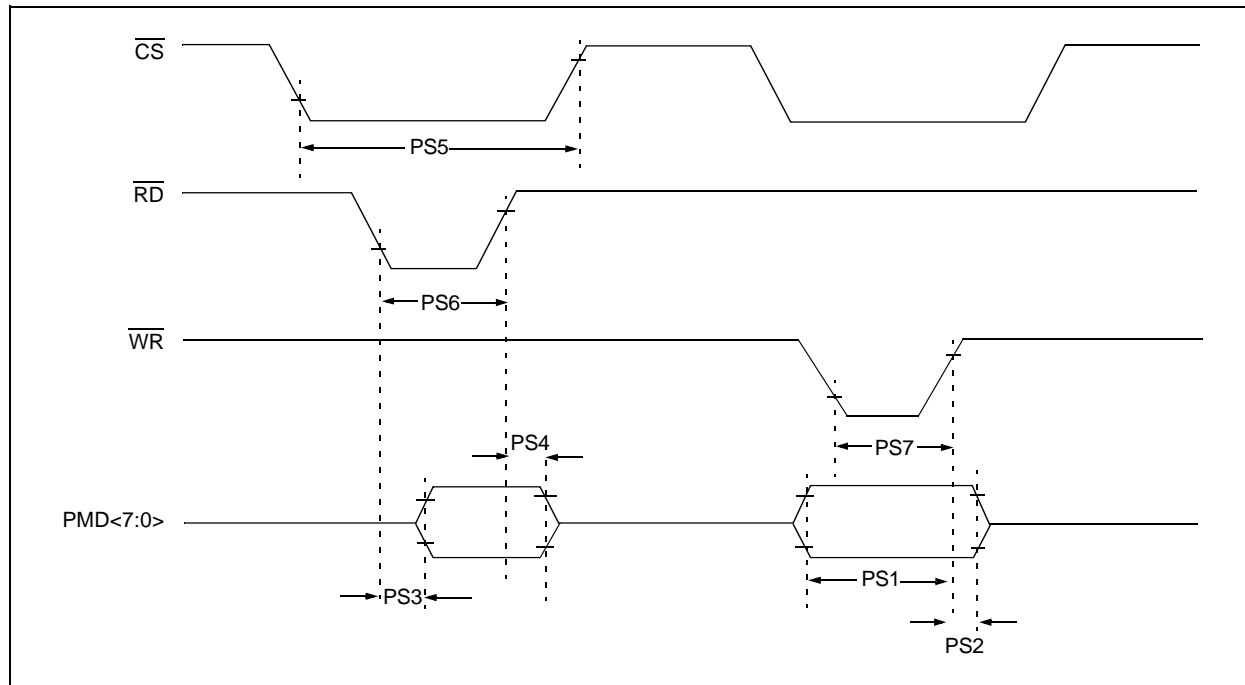


TABLE 32-39: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)			
				Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp			
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PS1	TdtV2wrH	Data In Valid before \overline{WR} or \overline{CS} Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtI	\overline{WR} or \overline{CS} Inactive to Data-In Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	\overline{RD} and \overline{CS} Active to Data-Out Valid	—	—	60	ns	—
PS4	TrdH2dtI	\overline{RD} Active or \overline{CS} Inactive to Data-Out Invalid	0	—	10	ns	—
PS5	Tcs	\overline{CS} Active Time	$TPB + 40$	—	—	ns	—
PS6	TWR	\overline{WR} Active Time	$TPB + 25$	—	—	ns	—
PS7	TRD	\overline{RD} Active Time	$TPB + 25$	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 32-42: USB OTG ELECTRICAL SPECIFICATIONS

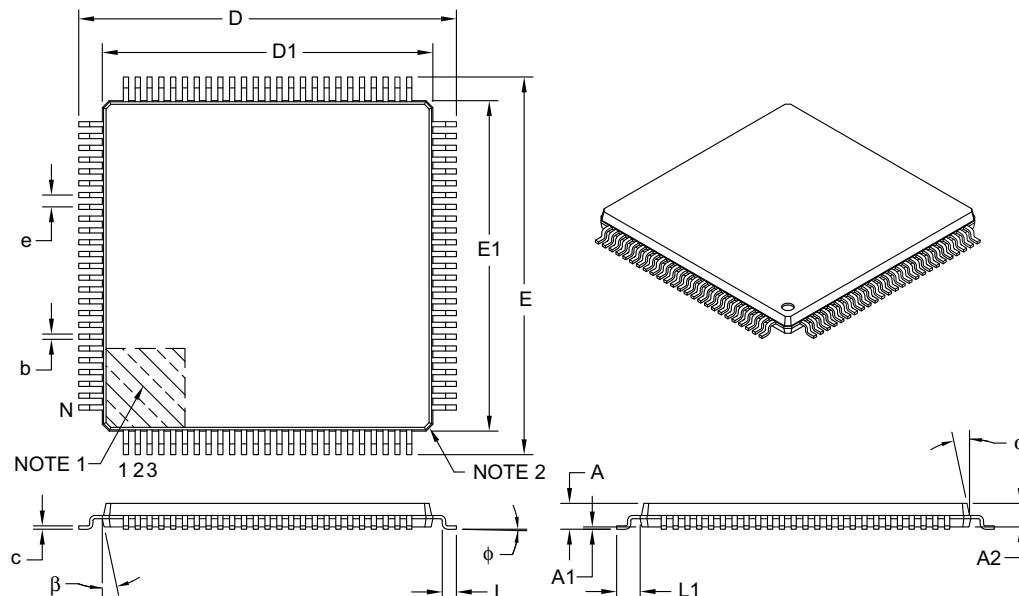
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	—
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized, but not tested in manufacturing.

PIC32MX5XX/6XX/7XX

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	100		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	16.00 BSC		
Overall Length	D	16.00 BSC		
Molded Package Width	E1	14.00 BSC		
Molded Package Length	D1	14.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

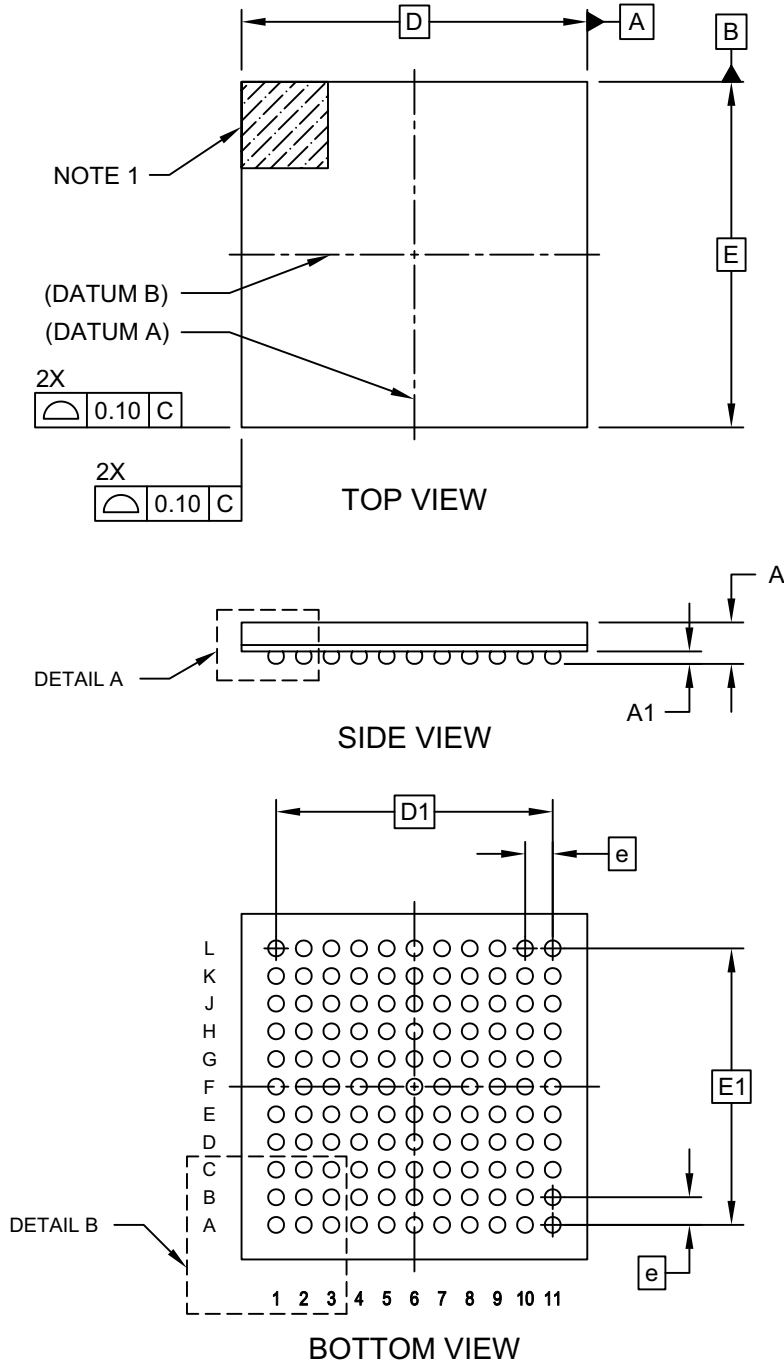
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

PIC32MX5XX/6XX/7XX

121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-148 Rev F Sheet 1 of 2

PIC32MX5XX/6XX/7XX

TABLE B-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
4.0 “Memory Organization” (Continued)	<p>Made the following bit name changes in the I2C1, I2C3, I2C4 and I2C5 Register Map (Table 4-11):</p> <ul style="list-style-type: none"> • I2C3BRG SFR: I2C1BRG was changed to I2C3BRG • I2C4BRG SFR: I2C1BRG was changed to I2C4BRG • I2C5BRG SFR: I2C1BRG was changed to I2C5BRG • I2C4TRN SFR: I2CT1DATA was changed to I2CT2ADATA • I2C4RCV SFR: I2CR2DATA was changed to I2CR2ADATA • I2C5TRN SFR: I2CT1DATA was changed to I2CT3ADATA • I2C5RCV SFR: I2CR1DATA was changed to I2CR3ADATA <p>Added the RTSMD bit and UEN<1:0> bits to the UART1A, UART1B, UART2A, UART2B, UART3A and UART3B Register Map (Table 4-13)</p> <p>Added the SIDL bit to the DMA Global Register Map (Table 4-17).</p> <p>Changed the CM bit to CMR in the System Control Register Map (Table 4-23).</p> <p>Added the following devices to the I2C2, SPI1, PORTA, PORTC, PORTD, PORTE, PORTF, PORTG, Change Notice and Pull-up Register Maps (Table 4-12, Table 4-14, Table 4-24, Table 4-27, Table 4-29, Table 4-31, Table 4-33, Table 4-35 and Table 4-36):</p> <ul style="list-style-type: none"> • PIC32MX534F064L • PIC32MX564F064L • PIC32MX564F128L • PIC32MX664F064L • PIC32MX664F128L • PIC32MX764F128L <p>Added the following devices to the PORTC, PORTD, PORTE, PORTF, PORTG, Change Notice and Pull-up Register Maps (Table 4-26, Table 4-28, Table 4-30, Table 4-32, Table 4-34 and Table 4-37):</p> <ul style="list-style-type: none"> • PIC32MX534F064H • PIC32MX564F064H • PIC32MX564F128H • PIC32MX664F064H • PIC32MX664F128H • PIC32MX764F128H <p>Added the following devices to the CAN1 Register Map (Table 4-45):</p> <ul style="list-style-type: none"> • PIC32MX534F064H • PIC32MX564F064H • PIC32MX564F128H • PIC32MX764F128H • PIC32MX534F064L • PIC32MX564F064L • PIC32MX564F128L • PIC32MX764F128L <p>Added the following devices to the Ethernet Controller Register Map (Table 4-47):</p> <ul style="list-style-type: none"> • PIC32MX664F064H • PIC32MX664F128H • PIC32MX764F128H • PIC32MX664F064L • PIC32MX664F128L • PIC32MX764F128L