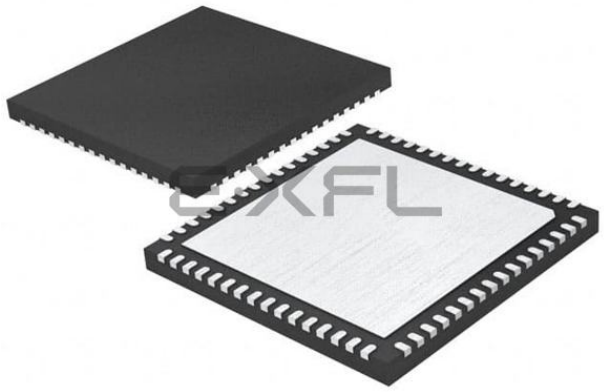

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx564f064h-v-mr

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)

L11

PIC32MX664F064L
PIC32MX664F128L
PIC32MX675F256L
PIC32MX675F512L
PIC32MX695F512L

L1

A11

A1

Note: The TFBGA package skips from row "H" to row "J" and has no "I" row.

Pin #	Full Pin Name
J3	PGED2/AN7/RB7
J4	AVDD
J5	AN11/ERXERR/AETXERR/PMA12/RB11
J6	TCK/RA1
J7	AN12/ERXD0/AECRS/PMA11/RB12
J8	No Connect (NC)
J9	No Connect (NC)
J10	SCL3/SDO3/U1TX/RF8
J11	D-/RG3
K1	PGEC1/AN1/CN3/RB1
K2	PGED1/AN0/CN2/RB0
K3	VREF+/CVREF+/AERXD3/PMA6/RA10
K4	AN8/C1OUT/RB8
K5	No Connect (NC)
K6	$\overline{SS4}$/U5RX/$\overline{U2CTS}$/RF12
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14
K8	VDD
K9	AETXD1/SCK3/U4TX/$\overline{U1RTS}$/CN21/RD15
K10	USBID/RF3
K11	SDA3/SDI3/U1RX/RF2
L1	PGEC2/AN6/OCFA/RB6
L2	VREF-/CVREF-/AERXD2/PMA7/RA9
L3	AVSS
L4	AN9/C2OUT/RB9
L5	AN10/CVREFOUT/PMA13/RB10
L6	SCK4/U5TX/$\overline{U2RTS}$/RF13
L7	AN13/ERXD1/AECOL/PMA10/RB13
L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
L9	AETXD0/$\overline{SS3}$/U4RX/$\overline{U1CTS}$/CN20/RD14
L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5

Note 1: Shaded pins are 5V tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
AN0	16	25	K2	B14	I	Analog	Analog input channels
AN1	15	24	K1	A15	I	Analog	
AN2	14	23	J2	B13	I	Analog	
AN3	13	22	J1	A13	I	Analog	
AN4	12	21	H2	B11	I	Analog	
AN5	11	20	H1	A12	I	Analog	
AN6	17	26	L1	A20	I	Analog	
AN7	18	27	J3	B16	I	Analog	
AN8	21	32	K4	A23	I	Analog	
AN9	22	33	L4	B19	I	Analog	
AN10	23	34	L5	A24	I	Analog	
AN11	24	35	J5	B20	I	Analog	
AN12	27	41	J7	B23	I	Analog	
AN13	28	42	L7	A28	I	Analog	
AN14	29	43	K7	B24	I	Analog	
AN15	30	44	L8	A29	I	Analog	
CLKI	39	63	F9	B34	I	ST/ CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	40	64	F11	A42	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	39	63	F9	B34	I	ST/ CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	40	64	F11	A42	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	73	C10	A47	I	ST/ CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise
SOSCO	48	74	B11	B40	O	—	32.768 kHz low-power oscillator crystal output

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

2: See **25.0 "Ethernet Controller"** for more information.

8.0 OSCILLATOR CONFIGURATION

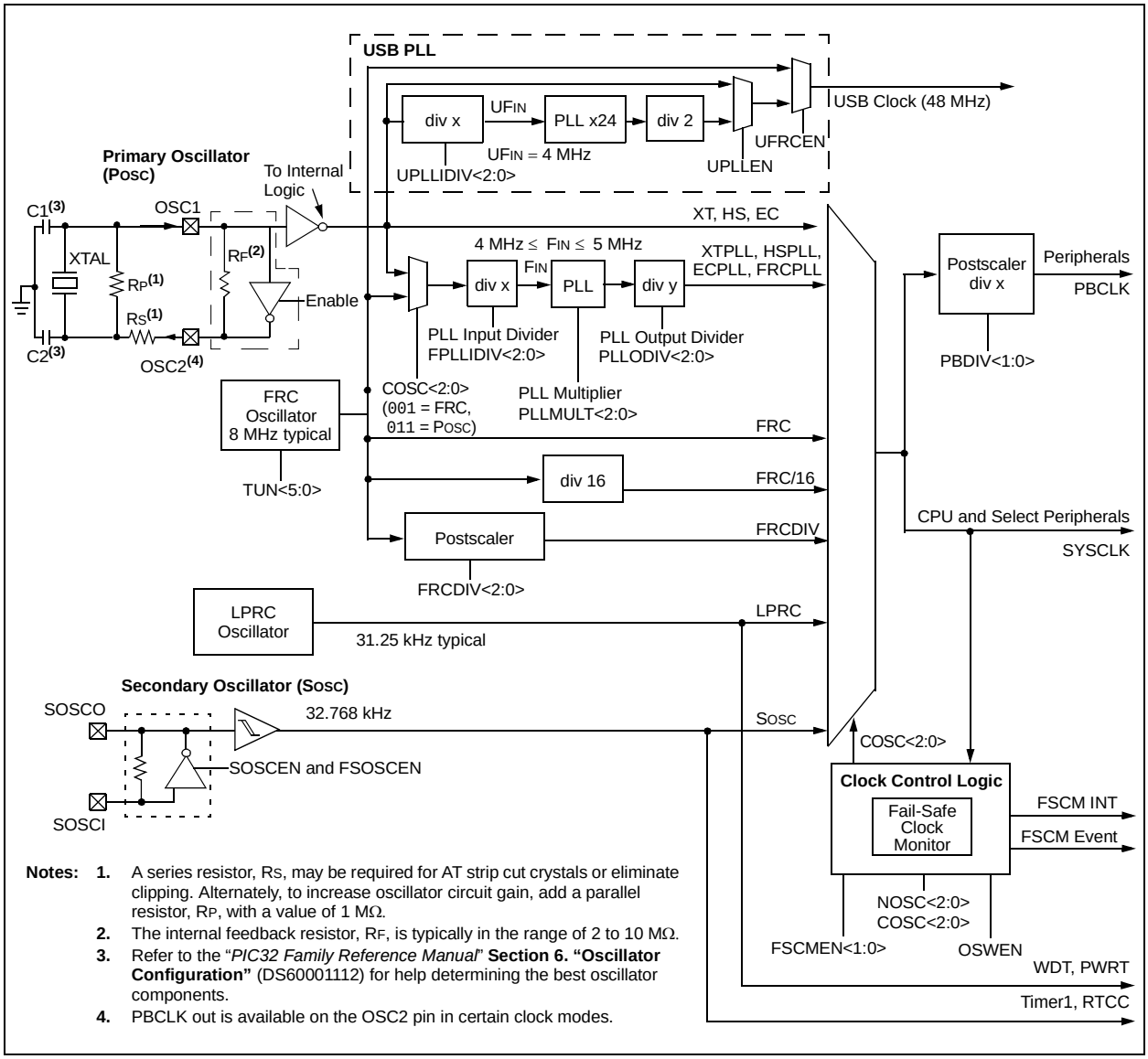
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Oscillator module has the following features:

- A total of four external and internal oscillator options as clock sources
- On-chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

Figure 8-1shows the Oscillator module block diagram.

FIGURE 8-1: OSCILLATOR BLOCK DIAGRAM



Notes:
1. A series resistor, RS, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP, with a value of 1 MΩ.
2. The internal feedback resistor, RF, is typically in the range of 2 to 10 MΩ.
3. Refer to the "*PIC32 Family Reference Manual*" **Section 6. "Oscillator Configuration"** (DS60001112) for help determining the best oscillator components.
4. PBCLK out is available on the OSC2 pin in certain clock modes.

REGISTER 9-3: CHETAG: CACHE TAG REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	LTAGBOOT	—	—	—	—	—	—	—
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	LTAG<19:12>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	LTAG<11:4>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-0	R/W-0	R/W-1	U-0
	LTAG<3:0>				LVALID	LLOCK	LTYPE	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **LTAGBOOT:** Line Tag Address Boot bit
- 1 = The line is in the 0x1D000000 (physical) area of memory
- 0 = The line is in the 0x1FC00000 (physical) area of memory

bit 30-24 **Unimplemented:** Write '0'; ignore read

bit 23-4 **LTAG<19:0>:** Line Tag Address bits

LTAG<19:0> bits are compared against physical address to determine a hit. Because its address range and position of PFM in kernel space and user space, the LTAG PFM address is identical for virtual addresses, (system) physical addresses, and PFM physical addresses.

bit 3 **LVALID:** Line Valid bit
- 1 = The line is valid and is compared to the physical address for hit detection
- 0 = The line is not valid and is not compared to the physical address for hit detection

bit 2 **LLOCK:** Line Lock bit
- 1 = The line is locked and will not be replaced
- 0 = The line is not locked and can be replaced

bit 1 **LTYPE:** Line Type bit
- 1 = The line caches instruction words
- 0 = The line caches data words

bit 0 **Unimplemented:** Write '0'; ignore read

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
34D0	DCH5DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
34E0	DCH6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
34F0	DCH6ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3500	DCH6INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3510	DCH6SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3520	DCH6DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
3530	DCH6SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3540	DCH6DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3550	DCH6SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3560	DCH6DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3570	DCH6CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3580	DCH6CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3590	DCH6DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
35A0	DCH7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
35B0	DCH7ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
35C0	DCH7INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
35D0	DCH7SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
35E0	DCH7DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

REGISTER 10-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.
Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.
Note: This must be the physical address of the destination.

REGISTER 11-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit
1 = Next token command to be executed at low-speed
0 = Next token command to be executed at full-speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 11-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	—	—	SAMC<4:0>(1)				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
	ADCS<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = Clock derived from FRC
0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits(2)
11111111 = TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD
•
•
•
00000001 = TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD
00000000 = TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
2: This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

REGISTER 24-3: CiINT: CAN INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIF	WAKIF	CERRIF	SERRIF(1)	RBOVIF	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 30 **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 29 **CERRIE:** CAN Bus Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 28 **SERRIE:** System Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 27 **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 26-20 **Unimplemented:** Read as '0'

bit 19 **MODIE:** Mode Change Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 18 **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 17 **RBIE:** Receive Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 16 **TBIE:** Transmit Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 15 **IVRIF:** Invalid Message Received Interrupt Flag bit
1 = An invalid messages interrupt has occurred
0 = An invalid message interrupt has not occurred

Note 1: This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CiCON<15>).

REGISTER 24-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)

bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)

bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)

bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)

bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)

bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning

bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter

bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 24-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **FIFOIP<31:0>:** FIFOn Interrupt Pending bits

1 = One or more enabled FIFO interrupts are pending

0 = No FIFO interrupts are pending

REGISTER 24-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)

bit 9 **TXHALFIF:** FIFO Transmit FIFO Half Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is ≤ half full
0 = FIFO is > half full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 8 **TXEMPTYIF:** Transmit FIFO Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is empty
0 = FIFO is not empty, at least 1 message queued to be transmitted
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **RXOVFLIF:** Receive FIFO Overflow Interrupt Flag bit
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = Overflow event has occurred
0 = No overflow event occured

bit 2 **RXFULLIF:** Receive FIFO Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is full
0 = FIFO is not full

bit 1 **RXHALFIF:** Receive FIFO Half Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **RXNEMPTYIF:** Receive Buffer Not Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is not empty, has at least 1 message
0 = FIFO is empty

Note 1: This bit is read-only and reflects the status of the FIFO.

REGISTER 25-5: ETHHT0: ETHERNET CONTROLLER HASH TABLE 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **HT<31:0>:** Hash Table Bytes 0-3 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 25-6: ETHHT1: ETHERNET CONTROLLER HASH TABLE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<39:32>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **HT<63:32>:** Hash Table Bytes 4-7 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 25-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

bit 6 **PKTPEND:** Packet Pending Interrupt bit

1 = RX packet pending in memory
0 = RX packet is not pending in memory

This bit is set when the BUFCNT counter has a value other than '0'. It is cleared by either a Reset or by writing the BUFCDEC bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 5 **RXACT:** Receive Activity Interrupt bit

1 = RX packet data was successfully received
0 = No interrupt pending

This bit is set whenever RX packet data is stored in the RXBM FIFO. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONE:** Transmit Done Interrupt bit

1 = TX packet was successfully sent
0 = No interrupt pending

This bit is set when the currently transmitted TX packet completes transmission, and the Transmit Status Vector is loaded into the first descriptor used for the packet. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 2 **TXABORT:** Transmit Abort Condition Interrupt bit

1 = TX abort condition occurred on the last TX packet
0 = No interrupt pending

This bit is set when the MAC aborts the transmission of a TX packet for one of the following reasons:

- Jumbo TX packet abort
- Underrun abort
- Excessive defer abort
- Late collision abort
- Excessive collisions abort

This bit is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 1 **RXBUFNA:** Receive Buffer Not Available Interrupt bit

1 = RX Buffer Descriptor Not Available condition has occurred
0 = No interrupt pending

This bit is set by a RX Buffer Descriptor Overrun condition. It is cleared by either a Reset or a CPU write of a '1' to the CLR register.

bit 0 **RXOVFLW:** Receive FIFO Over Flow Error bit

1 = RX FIFO Overflow Error condition has occurred
0 = No interrupt pending

RXOVFLW is set by the RXBM Logic for an RX FIFO Overflow condition. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

Note:	It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-38: EMAC1SA1: ETHERNET CONTROLLER MAC STATION ADDRESS 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR4<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR3<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR4<7:0>:** Station Address Octet 4 bits
These bits hold the fourth transmitted octet of the station address.

bit 7-0 **STNADDR3<7:0>:** Station Address Octet 3 bits
These bits hold the third transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

NOTES:

TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Parameter No.	**Typical(2)**	**Max.**	**Units**	**Conditions**		
Idle Current (IIDLE)(1) for PIC32MX534/564/664/764 Family Devices						
DC30a	1.5	5	mA	-40ºC, +25ºC, +85ºC	—	4 MHz
DC30c	3.5	6		+105ºC		
DC31a	7	11		-40ºC, +25ºC, +85ºC	—	25 MHz **(Note 3)**
DC32a	13	20	mA	-40ºC, +25ºC, +85ºC	—	60 MHz **(Note 3)**
DC33a	17	25	mA	-40ºC, +25ºC, +85ºC	—	80 MHz
DC33c	20	27		+105ºC		
DC34c	—	40	µA	-40°C	2.3V	LPRC (31 kHz) **(Note 3)**
DC34d		75		+25°C		
DC34e		800		+85°C		
DC34f		1000		+105ºC		
DC35c	30	—	µA	-40°C	3.3V	
DC35d	55			+25°C		
DC35e	230			+85°C		
DC35f	800			+105ºC		
DC36c	—	43	µA	-40°C	3.6V	
DC36d		106		+25°C		
DC36e		800		+85°C		
DC36f		1000		+105ºC		

Note 1: The test conditions for IIDLE current measurements are as follows:

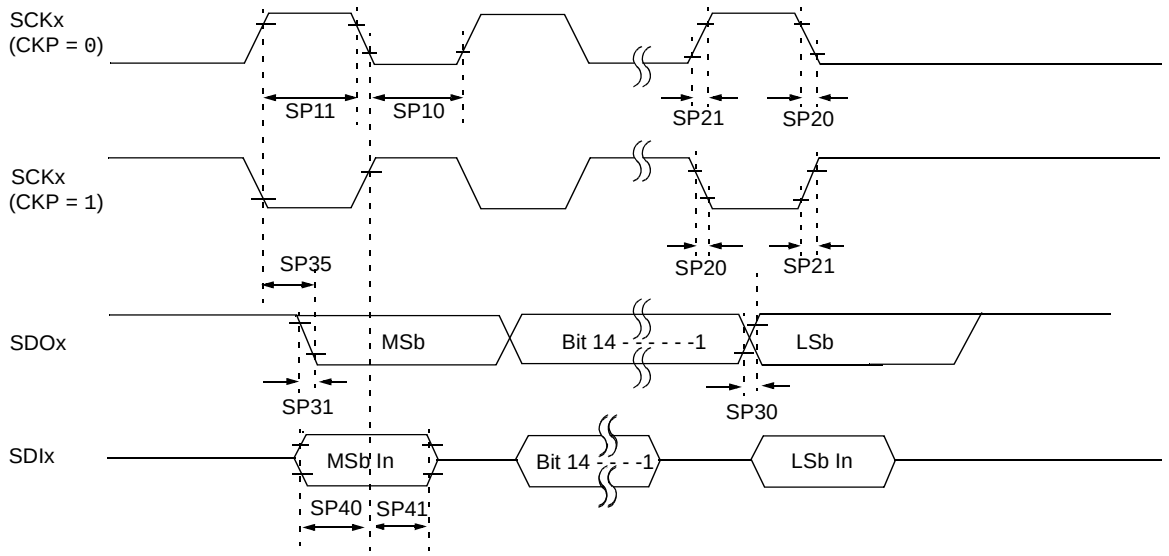
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

4: All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

FIGURE 32-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

TABLE 32-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(3)	TSCK/2	—	—	ns	—
SP11	TscH	SCKx Output High Time(3)	TSCK/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

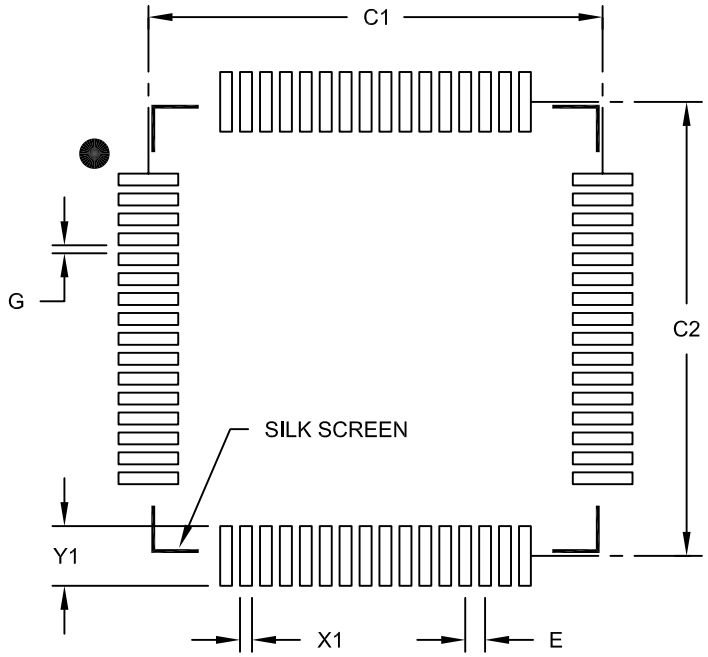
2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

Revision E (July 2010)

Minor corrections were incorporated throughout the document.

Revision F (December 2010)

The revision includes the following global update:

VCAP/VDDCORE has been changed to: VCAP/VCORE

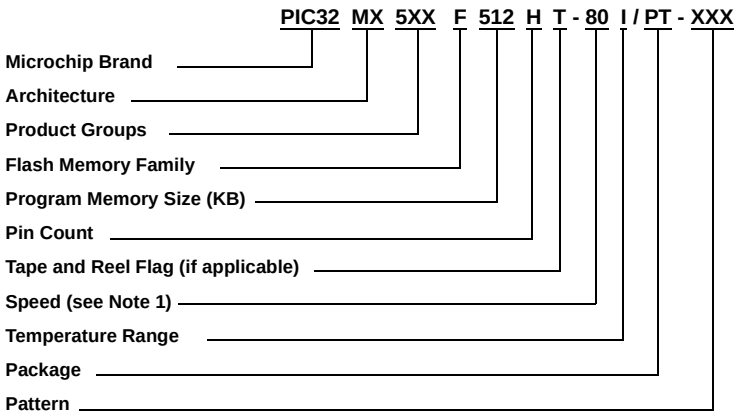
Other major changes are referenced by their respective chapter/section in Table B-4:

TABLE B-4: SECTION UPDATES

Section Name	Update Description
High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers	Removed the following Analog Feature: FV tolerant input pins (digital pins only) Updated the term LIN 1.2 support as LIN support for the peripheral feature: Six UART modules with: RS-232, RS-485, and LIN support
1.0 "Device Overview"	Updated the value of 64-pin QFN/TQFP pin number for the following pin names: PMA0, PMA1 and ECRSDV
4.0 "Memory Organization"	The following register map tables were updated: • Table 4-2: - Changed bits 24/8 to I2C5BIF in IFS1 - Changed bits 24/8-24/10 to SRIPL<2:0> in INTSTAT - Changed bits 25/9/-24/8 to U5IS<1:0> in IPC12 - Added note 2 • Table 4-3 through Table 4-7: - Changed bits 24/8-24/10 to SRIPL<2:0> in INTSTAT - Changed bits 25/9-24/8 to U5IS<1:0> in IPC12 • Table 4-3: - Changed bits 24/8 to I2C5BIF in IFS1 - Added note 2 • Table 4-4: - Changed bits 24/8 to I2C5BIF in IFS1 - Changed bits 24/8 to I2C5BIE in IEC1 - Added note 2 references • Table 4-5: - Changed bits 24/8 to I2C5BIF in IFS1 - Changed bits 24/8 to I2C5BIE in IEC1 - Added note 2 references • Table 4-6: - Changed bit 24/8 to I2C5BIF in IFS1 - Updated the bit value of bit 24/8 as I2C5BIE for the IEC1 register. - Added note 2 • Table 4-7: - Changed bit 25/9 to I2C5SIF in IFS1 - Changed bit 24/8 as I2C5BIF in IFS1 - Changed bit 25/9 as I2C5SIE in IEC1 - Changed bit 24/8 as I2C5BIE in IEC1 - Added note 2 references • Added note 2 to Table 4-8 • Updated the All Resets values for the following registers in Table 4-11: I2C3CON, I2C4CON, I2C5CON and I2C1CON. • Updated the All Resets values for the I2C2CON register in Table 4-12

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Example:

PIC32MX575F256H-80I/PT:
General purpose PIC32,
32-bit RISC MCU,
256 KB program memory,
64-pin, Industrial temperature,
TQFP package.

Flash Memory Family

Architecture	MX = 32-bit RISC MCU core
Product Groups	5XX = General purpose microcontroller family 6XX = General purpose microcontroller family 7XX = General purpose microcontroller family
Flash Memory Family	F = Flash program memory
Program Memory Size	**64 = 64K** **128 = 128K** 256 = 256K 512 = 512K
Pin Count	H = 64-pin L = 100-pin, 121-pin, 124-pin
Speed (see **Note 1**)	Blank or 80 = 80 MHz
Temperature Range	I = -40°C to +85°C (Industrial) V = -40°C to +105°C (V-Temp)
Package	PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) PF = 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack) MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat) BG = 121-Lead (10x10x1.1 mm) TFBGA (Plastic Thin Profile Ball Grid Array) TL = 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample

Note 1: This option is not available for PIC32MX534/564/664/764 devices.