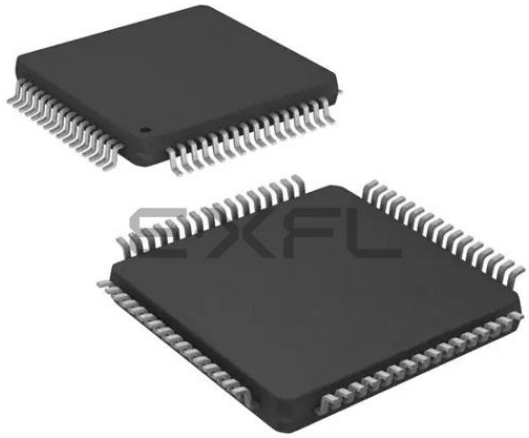

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx564f064h-v-pt

TABLE 5: PIN NAMES FOR 64-PIN USB AND ETHERNET DEVICES

64-PIN QFN(2) AND TQFP (TOP VIEW)

PIC32MX664F064H
PIC32MX664F128H
PIC32MX675F256H
PIC32MX675F512H
PIC32MX695F512H

64 1

QFN(2)

64 1

TQFP

Pin #	Full Pin Name	Pin #	Full Pin Name
1	ETXEN/PMD5/RE5	33	USBID/RF3
2	ETXD0/PMD6/RE6	34	VBUS
3	ETXD1/PMD7/RE7	35	VUSB3V3
4	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	36	D-/RG3
5	SDA4/SDI2/U3RX/PMA4/CN9/RG7	37	D+/RG2
6	SCL4/SDO2/U3TX/PMA3/CN10/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	SS2/U6RX/U3CTS/PMA2/CN11/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RTCC/AERXD1/ETXD3/IC1/INT1/RD8
11	AN5/C1IN+/VBUSON/CN7/RB5	43	AERXD0/ETXD2/SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9
12	AN4/C1IN-/CN6/RB4	44	ECOL/AECRSDV/SCL1/IC3/PMCS2/PMA15/INT3/RD10
13	AN3/C2IN+/CN5/RB3	45	ECRS/AEREFCLK/IC4/PMCS1/PMA14/INT4/RD11
14	AN2/C2IN-/CN4/RB2	46	OC1/INT0/RD0
15	PGEC1/AN1/VREF-/CVREF-/CN3/RB1	47	SOSCI/CN1/RC13
16	PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0	48	SOSCO/T1CK/CN0/RC14
17	PGEC2/AN6/OCFA/RB6	49	EMDIO/AEMDIO/SCK3/U4TX/U1RTS/OC2/RD1
18	PGED2/AN7/RB7	50	SDA3/SDI3/U1RX/OC3/RD2
19	AVDD	51	SCL3/SDO3/U1TX/OC4/RD3
20	AVSS	52	OC5/IC5/PMWR/CN13/RD4
21	AN8/SS4/U5RX/U2CTS/C1OUT/RB8	53	PMRD/CN14/RD5
22	AN9/C2OUT/PMA7/RB9	54	AETXEN/ETXERR/CN15/RD6
23	TMS/AN10/CVREFOUT/PMA13/RB10	55	ETXCLK/AERXERR/CN16/RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	AETXD1/ERXD3/RF0
27	TCK/AN12/PMA11/RB12	59	AETXD0/ERXD2/RF1
28	TDI/AN13/PMA10/RB13	60	ERXD1/PMD0/RE0
29	AN14/SCK4/U5TX/U2RTSU2RTS/PMALH/PMA1/RB14	61	ERXD0/PMD1/RE1
30	AN15/EMDC/AEMDC/OCFB/PMALL/PMA0/CN12/RB15	62	ERXDV/ECRSDV/PMD2/RE2
31	SDA5/SDI4/U2RX/PMA9/CN17/RF4	63	ERXCLK/EREFCLK/PMD3/RE3
32	SCL5/SDO4/U2TX/PMA8/CN18/RF5	64	ERXERR/PMD4/RE4

Note 1: Shaded pins are 5V tolerant.
2: The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
CN0	48	74	B11	B40	I	ST	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
CN1	47	73	C10	A47	I	ST	
CN2	16	25	K2	B14	I	ST	
CN3	15	24	K1	A15	I	ST	
CN4	14	23	J2	B13	I	ST	
CN5	13	22	J1	A13	I	ST	
CN6	12	21	H2	B11	I	ST	
CN7	11	20	H1	A12	I	ST	
CN8	4	10	E3	A7	I	ST	
CN9	5	11	F4	B6	I	ST	
CN10	6	12	F2	A8	I	ST	
CN11	8	14	F3	A9	I	ST	
CN12	30	44	L8	A29	I	ST	
CN13	52	81	C8	B44	I	ST	
CN14	53	82	B8	A55	I	ST	
CN15	54	83	D7	B45	I	ST	
CN16	55	84	C7	A56	I	ST	
CN17	31	49	L10	B27	I	ST	
CN18	32	50	L11	A32	I	ST	
CN19	—	80	D8	A54	I	ST	
CN20	—	47	L9	B26	I	ST	
CN21	—	48	K9	A31	I	ST	
IC1	42	68	E9	B37	I	ST	Capture Inputs 1-5
IC2	43	69	E10	A45	I	ST	
IC3	44	70	D11	B38	I	ST	
IC4	45	71	C11	A46	I	ST	
IC5	52	79	A9	A60	I	ST	
OCFA	17	26	L1	A20	I	ST	Output Compare Fault A Input
OC1	46	72	D9	B39	O	—	Output Compare Output 1
OC2	49	76	A11	A52	O	—	Output Compare Output 2
OC3	50	77	A10	B42	O	—	Output Compare Output 3
OC4	51	78	B9	A53	O	—	Output Compare Output 4
OC5	52	81	C8	B44	O	—	Output Compare Output 5
OCFB	30	44	L8	A29	I	ST	Output Compare Fault B Input
INT0	46	72	D9	B39	I	ST	External Interrupt 0
INT1	42	18	G1	A11	I	ST	External Interrupt 1
INT2	43	19	G2	B10	I	ST	External Interrupt 2
INT3	44	66	E11	B36	I	ST	External Interrupt 3
INT4	45	67	E8	A44	I	ST	External Interrupt 4

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

2: See **25.0 "Ethernet Controller"** for more information.

REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-1	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1
	—	BMX WSDRM	—	—	—	BMXARB<2:0>		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **BMXERRIXI:** Enable Bus Error from IXI bit
1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus
0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus

bit 19 **BMXERRICD:** Enable Bus Error from ICD Debug Unit bit
1 = Enable bus error exceptions for unmapped address accesses initiated from ICD
0 = Disable bus error exceptions for unmapped address accesses initiated from ICD

bit 18 **BMXERRDMA:** Bus Error from DMA bit
1 = Enable bus error exceptions for unmapped address accesses initiated from DMA
0 = Disable bus error exceptions for unmapped address accesses initiated from DMA

bit 17 **BMXERRDS:** Bus Error from CPU Data Access bit (disabled in Debug mode)
1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access
0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access

bit 16 **BMXERRIS:** Bus Error from CPU Instruction Access bit (disabled in Debug mode)
1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access
0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **BMXWSDRM:** CPU Instruction or Data Access from Data RAM Wait State bit
1 = Data RAM accesses from CPU have one wait state for address setup
0 = Data RAM accesses from CPU have zero wait states for address setup

bit 5-3 **Unimplemented:** Read as '0'

bit 2-0 **BMXARB<2:0>:** Bus Matrix Arbitration Mode bits
111 = Reserved (using these Configuration modes will produce undefined behavior)
•
•
•
011 = Reserved (using these Configuration modes will produce undefined behavior)
010 = Arbitration Mode 2
001 = Arbitration Mode 1 (default)
000 = Arbitration Mode 0

REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDUDBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDUDBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUDBA<15:10>:** DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 **BMXDUDBA<9:0>:** DRM User Data Base Address Read-Only bits

Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

TABLE 7-3: INTERRUPT REGISTER MAP FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H AND PIC32MX695F512H DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	—	—	USBIF	FCEIF	DMA7IF(2)	DMA6IF(2)	DMA5IF(2)	DMA4IF(2)	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	—	—	—	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1050	IFS2	31:16	—	—			—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	—	—	USBIE	FCEIE	DMA7IE(2)	DMA6IE(2)	DMA5IE(2)	DMA4IE(2)	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	—	—	—	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: These bits are not available on PIC32MX664 devices.

3: This register does not have associated CLR, SET, and INV registers.

TABLE 7-4: INTERRUPT REGISTER MAP FOR PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	CAN2IF(2)	CAN1IF	USBIF	FCEIF	DMA7IF(2)	DMA6IF(2)	DMA5IF(2)	DMA4IF(2)	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	—	—	—	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	CAN2IE(2)	CAN1IE	USBIE	FCEIE	DMA7IE(2)	DMA6IE(2)	DMA5IE(2)	DMA4IE(2)	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	—	—	—	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This bit is unimplemented on PIC32MX764F128H device.

3: This register does not have associated CLR, SET, and INV registers.

REGISTER 11-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS
	BTSEF	BMXEF	DMAEF(1)	BTOEF(2)	DFN8EF	CRC16EF	CRC5EF(4) / EOFEF(3,5)	PIDEF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit
- 1 = Packet is rejected due to bit stuff error
- 0 = Packet is accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
- 1 = Invalid base address of the BDT, or the address of an individual buffer pointed to by a BDT entry
- 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit(1)
- 1 = USB DMA error condition detected
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit(2)
- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit
- 1 = Data field received is not an integral number of bytes
- 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
- 1 = Data packet is rejected due to CRC16 error
- 0 = Data packet is accepted

bit 1 **CRC5EF:** CRC5 Host Error Flag bit(4)
- 1 = Token packet is rejected due to CRC5 error
- 0 = Token packet is accepted

EOFEF: EOF Error Flag bit(3,5)
- 1 = EOF error condition is detected
- 0 = No EOF error condition

bit 0 **PIDEF:** PID Check Failure Flag bit
- 1 = PID check is failed
- 0 = PID check is passed

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

REGISTER 11-11: U1CON: USB CONTROL REGISTER (CONTINUED)

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Reset all Even/Odd buffer pointers to the Even buffer descriptor banks
0 = Even/Odd buffer pointers are not reset

bit 0 **USBEN:** USB Module Enable bit(4)
1 = USB module and supporting circuitry is enabled
0 = USB module and supporting circuitry is disabled

SOFEN: SOF Enable bit(5)
1 = SOF token is sent every 1 ms
0 = SOF token is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).

2: All host control logic is reset any time that the value of this bit is toggled.

3: Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.

4: Device mode.

5: Host mode.

TABLE 12-5: PORTD REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0FFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 12-6: PORTD REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LAT15	LAT14	LAT13	LAT12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

20.1 Control Registers

TABLE 20-1: UART1 THROUGH UART6 REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	U1MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6010	U1STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6040	U1BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BRG<15:0>																0000
6200	U4MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	—	—	—	—	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6210	U4STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6220	U4TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6230	U4RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6240	U4BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BRG<15:0>																0000
6400	U3MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6410	U3STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6420	U3TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6430	U3RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6440	U3BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BRG<15:0>																0000
6600	U6MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	—	—	—	—	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6610	U6STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

22.1 Control Registers

TABLE 22-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	—	—	—	RTSECSEL	RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0220	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx00
0240	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 24-2: CAN2 REGISTER SUMMARY FOR PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C100	C2FLTCON4	31:16	FLTEN19	MSEL19<1:0>		FSEL19<4:0>					FLTEN18	MSEL18<1:0>		FSEL18<4:0>					0000
		15:0	FLTEN17	MSEL17<1:0>		FSEL17<4:0>					FLTEN16	MSEL16<1:0>		FSEL16<4:0:					0000
C110	C2FLTCON5	31:16	FLTEN23	MSEL23<1:0>		FSEL23<4:0>					FLTEN22	MSEL22<1:0>		FSEL22<4:0>					0000
		15:0	FLTEN21	MSEL21<1:0>		FSEL21<4:0>					FLTEN20	MSEL20<1:0>		FSEL20<4:0>					0000
C120	C2FLTCON6	31:16	FLTEN27	MSEL27<1:0>		FSEL27<4:0>					FLTEN26	MSEL26<1:0>		FSEL26<4:0>					0000
		15:0	FLTEN25	MSEL25<1:0>		FSEL25<4:0>					FLTEN24	MSEL24<1:0>		FSEL24<4:0>					0000
C130	C2FLTCON7	31:16	FLTEN31	MSEL31<1:0>		FSEL31<4:0>					FLTEN30	MSEL30<1:0>		FSEL30<4:0>					0000
		15:0	FLTEN29	MSEL29<1:0>		FSEL29<4:0>					FLTEN28	MSEL28<1:0>		FSEL28<4:0>					0000
C140	C2RXFn (n = 0-31)	31:16	SID<10:0>											-—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
C340	C2FIFOBA	31:16	C2FIFOBA<31:0>																0000
		15:0																	0000
C350	C2FIFOCONn (n = 0-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
C360	C2FIFOINTn (n = 0-31)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
C370	C2FIFOUAn (n = 0-31)	31:16	C2FIFOUA<31:0>																0000
		15:0																	0000
C380	C2FIFOCIn (n = 0-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C2FIFOCI<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 24-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 24-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)

bit 9 **TXHALFIF:** FIFO Transmit FIFO Half Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is ≤ half full
0 = FIFO is > half full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 8 **TXEMPTYIF:** Transmit FIFO Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is empty
0 = FIFO is not empty, at least 1 message queued to be transmitted
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **RXOVFLIF:** Receive FIFO Overflow Interrupt Flag bit
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = Overflow event has occurred
0 = No overflow event occured

bit 2 **RXFULLIF:** Receive FIFO Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is full
0 = FIFO is not full

bit 1 **RXHALFIF:** Receive FIFO Half Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **RXNEMPTYIF:** Receive Buffer Not Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is not empty, has at least 1 message
0 = FIFO is empty

Note 1: This bit is read-only and reflects the status of the FIFO.

REGISTER 25-22: ETHALGNERR: ETHERNET CONTROLLER ALIGNMENT ERRORS STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **ALGNERRCNT<15:0>:** Alignment Error Count bits

Increment count for frames with alignment errors. Note that an alignment error is a frame that has an FCS error and the frame length in bits is not an integral multiple of 8 bits (a.k.a., dribble nibble)

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

REGISTER 25-29: EMAC1SUPP: ETHERNET CONTROLLER MAC PHY SUPPORT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
	—	—	—	—	RESETRMII(1)	—	—	SPEEDRMII(1)
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMII:** Reset RMII Logic bit(1)
1 = Reset the MAC RMII module
0 = Normal operation.

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPEEDRMII:** RMII Speed bit(1)
This bit configures the Reduced MII logic for the current operating speed.
1 = RMII is running at 100 Mbps
0 = RMII is running at 10 Mbps

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is only used for the RMII module.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

FIGURE 32-26: PARALLEL MASTER PORT READ TIMING DIAGRAM

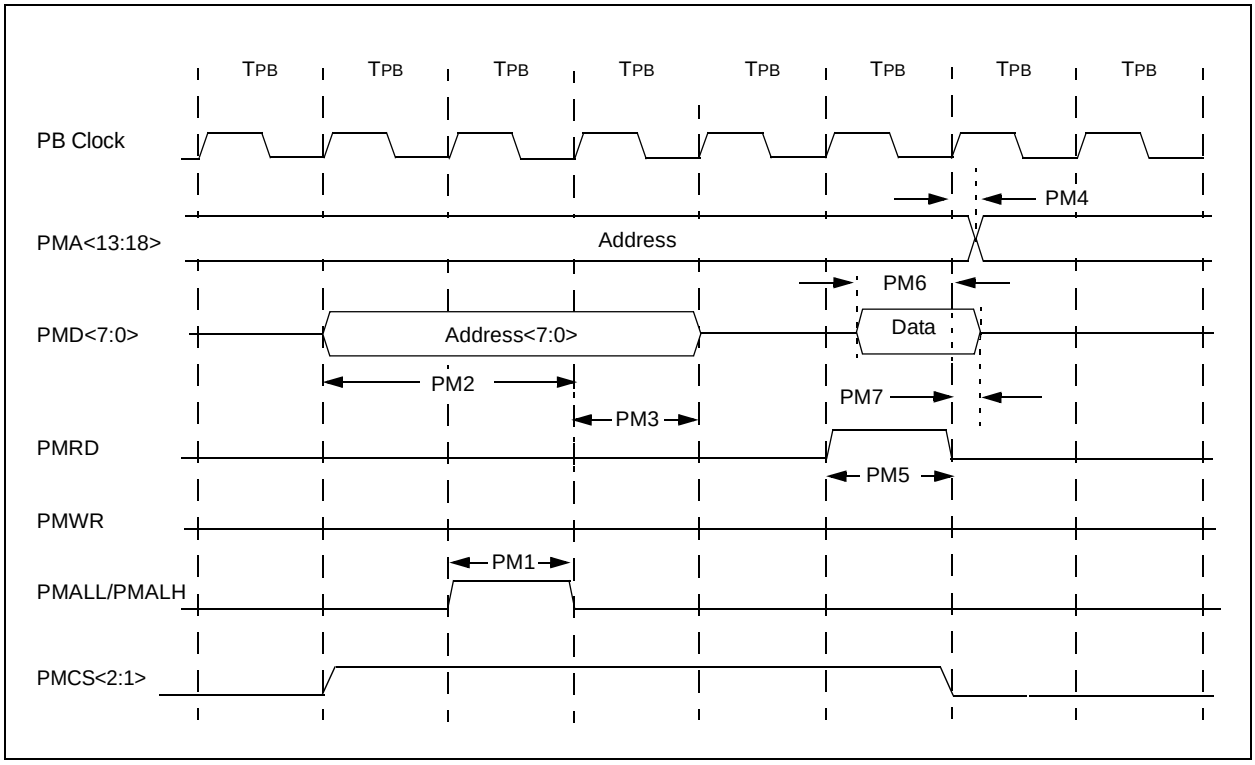


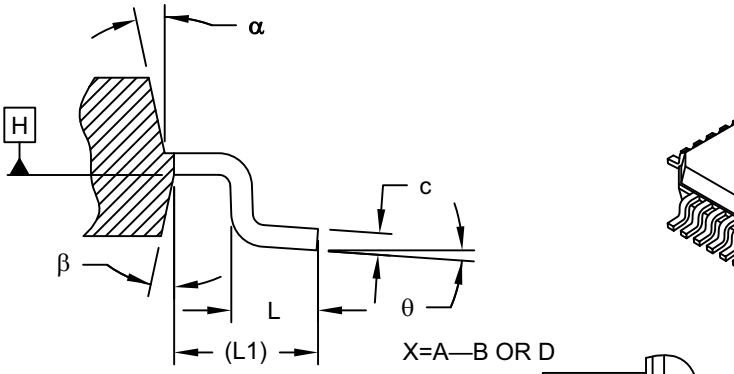
TABLE 32-40: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	—
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)	—	2 TPB	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	1 TPBCLK	—	—	ns	PMP PBCLK

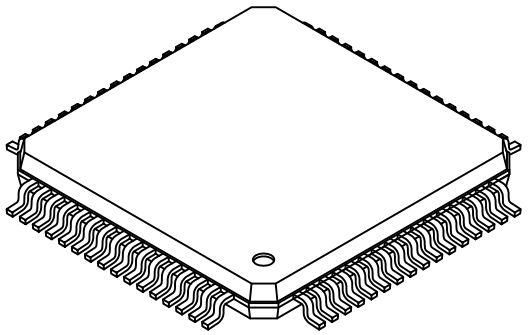
Note 1: These parameters are characterized, but not tested in manufacturing.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

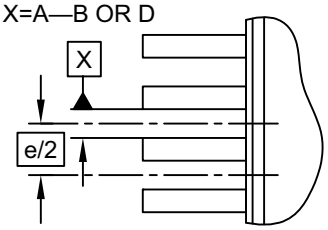
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



X=A—B OR D



DETAIL 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

Revision D (May 2010)

The revision includes the following updates, as described in Table B-3:

TABLE B-3: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"	Updated the initial Flash memory range to 64K. Updated the initial SRAM memory range to 16K. Added the following devices (see Table 1, Table 2, Table 3 and the Pin Diagrams): • PIC32MX534F064H • PIC32MX564F064H • PIC32MX664F064H • PIC32MX564F128H • PIC32MX664F128H • PIC32MX764F128H • PIC32MX534F064L • PIC32MX564F064L • PIC32MX664F064L • PIC32MX564F128L • PIC32MX664F128L • PIC32MX764F128L
4.0 "Memory Organization"	Added new Memory Maps (Figure 4-1, Figure 4-2 and Figure 4-3). The bit named I2CSIF was changed to I2C1SIF and the bit named I2CBIF was changed to I2C1BIF in the Interrupt Register Map tables (Table 4-2, Table 4-3, Table 4-4, Table 4-5, Table 4-6 and Table 4-7) Added the following devices to the Interrupt Register Map (Table 4-2): • PIC32MX534F064H • PIC32MX564F064H • PIC32MX564F128H Added the following devices to the Interrupt Register Map (Table 4-3): • PIC32MX664F064H • PIC32MX664F128H Added the following device to the Interrupt Register Map (Table 4-4): • PIC32MX764F128H Added the following devices to the Interrupt Register Map (Table 4-5): • PIC32MX534F064L • PIC32MX564F064L • PIC32MX564F128L Added the following devices to the Interrupt Register Map (Table 4-6): • PIC32MX664F064L • PIC32MX664F128L Added the following device to the Interrupt Register Map (Table 4-7): • PIC32MX764F128L

TABLE B-4: SECTION UPDATES (CONTINUED)

Section Name	Update Description
4.0 "Memory Organization" (Continued)	• Table 4-13: - Changed register U4RG to U1BRG - Changed register U5RG to U3BRG - Changed register U6RG to U2BRG • Table 4-14: - Updated the All Resets values for the following registers: SPI3STAT, SPI2STAT and SPI4STAT • Table 4-15: Updated the All Resets values for the SPI1STAT register • Table 4-17: Added note 2 • Table 4-19: Added note 2 • Table 4-20: Updated the All Resets values for the CM1CON and CM2CON registers • Table 4-21: - Updated the All Resets values as 0000 for the CVRCON register - Updated note 2 • Table 4-38: Updated the All Resets values for the PMSTAT register • Table 4-40: Updated the All Resets values for the CHECON and CHETAG registers • Table 4-42: Updated the bit value of bit 29/13 as '—' for the DEVCFG3 register • Table 4-44: - Updated the note references in the entire table - Changed existing note 1 to note 4 - Added notes 1, 2 and 3 - Changed bits 23/7 in U1PWRC to UACTPND - Changed register U1DDR to U1ADDR - Changed register U4DTP1 to U1BDTP1 - Changed register U4DTP2 to U1BDTP2 - Changed register U4DTP3 to U1BDTP3 • Table 4-45: - Updated the All Resets values for the C1CON and C1VEC registers - Changed bits 30/14 in C1CON to FRZ - Changed bits 27/11 in C1CON to CANBUSY - Changed bits 22/6-16/0 in C1VEC to ICODE<6:0> - Changed bits 22/6-16/0 in C1TREC to RERRCNT<7:0> - Changed bits 31/15-24/8 in C1TREC to TERRCNT<7:0> • Table 4-46: - Updated the All Resets values for the C2CON and C2VEC registers - Changed bits 30/14 in C1CON to FRZ - Changed bits 27/11 in C1CON to CANBUSY - Changed bits 22/6-16/0 in C1VEC register to ICODE<6:0> - Changed bits 22/6-16/0 in C1TREC register to RERRCNT<7:0> - Changed bits 31/15-24/8 in C1TREC to TERRCNT<7:0>