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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx564f064ht-v-mr

PIC32MX5XX/6XX/7XX

TABLE 7: PIN NAMES FOR 100-PIN USB AND CAN DEVICES

100-PIN TQFP (TOP VIEW)			
PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX575F512L PIC32MX575F256L		100 1	
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RG15	36	VSS
2	VDD	37	VDD
3	PMD5/RE5	38	TCK/RA1
4	PMD6/RE6	39	AC1TX/SCK4/U5TX/U2RTS/RF13
5	PMD7/RE7	40	AC1RX/SS4/U5RX/U2CTS/RF12
6	T2CK/RC1	41	AN12/PMA11/RB12
7	T3CK/RC2	42	AN13/PMA10/RB13
8	T4CK/RC3	43	AN14/PMALH/PMA1/RB14
9	T5CK/SDI1/RC4	44	AN15/OCFB/PMALL/PMA0/CN12/RB15
10	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	45	VSS
11	SDA4/SDI2/U3RX/PMA4/CN9/RG7	46	VDD
12	SCL4/SDO2/U3TX/PMA3/CN10/RG8	47	SS3/U4RX/U1CTS/CN20/RD14
13	MCLR	48	SCK3/U4TX/U1RTS/CN21/RD15
14	SS2/U6RX/U3CTS/PMA2/CN11/RG9	49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
15	VSS	50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
16	VDD	51	USBID/RF3
17	TMS/RA0	52	SDA3/SDI3/U1RX/RF2
18	INT1/RE8	53	SCL3/SDO3/U1TX/RF8
19	INT2/RE9	54	VBUS
20	AN5/C1IN+/VBUSON/CN7/RB5	55	VUSB3V3
21	AN4/C1IN-/CN6/RB4	56	D-/RG3
22	AN3/C2IN+/CN5/RB3	57	D+/RG2
23	AN2/C2IN-/CN4/RB2	58	SCL2/RA2
24	PGEC1/AN1/CN3/RB1	59	SDA2/RA3
25	PGED1/AN0/CN2/RB0	60	TDI/RA4
26	PGEC2/AN6/OCFA/RB6	61	TDO/RA5
27	PGED2/AN7/RB7	62	VDD
28	VREF-/CVREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	SCL1/INT3/RA14
32	AN8/C1OUT/RB8	67	SDA1/INT4/RA15
33	AN9/C2OUT/RB9	68	RTCC/IC1/RD8
34	AN10/CVREFOUT/PMA13/RB10	69	SS1/IC2/RD9
35	AN11/PMA12/RB11	70	SCK1/IC3/PMCS2/PMA15/RD10

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 13: PIN NAMES FOR 124-PIN USB, ETHERNET, AND CAN DEVICES

124-PIN VTLA (BOTTOM VIEW) ^(2,3)		A17		B13		B29		A34	
								Conductive Thermal Pad	
PIC32MX675F512L PIC32MX695F512L PIC32MX795F512L				B1		B56		B41	
		A1						A51	
		Polarity Indicator				A68			
Package Bump #	Full Pin Name	Package Bump #	Full Pin Name	Package Bump #	Full Pin Name	Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
A1	No Connect (NC)	A38	D-/RG3	A38	D-/RG3	A38	D-/RG3	A38	D-/RG3
A2	AERXERR/RG15	A39	SCL2/RA2	A39	SCL2/RA2	A39	SCL2/RA2	A39	SCL2/RA2
A3	Vss	A40	TDI/RA4	A40	TDI/RA4	A40	TDI/RA4	A40	TDI/RA4
A4	PMD6/RE6	A41	VDD	A41	VDD	A41	VDD	A41	VDD
A5	T2CK/RC1	A42	OSC2/CLKO/RC15	A42	OSC2/CLKO/RC15	A42	OSC2/CLKO/RC15	A42	OSC2/CLKO/RC15
A6	T4CK/AC2RX ⁽¹⁾ /RC3	A43	Vss	A43	Vss	A43	Vss	A43	Vss
A7	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6	A44	AETXEN/SDA1/INT4/RA15	A44	AETXEN/SDA1/INT4/RA15	A44	AETXEN/SDA1/INT4/RA15	A44	AETXEN/SDA1/INT4/RA15
A8	ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8	A45	SS1/IC2/RD9	A45	SS1/IC2/RD9	A45	SS1/IC2/RD9	A45	SS1/IC2/RD9
A9	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9	A46	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	A46	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	A46	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	A46	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11
A10	VDD	A47	SOSCI/CN1/RC13	A47	SOSCI/CN1/RC13	A47	SOSCI/CN1/RC13	A47	SOSCI/CN1/RC13
A11	AERXD0/INT1/RE8	A48	VDD	A48	VDD	A48	VDD	A48	VDD
A12	AN5/C1IN+VBUSON/CN7/RB5	A49	No Connect (NC)	A49	No Connect (NC)	A49	No Connect (NC)	A49	No Connect (NC)
A13	AN3/C2IN+/CN5/RB3	A50	No Connect (NC)	A50	No Connect (NC)	A50	No Connect (NC)	A50	No Connect (NC)
A14	VDD	A51	No Connect (NC)	A51	No Connect (NC)	A51	No Connect (NC)	A51	No Connect (NC)
A15	PGEC1/AN1/CN3/RB1	A52	OC2/RD1	A52	OC2/RD1	A52	OC2/RD1	A52	OC2/RD1
A16	No Connect (NC)	A53	OC4/RD3	A53	OC4/RD3	A53	OC4/RD3	A53	OC4/RD3
A17	No Connect (NC)	A54	ETXD3/PMD13/CN19/RD13	A54	ETXD3/PMD13/CN19/RD13	A54	ETXD3/PMD13/CN19/RD13	A54	ETXD3/PMD13/CN19/RD13
A18	No Connect (NC)	A55	PMRD/CN14/RD5	A55	PMRD/CN14/RD5	A55	PMRD/CN14/RD5	A55	PMRD/CN14/RD5
A19	No Connect (NC)	A56	ETXCLK/PMD15/CN16/RD7	A56	ETXCLK/PMD15/CN16/RD7	A56	ETXCLK/PMD15/CN16/RD7	A56	ETXCLK/PMD15/CN16/RD7
A20	PGEC2/AN6/OCFA/RB6	A57	No Connect (NC)	A57	No Connect (NC)	A57	No Connect (NC)	A57	No Connect (NC)
A21	VREF-/CVREF-/AERXD2/PMA7/RA9	A58	No Connect (NC)	A58	No Connect (NC)	A58	No Connect (NC)	A58	No Connect (NC)
A22	AVDD	A59	VDD	A59	VDD	A59	VDD	A59	VDD
A23	AN8/C1OUT/RB8	A60	C1TX/ETXD0/PMD10/RF1	A60	C1TX/ETXD0/PMD10/RF1	A60	C1TX/ETXD0/PMD10/RF1	A60	C1TX/ETXD0/PMD10/RF1
A24	AN10/CVREFOUT/PMA13/RB10	A61	C2RX ⁽¹⁾ /PMD8/RG0	A61	C2RX ⁽¹⁾ /PMD8/RG0	A61	C2RX ⁽¹⁾ /PMD8/RG0	A61	C2RX ⁽¹⁾ /PMD8/RG0
A25	Vss	A62	TRD3/RA7	A62	TRD3/RA7	A62	TRD3/RA7	A62	TRD3/RA7
A26	TCK/RA1	A63	Vss	A63	Vss	A63	Vss	A63	Vss
A27	AC1RX ⁽¹⁾ /SS4/U5RX/U2CTS/RF12	A64	PMD1/RE1	A64	PMD1/RE1	A64	PMD1/RE1	A64	PMD1/RE1
A28	AN13/ERXD1/AECOL/PMA10/RB13	A65	TRD1/RG12	A65	TRD1/RG12	A65	TRD1/RG12	A65	TRD1/RG12
A29	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15	A66	PMD2/RE2	A66	PMD2/RE2	A66	PMD2/RE2	A66	PMD2/RE2
A30	VDD	A67	PMD4/RE4	A67	PMD4/RE4	A67	PMD4/RE4	A67	PMD4/RE4
A31	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15	A68	No Connect (NC)	A68	No Connect (NC)	A68	No Connect (NC)	A68	No Connect (NC)
A32	SCL5/SDO4/U2TX/PMA8/CN18/RF5	B1	VDD	B1	VDD	B1	VDD	B1	VDD
A33	No Connect (NC)	B2	PMD5/RE5	B2	PMD5/RE5	B2	PMD5/RE5	B2	PMD5/RE5
A34	No Connect (NC)	B3	PMD7/RE7	B3	PMD7/RE7	B3	PMD7/RE7	B3	PMD7/RE7
A35	USBID/RF3	B4	T3CK/AC2TX ⁽¹⁾ /RC2	B4	T3CK/AC2TX ⁽¹⁾ /RC2	B4	T3CK/AC2TX ⁽¹⁾ /RC2	B4	T3CK/AC2TX ⁽¹⁾ /RC2
A36	SDA3/SDI3/U1RX/RF2	B5	T5CK/SDI1/RC4	B5	T5CK/SDI1/RC4	B5	T5CK/SDI1/RC4	B5	T5CK/SDI1/RC4
A37	VBus	B6	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7	B6	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7	B6	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7	B6	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7
B7	MCLR	B32	SDA2/RA3	B32	SDA2/RA3	B32	SDA2/RA3	B32	SDA2/RA3

- Note**
- 1: This pin is only available on PIC32MX795F512L devices.
 - 2: Shaded package bumps are 5V tolerant.
 - 3: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

1.0 DEVICE OVERVIEW

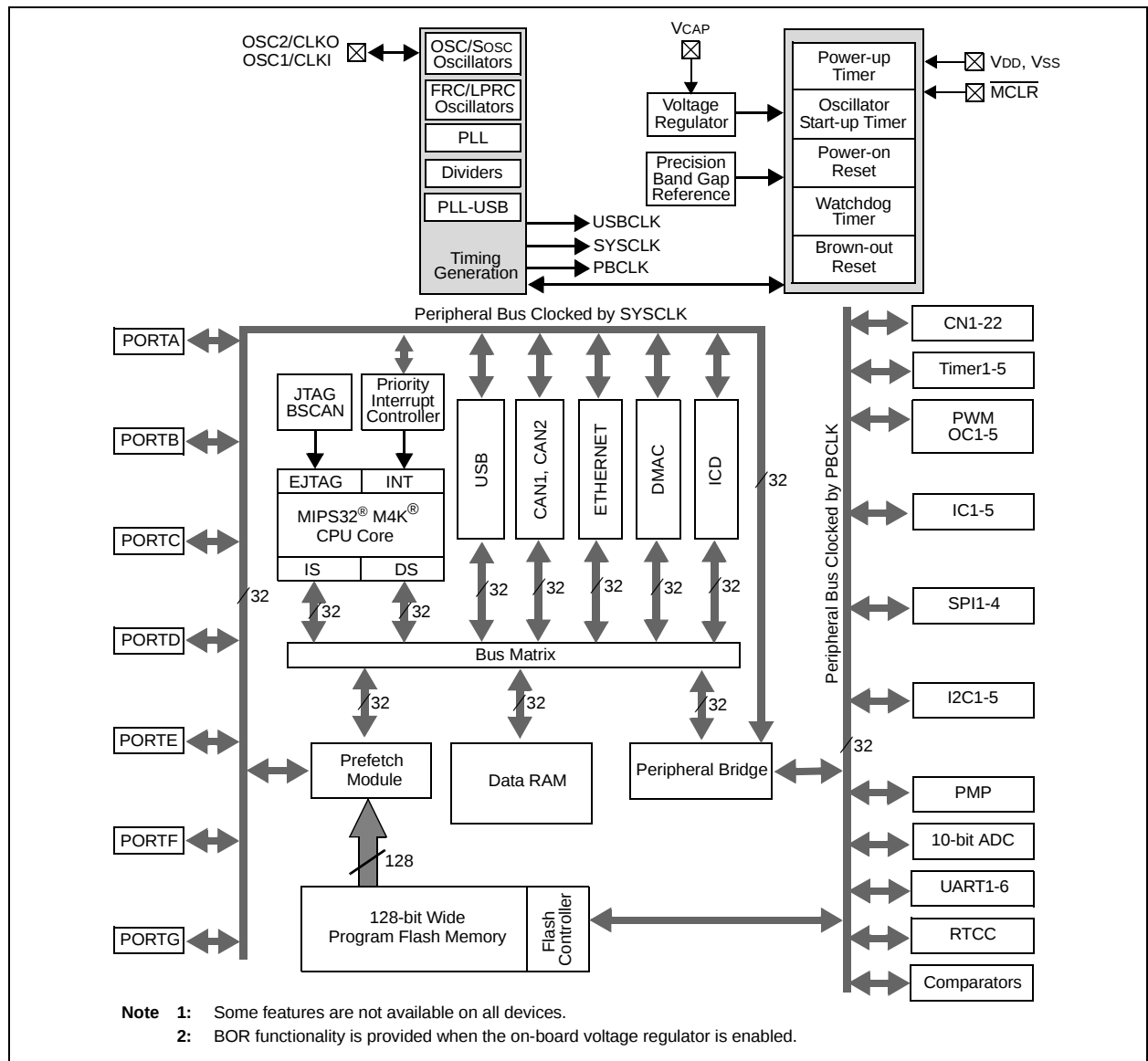
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX5XX/6XX/7XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX5XX/6XX/7XX family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM^(1,2)



PIC32MX5XX/6XX/7XX

REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0
7:0	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VEEC<5:0> ⁽¹⁾								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **RIPL<2:0>:** Requested Priority Level bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits⁽¹⁾

11111-00000 = The interrupt vector that is presented to the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single-vector mode.

REGISTER 7-3: TPTMR: TEMPORAL PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TPTMR<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TPTMR<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TPTMR<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TPTMR<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **TPTMR<31:0>:** Temporal Proximity Timer Reload bits

Used by the Temporal Proximity Timer as a reload value when the Temporal Proximity timer is triggered by an interrupt event.

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REGISTER 9-12: CHEPFABT: PREFETCH CACHE ABORT STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEPFABT<31:0>**: Prefab Abort Count bits

Incremented each time an automatic prefetch cache is aborted due to a non-sequential instruction fetch, load or store.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
35F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

REGISTER 10-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	ON ⁽¹⁾	—	—	SUSPEND	DMABUSY	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit⁽¹⁾

1 = DMA module is enabled

0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit

1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus

0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit

1 = DMA module is active

0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 14-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

bit 3	T32: 32-Bit Timer Mode Select bit ⁽²⁾ 1 = Odd numbered and even numbered timers form a 32-bit timer 0 = Odd numbered and even numbered timers form a separate 16-bit timer
bit 2	Unimplemented: Read as '0'
bit 1	TCS: Timer Clock Source Select bit ⁽³⁾ 1 = External clock from TxCK pin 0 = Internal peripheral clock
bit 0	Unimplemented: Read as '0'

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit is only available on even numbered timers (Timer2 and Timer4).
- 3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, and Timer5). All timer functions are set through the even numbered timers.
- 4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 18-1: SPIxCON: SPI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 FRMEN	R/W-0 FRMSYNC	R/W-0 FRMPOL	R/W-0 MSEN	R/W-0 FRMSYPW	FRMCNT<2:0>		
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 SPIFE	R/W-0 ENHBUF ⁽²⁾
15:8	R/W-0 ON ⁽¹⁾	U-0 —	R/W-0 SIDL	R/W-0 DISSDO	R/W-0 MODE32	R/W-0 MODE16	R/W-0 SMP	R/W-0 CKE ⁽³⁾
7:0	R/W-0 SSEN	R/W-0 CKP	R/W-0 MSTEN	U-0 —	R/W-0 STXISEL<1:0>	R/W-0 SRXISEL<1:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (only Framed SPI mode)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)
- bit 29 **FRMPOL:** Frame Sync Polarity bit (only Framed SPI mode)
1 = Frame pulse is active-high
0 = Frame pulse is active-low
- bit 28 **MSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The $\overline{SS}$ pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.
- bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in Framed Sync mode.
111 = Reserved
110 = Reserved
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character
- bit 23-18 **Unimplemented:** Read as '0'
- bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (only Framed SPI mode)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF:** Enhanced Buffer Enable bit⁽²⁾
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit can only be written when the ON bit = 0.

3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

PIC32MX5XX/6XX/7XX

NOTES:

PIC32MX5XX/6XX/7XX

REGISTER 23-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CSSL<15:0>:** ADC Input Pin Scan Selection bits⁽¹⁾

1 = Select ANx for input scan

0 = Skip ANx for input scan

Note 1: CSSL = ANx, where 'x' = 0-15.

TABLE 24-2: CAN2 REGISTER SUMMARY FOR PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
C000	C2CON	31:16	—	—	—	—	ABAT	REQOP<2:0>				OPMOD<2:0>			CANCAP	—	—	—	—	0480	
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>				0000			
C010	C2CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>				0000	
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>				PRSEG<2:0>			SJW<1:0>		BRP<5:0>					0000		
C020	C2INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000		
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000		
C030	C2VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>						0040			
C040	C2TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000		
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000		
C050	C2FSTAT	31:16	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16	0000		
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000		
C060	C2RXOVF	31:16	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000		
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000		
C070	C2TMR	31:16	CANTS<15:0>																0000		
		15:0	CANTSPRE<15:0>															0000			
C080	C2RXM0	31:16	SID<10:0>											—	MIDE	—	EID<17:16>			xxxx	
		15:0	EID<15:0>																xxxx		
C0A0	C2RXM1	31:16	SID<10:0>											—	MIDE	—	EID<17:16>			xxxx	
		15:0	EID<15:0>																xxxx		
C0B0	C2RXM2	31:16	SID<10:0>											—	MIDE	—	EID<17:16>			xxxx	
		15:0	EID<15:0>																xxxx		
C0B0	C2RXM3	31:16	SID<10:0>											—	MIDE	—	EID<17:16>			xxxx	
		15:0	EID<15:0>																xxxx		
C0C0	C2FLTCON0	31:16	FLTEN3	MSEL3<1:0>				FSEL3<4:0>				FLTEN2	MSEL2<1:0>				FSEL2<4:0>				0000
		15:0	FLTEN1	MSEL1<1:0>				FSEL1<4:0>				FLTEN0	MSEL0<1:0>				FSEL0<4:0>				0000
C0D0	C2FLTCON1	31:16	FLTEN7	MSEL7<1:0>				FSEL7<4:0>				FLTEN6	MSEL6<1:0>				FSEL6<4:0>				0000
		15:0	FLTEN5	MSEL5<1:0>				FSEL5<4:0>				FLTEN4	MSEL4<1:0>				FSEL4<4:0>				0000
C0E0	C2FLTCON2	31:16	FLTEN11	MSEL11<1:0>				FSEL11<4:0>				FLTEN10	MSEL10<1:0>				FSEL10<4:0>				0000
		15:0	FLTEN9	MSEL9<1:0>				FSEL9<4:0>				FLTEN8	MSEL8<1:0>				FSEL8<4:0>				0000
C0F0	C2FLTCON3	31:16	FLTEN15	MSEL15<1:0>				FSEL15<4:0>				FLTEN14	MSEL14<1:0>				FSEL14<4:0>				0000
		15:0	FLTEN13	MSEL13<1:0>				FSEL13<4:0>				FLTEN12	MSEL12<1:0>				FSEL12<4:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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REGISTER 24-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN31	MSEL31<1:0>		FSEL31<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN30	MSEL30<1:0>		FSEL30<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN29	MSEL29<1:0>		FSEL29<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN28	MSEL28<1:0>		FSEL28<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **FLTEN31:** Filter 31 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 30-29 **MSEL31<1:0>:** Filter 31 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 28-24 **FSEL31<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0
- bit 23 **FLTEN30:** Filter 30 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 22-21 **MSEL30<1:0>:** Filter 30 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 20-16 **FSEL30<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

TABLE 25-5: ETHERNET CONTROLLER REGISTER SUMMARY FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX695F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX764F128H, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
90E0	ETHSTAT	31:16	—	—	—	—	—	—	—	—	BUFCNT<7:0>								0000
		15:0	—	—	—	—	—	—	—	—	BUSY	TXBUSY	RXBUSY	—	—	—	—	—	0000
9100	ETH RXOVFLOW	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVFLWCNT<15:0>																0000
9110	ETH FRMTXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMTXOKCNT<15:0>																0000
9120	ETH SCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SCOLFRMCNT<15:0>																0000
9130	ETH MCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MCOLFRMCNT<15:0>																0000
9140	ETH FRMRXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMRXOKCNT<15:0>																0000
9150	ETH FCSERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FCSERRCNT<15:0>																0000
9160	ETH ALGNERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALGNERRCNT<15:0>																0000
9200	EMAC1 CFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN	—	—	—	LOOPBACK	TXPAUSE	RXPAUSE	PASSALL	RXENABLE	800D
9210	EMAC1 CFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	EXCESS DFR	BP NOBKOFF	NOBKOFF	—	—	LONGPRE	PUREPRE	AUTOPAD	VLANPAD	PAD ENABLE	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX	4082
9220	EMAC1 IPGT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0012
9230	EMAC1 IPGR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	NB2BIPKTGP1<6:0>							—	NB2BIPKTGP2<6:0>							0C12
9240	EMAC1 CLRT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CWINDOW<5:0>							—	—	—	RETX<3:0>				370F
9250	EMAC1 MAXF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MACMAXF<15:0>																05EE

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2: Reset values default to the factory programmed value.

REGISTER 25-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

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REGISTER 29-1: DEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	R/P	r-1	r-1	r-1	R/P
	—	—	—	CP	—	—	—	BWP
23:16	r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
	—	—	—	—	PWP<7:4>			
15:8	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	PWP<3:0>				—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	r-1	R/P	R/P
	—	—	—	—	ICSEL	—	DEBUG<1:0>	

Legend:

R = Readable bit

-n = Value at POR

r = Reserved bit

W = Writable bit

'1' = Bit is set

P = Programmable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31 **Reserved:** Write '0'

bit 30-29 **Reserved:** Write '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.

1 = Protection is disabled

0 = Protection is enabled

bit 27-25 **Reserved:** Write '1'

bit 24 **BWP:** Boot Flash Write-Protect bit

Prevents boot Flash memory from being modified during code execution.

1 = Boot Flash is writable

0 = Boot Flash is not writable

bit 23-20 **Reserved:** Write '1'

bit 19-12 **PWP<7:0>:** Program Flash Write-Protect bits

Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the 1's complement of the number of write-protected program Flash memory pages.

11111111 = Disabled

11111110 = 0xBD00_0FFF

11111101 = 0xBD00_1FFF

11111100 = 0xBD00_2FFF

11111011 = 0xBD00_3FFF

11111010 = 0xBD00_4FFF

11111001 = 0xBD00_5FFF

11111000 = 0xBD00_6FFF

11110111 = 0xBD00_7FFF

11110110 = 0xBD00_8FFF

11110101 = 0xBD00_9FFF

11110100 = 0xBD00_AFFF

11110011 = 0xBD00_BFFF

11110010 = 0xBD00_CFFF

11110001 = 0xBD00_DFFF

11110000 = 0xBD00_EFFF

11101111 = 0xBD00_FFFF

.

.

.

01111111 = 0xBD07_FFFF

bit 11-4 **Reserved:** Write '1'

TABLE 32-38: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	Analog-to-Digital Clock Period ⁽²⁾	65	—	—	ns	See Table 32-37
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1 TAD	—	—	—	TSAMP must be ≥ 132 ns
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽³⁾	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from Analog-to-Digital Off to Analog-to-Digital On ⁽³⁾	—	—	2	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 32-26: PARALLEL MASTER PORT READ TIMING DIAGRAM

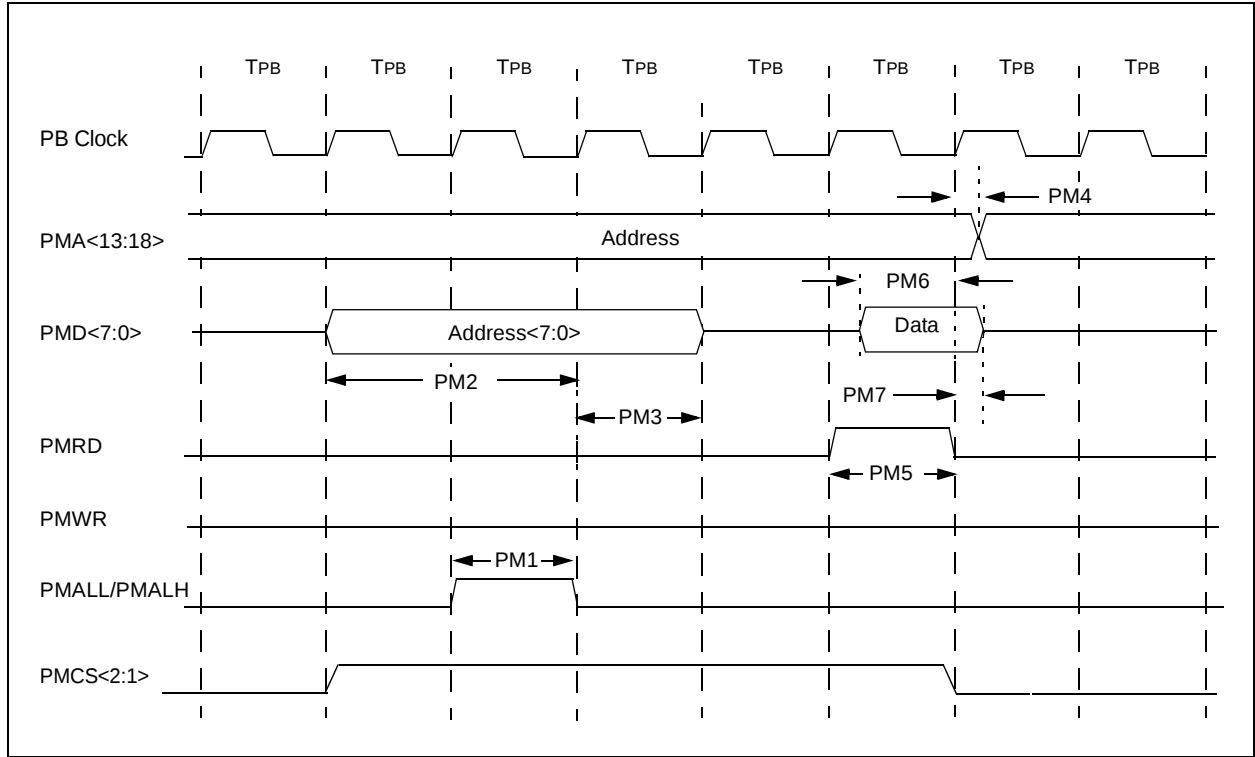


TABLE 32-40: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

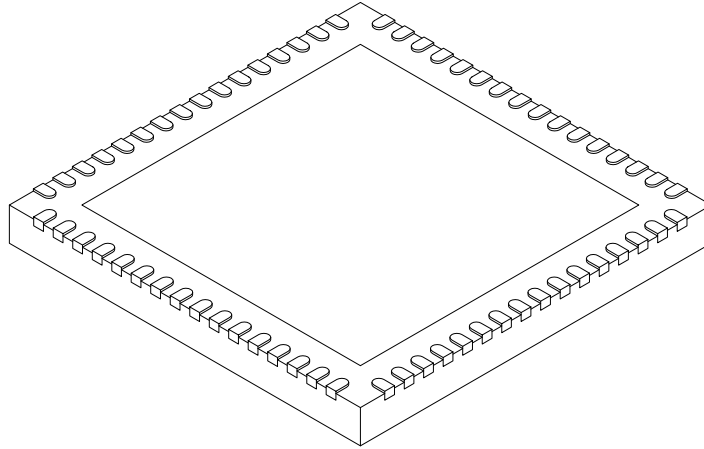
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	—
PM2	TADSU	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 TPB	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	1 TPBCLK	—	—	ns	PMP PBCLK

Note 1: These parameters are characterized, but not tested in manufacturing.

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64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		64		
Pitch	e		0.50 BSC		
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Width	E		9.00 BSC		
Exposed Pad Width	E2		7.05	7.15	7.50
Overall Length	D		9.00 BSC		
Exposed Pad Length	D2		7.05	7.15	7.50
Contact Width	b		0.18	0.25	0.30
Contact Length	L		0.30	0.40	0.50
Contact-to-Exposed Pad	K		0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

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PIC32MX5XX/6XX/7XX

APPENDIX B: REVISION HISTORY

Revision A (August 2009)

This is the initial released version of this document.

Revision B (November 2009)

The revision includes the following global update:

Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits.

Other major changes are referenced by their respective chapter/section in Table B-1.

TABLE B-1: MAJOR SECTION UPDATES

Section Name	Update Description
“High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers”	Added the following devices: - PIC32MX575F256L - PIC32MX695F512L - PIC32MX695F512H The 100-pin TQFP pin diagrams have been updated to reflect the current pin name locations (see the “Pin Diagrams” section). Added the 121-pin Ball Grid Array (XBGA) pin diagram. Updated Table 1: “PIC32 USB and CAN – Features” Added the following tables: - Table 4: “Pin Names: PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L and PIC32MX575F512L Devices” - Table 5: “Pin Names: PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L and PIC32MX695F512L Devices” - Table 6: “Pin Names: PIC32MX775F256L, PIC32MX775F512L and PIC32MX795F512L Devices” Updated the following pins as 5V tolerant: - 64-pin QFN: Pin 36 (D-/RG3) and Pin 37 (D+/RG2) - 64-pin TQFP: Pin 36 (D-/RG3) and Pin 37 (D+/RG2) - 100-pin TQFP: Pin 56 (D-/RG3) and Pin 57 (D+/RG2)
1.0 “Guidelines for Getting Started with 32-bit Microcontrollers”	Removed the last sentence of 1.3.1 “Internal Regulator Mode”. Removed Section 2.3.2 “External Regulator Mode”