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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx564f064lt-i-pt

PIC32MX5XX/6XX/7XX

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1	
Pin #	Full Pin Name	Pin #	Full Pin Name
J3	PGED2/AN7/RB7	K8	VDD
J4	AVDD	K9	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
J5	AN11/ERXERR/AETXERR/PMA12/RB11	K10	USBID/RF3
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2
J7	AN12/ERXD0/AECRS/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6
J8	No Connect (NC)	L2	VREF-/CVREF-/AERXD2/PMA7/RA9
J9	No Connect (NC)	L3	AVss
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10
K1	PGEC1/AN1/CN3/RB1	L6	SCK4/U5TX/U2RTS/RF13
K2	PGED1/AN0/CN2/RB0	L7	AN13/ERXD1/AECOL/PMA10/RB13
K3	VREF+/CVREF+/AERXD3/PMA6/RA10	L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
K4	AN8/C1OUT/RB8	L9	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
K6	SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14		

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
RA0	—	17	G3	B9	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	J6	A26	I/O	ST	
RA2	—	58	H11	A39	I/O	ST	
RA3	—	59	G10	B32	I/O	ST	
RA4	—	60	G11	A40	I/O	ST	
RA5	—	61	G9	B33	I/O	ST	
RA6	—	91	C5	B51	I/O	ST	
RA7	—	92	B5	A62	I/O	ST	
RA9	—	28	L2	A21	I/O	ST	
RA10	—	29	K3	B17	I/O	ST	
RA14	—	66	E11	B36	I/O	ST	
RA15	—	67	E8	A44	I/O	ST	
RB0	16	25	K2	B14	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	K1	A15	I/O	ST	
RB2	14	23	J2	B13	I/O	ST	
RB3	13	22	J1	A13	I/O	ST	
RB4	12	21	H2	B11	I/O	ST	
RB5	11	20	H1	A12	I/O	ST	
RB6	17	26	L1	A20	I/O	ST	
RB7	18	27	J3	B16	I/O	ST	
RB8	21	32	K4	A23	I/O	ST	
RB9	22	33	L4	B19	I/O	ST	
RB10	23	34	L5	A24	I/O	ST	
RB11	24	35	J5	B20	I/O	ST	
RB12	27	41	J7	B23	I/O	ST	
RB13	28	42	L7	A28	I/O	ST	
RB14	29	43	K7	B24	I/O	ST	
RB15	30	44	L8	A29	I/O	ST	
RC1	—	6	D1	A5	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	E4	B4	I/O	ST	
RC3	—	8	E2	A6	I/O	ST	
RC4	—	9	E1	B5	I/O	ST	
RC12	39	63	F9	B34	I/O	ST	
RC13	47	73	C10	A47	I/O	ST	
RC14	48	74	B11	B40	I/O	ST	
RC15	40	64	F11	A42	I/O	ST	

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input P = Power
O = Output I = Input

Note 1: Pin numbers are only provided for reference. See the “**Device Pin Tables**” section for device pin availability.

2: See **25.0 “Ethernet Controller”** for more information.

4.2 Control Registers

Register 4-1 through Register 4-8 are used for setting the RAM and Flash memory partitions for data and code.

TABLE 4-2: BUS MATRIX REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	BMXCON ⁽¹⁾	31:16	—	—	—	—	—	BMXCHEDMA	—	—	—	—	—	BMXERRIXI	BMXERRICD	BMXERRDMA	BMXERRDS	BMXERRIS	001F
		15:0	—	—	—	—	—	—	—	—	—	BMXWSDRM	—	—	—	BMXARB<2:0>			0041
2010	BMXDKPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDKPBA<15:0>																0000
2020	BMXDUDBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUDBA<15:0>																0000
2030	BMXDUPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUPBA<15:0>																0000
2040	BMXDRMSZ	31:16	BMXDRMSZ<31:0>																XXXX
		15:0																	XXXX
2050	BMXPUPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	BMXPUPBA<19:16>					0000
		15:0	BMXPUPBA<15:0>																0000
2060	BMXPFMSZ	31:16	BMXPFMSZ<31:0>																XXXX
		15:0																	XXXX
2070	BMXBOOTSZ	31:16	BMXBOOTSZ<31:0>																0000
		15:0																	3000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000	
3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000	
31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000	
31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000	
31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000	
31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHPDAT<7:0>										0000
31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000	
31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>										00FF
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00		
3200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000	
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000	
3210	DCH2SSA	31:16	CHSSA<31:0>																0000	
		15:0																	0000	
3220	DCH2DSA	31:16	CHDSA<31:0>																0000	
		15:0																	0000	
3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>																0000	
3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000	
3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000	
3260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000	
3270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000	
3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- 2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
35F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	—	CRCCH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>**: CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (reverse source byte order)

00 = No swapping (source byte order)

bit 27 **WBO**: CRC Write Byte Order Selection bit⁽¹⁾

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO**: CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (reflected)

0 = The LFSR CRC is calculated Most Significant bit first (not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>**: Polynomial Length bits⁽¹⁾

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN**: CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

TABLE 11-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
 - 2: This register does not have associated SET and INV registers.
 - 3: This register does not have associated CLR, SET and INV registers.
 - 4: Reset value for this bit is undefined.

REGISTER 11-4: U1OTGCON: USB OTG CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit

1 = D+ data line pull-up resistor is enabled

0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

1 = D- data line pull-up resistor is enabled

0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit

1 = D+ data line pull-down resistor is enabled

0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit

1 = D- data line pull-down resistor is enabled

0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit

1 = VBUS line is powered

0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Functionality Enable bit

1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control

0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 **VBUSCHG:** VBUS Charge Enable bit

1 = VBUS line is charged through a pull-up resistor

0 = VBUS line is not charged through a resistor

bit 0 **VBUSDIS:** Vbus Discharge Enable bit

1 = VBUS line is discharged through a pull-down resistor

0 = VBUS line is not discharged through a resistor

REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON ^(1,2)	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	—	SWDTPS<4:0>					WDTWINEN	WDTCLR

Legend:

y = Values set from Configuration bits on POR
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit^(1,2)

1 = Enables the WDT if it is not enabled by the device configuration
0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit

1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit

1 = Writing a '1' will clear the WDT
0 = Software cannot force this bit to a '0'

- Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
2: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX5XX/6XX/7XX

REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

bit 2-0 **ICM<2:0>**: Input Capture Mode Select bits

- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode – every sixteenth rising edge
- 100 = Prescaled Capture Event mode – every fourth rising edge
- 011 = Simple Capture Event mode – every rising edge
- 010 = Simple Capture Event mode – every falling edge
- 001 = Edge Detect mode – every edge (rising and falling)
- 000 = Input Capture module is disabled

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX5XX/6XX/7XX

NOTES:

PIC32MX5XX/6XX/7XX

REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>**: Alarm Repeat Counter Value bits⁽²⁾

11111111 = Alarm will trigger 256 times

•
•
•

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
- 2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
- 3:** This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is only reset on a Power-on Reset (POR).

24.0 CONTROLLER AREA NETWORK (CAN)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. “Controller Area Network (CAN)”** (DS60001154) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

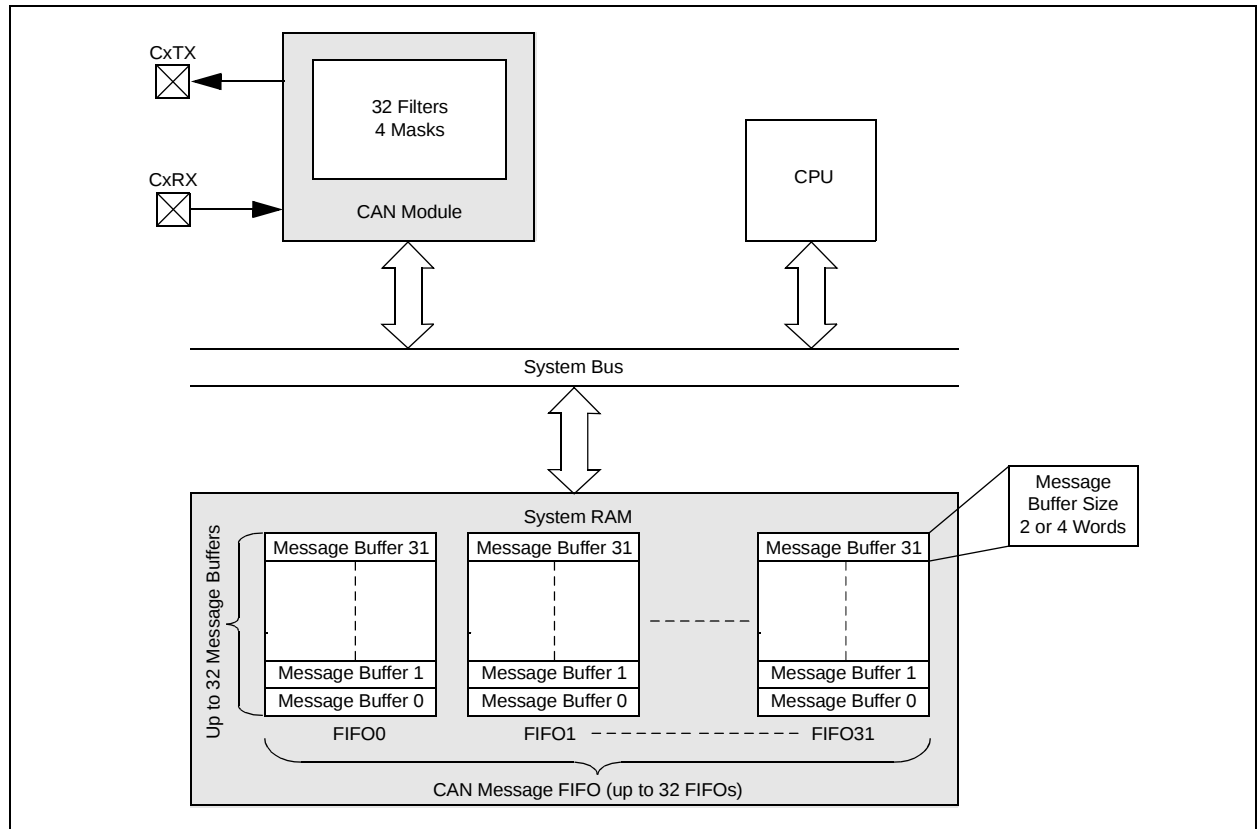
The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
 - Full CAN 2.0B compliance
 - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
 - 32 message FIFOs
 - Each FIFO can have up to 32 messages for a total of 1024 messages

- FIFO can be a transmit message FIFO or a receive message FIFO
- User-defined priority levels for message FIFOs used for transmission
- 32 acceptance filters for message filtering
- Four acceptance filter mask registers for message filtering
- Automatic response to remote transmit request
- DeviceNet™ addressing support
- Additional Features:
 - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
 - Low-power operating modes
 - CAN module is a bus master on the PIC32 system bus
 - Use of DMA is not required
 - Dedicated time-stamp timer
 - Dedicated DMA channels
 - Data-only Message Reception mode

Figure 24-1 illustrates the general structure of the CAN module.

FIGURE 24-1: PIC32 CAN MODULE BLOCK DIAGRAM



PIC32MX5XX/6XX/7XX

REGISTER 24-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 FLTEN3	R/W-0 MSEL3<1:0>	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	R/W-0 FLTEN2	R/W-0 MSEL2<1:0>	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	R/W-0 FLTEN1	R/W-0 MSEL1<1:0>	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	R/W-0 FLTEN0	R/W-0 MSEL0<1:0>	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0
- bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENN) bit is '0'.

REGISTER 24-17: C_iFLTCON7: CAN FILTER CONTROL REGISTER 7 (CONTINUED)

- bit 15 **FLTEN29**: Filter 29 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 14-13 **MSEL29<1:0>**: Filter 29 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL29<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 .
 .
 .
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN28**: Filter 28 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 6-5 **MSEL28<1:0>**: Filter 28 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL28<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 .
 .
 .
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTEN _n) bit is '0'.
--

26.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS60001110) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Comparator module contains two comparators that can be configured in a variety of ways.

Key features of the Comparator module include:

- Selectable inputs available include:
 - Analog inputs multiplexed with I/O pins
 - On-chip internal absolute voltage reference (IVREF)
 - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the Comparator module is illustrated in Figure 26-1.

FIGURE 26-1: COMPARATOR MODULE BLOCK DIAGRAM

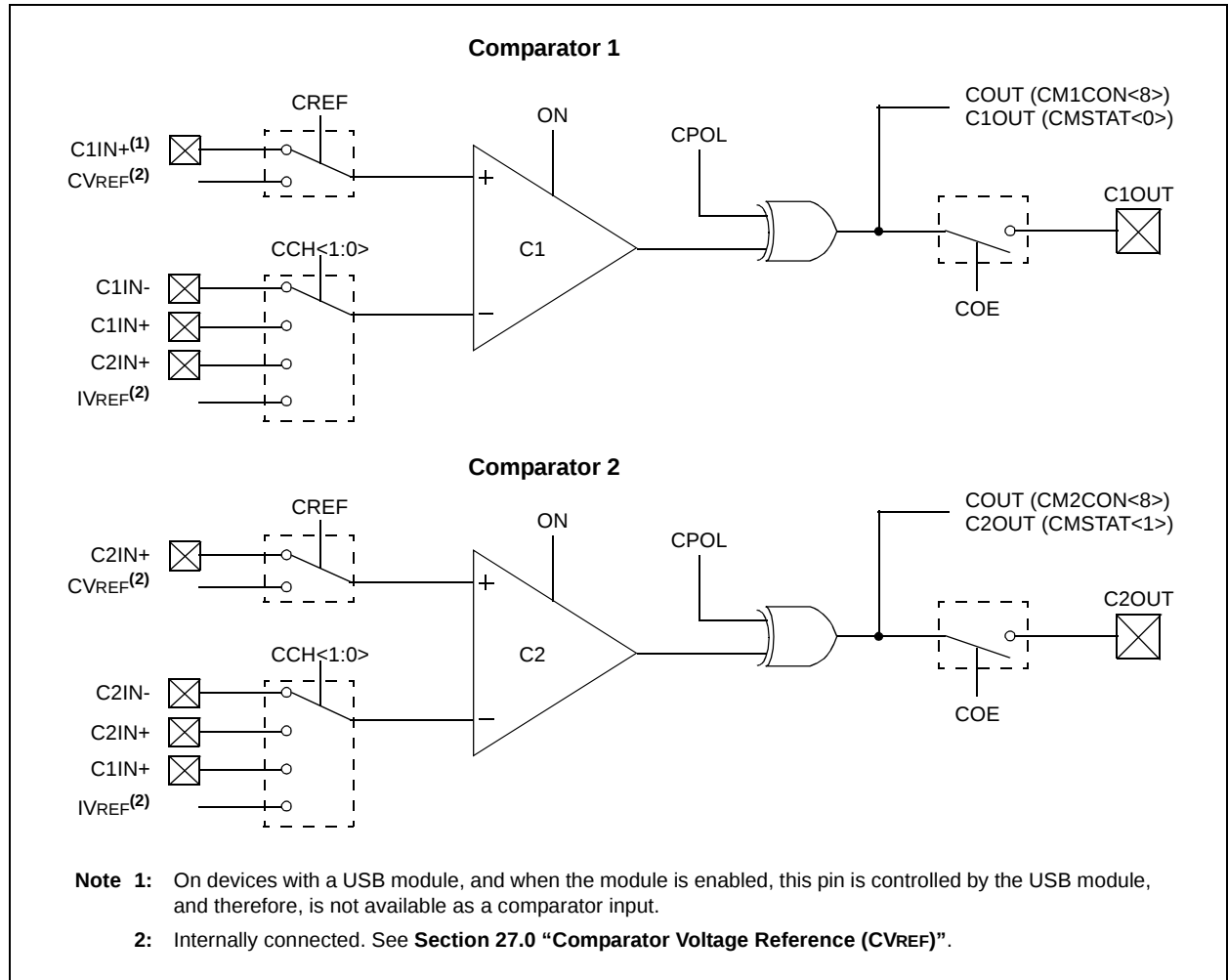


TABLE 29-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2FF0	DEVCFG3	31:16	FVBUSONIO	FUSBIDIO	—	—	—	FCANIO	FETHIO	FMIEN	—	—	—	—	—	FSRSSEL<2:0>		xxxx	
		15:0	USERID<15:0>															xxxx	
2FF4	DEVCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>		xxxx	
		15:0	UPLLEN	—	—	—	—	UPLLDIV<2:0>			—	FPLLMUL<2:0>			—	FPLLDIV<2:0>		xxxx	
2FF8	DEVCFG1	31:16	—	—	—	—	—	—	—	FWDTEN	—	—	WDTPS<4:0>			xxxx			
		15:0	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>		IESO	—	FSOSCEN	—	—	FNOSC<2:0>		xxxx	
2FFC	DEVCFG0	31:16	—	—	—	CP	—	—	—	BWP	—	—	—	—	PWP<7:4>			xxxx	
		15:0	PWP<3:0>				—	—	—	—	—	—	—	—	ICESEL	—	DEBUG<1:0>		xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 29-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
F200	DDPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	JTAGEN	TROEN	—	TDOEN
F220	DEVID	31:16	VER<3:0>				DEVID<27:16>											xxxx
		15:0	DEVID<15:0>															xxxx
F230	SYSKEY	31:16	SYSKEY<31:0>															0000
		15:0																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant. Refer to "PIC32MX5XX/6XX/7XX Family Silicon Errata and Data Sheet Clarification" (DS80000480) for more information.

FIGURE 32-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

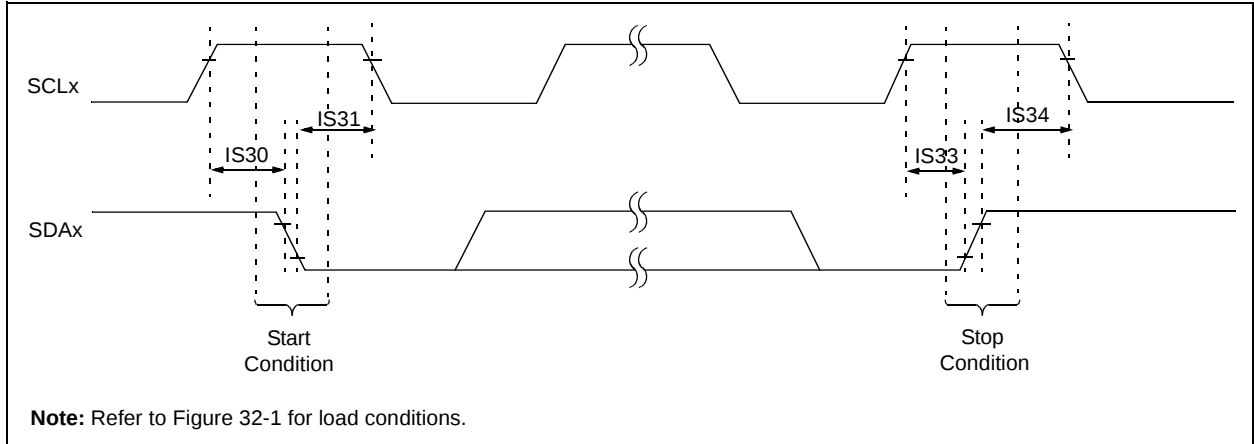
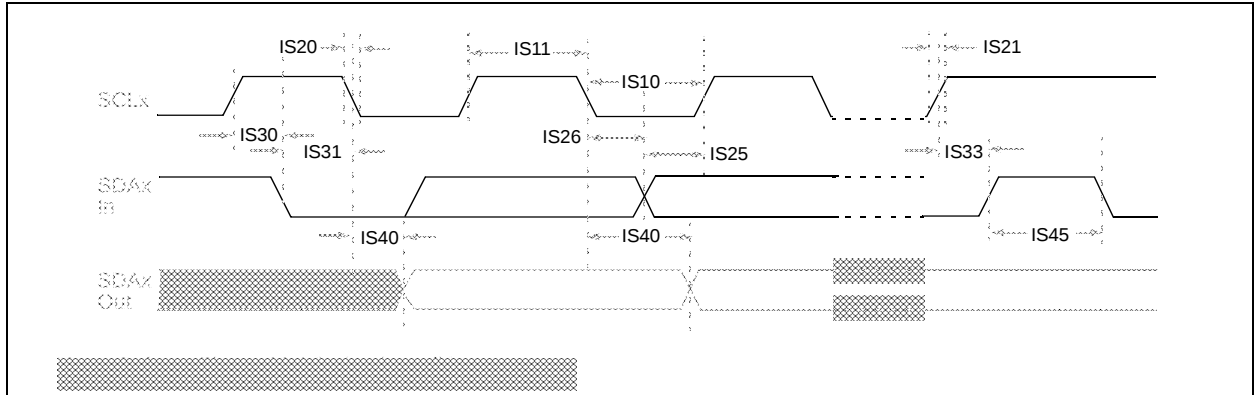


FIGURE 32-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



APPENDIX A: MIGRATING FROM PIC32MX3XX/4XX TO PIC32MX5XX/6XX/7XX DEVICES

This appendix provides an overview of considerations for migrating from PIC32MX3XX/4XX devices to the PIC32MX5XX/6XX/7XX family of devices. The code developed for the PIC32MX3XX/4XX devices can be ported to the PIC32MX5XX/6XX/7XX devices after making the appropriate changes outlined below.

A.1 DMA

PIC32MX5XX/6XX/7XX devices do not support stopping DMA transfers in Idle mode.

A.2 Interrupts

PIC32MX5XX/6XX/7XX devices have persistent interrupts for some of the peripheral modules. This means that the interrupt condition for these peripherals must be cleared before the interrupt flag can be cleared.

For example, to clear a UART receive interrupt, the user application must first read the UART Receive register to clear the interrupt condition and then clear the associated UxIF flag to clear the pending UART interrupt. In other words, the UxIF flag cannot be cleared by software until the UART Receive register is read.

Table A-1 outlines the peripherals and associated interrupts that are implemented differently on PIC32MX5XX/6XX/7XX versus PIC32MX3XX/4XX devices.

In addition, on the SPI module, the IRQ numbers for the receive done interrupts were changed from 25 to 24 and the transfer done interrupts were changed from 24 to 25.

TABLE A-1: PIC32MX3XX/4XX VERSUS PIC32MX5XX/6XX/7XX INTERRUPT IMPLEMENTATION DIFFERENCES

Module	Interrupt Implementation
Input Capture	To clear an interrupt source, read the Buffer Result (ICxBUF) register to obtain the number of capture results in the buffer that are below the interrupt threshold (specified by ICI<1:0> bits).
SPI	Receive and transmit interrupts are controlled by the SRXISEL<1:0> and STXISEL<1:0> bits, respectively. To clear an interrupt source, data must be written to, or read from, the SPIxBUF register to obtain the number of data to receive/transmit below the level specified by the SRXISEL<1:0> and STXISEL<1:0> bits.
UART	TX interrupt will be generated as soon as the UART module is enabled. Receive and transmit interrupts are controlled by the URXISEL<1:0> and UTXISEL<1:0> bits, respectively. To clear an interrupt source, data must be read from, or written to, the UxRXREG or UxTXREG registers to obtain the number of data to receive/transmit below the level specified by the URXISEL<1:0> and UTXISEL<1:0> bits.
ADC	All samples must be read from the result registers (ADC1BUFx) to clear the interrupt source.
PMP	To clear an interrupt source, read the Parallel Master Port Data Input/Output (PMDIN/PMDOUT) register.

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