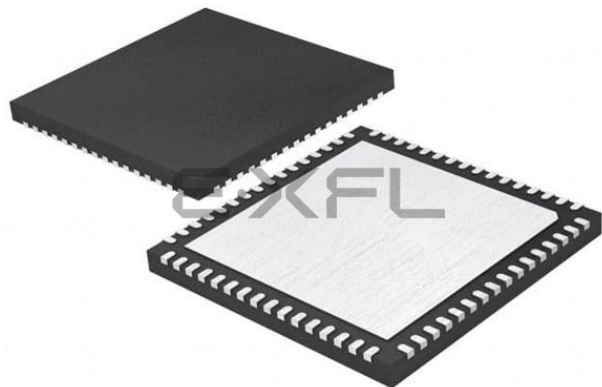




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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx564f128h-i-mr

PIC32MX5XX/6XX/7XX

TABLE 1: PIC32MX5XX USB AND CAN FEATURES

USB and CAN																
Device	Pins	Program Memory (KB)	Data Memory (KB)	USB	CAN	Timers/Capture/Compare	DMA Channels (Programmable/Dedicated)	UART ^(2,3)	SPI ⁽³⁾	I ² C ⁽³⁾	10-bit 1 Msps ADC (Channels)	Comparators	PMP/PSP	JTAG	Trace	Packages ⁽⁴⁾
PIC32MX534F064H	64	64 + 12 ⁽¹⁾	16	1	1	5/5/5	4/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX564F064H	64	64 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX564F128H	64	128 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX575F256H	64	256 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX575F512H	64	512 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	3	4	16	2	Yes	Yes	No	PT, MR
PIC32MX534F064L	100	64 + 12 ⁽¹⁾	16	1	1	5/5/5	4/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX564F064L	100	64 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX564F128L	100	128 + 12 ⁽¹⁾	32	1	1	5/5/5	4/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX575F256L	100	256 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG
PIC32MX575F512L	100	512 + 12 ⁽¹⁾	64	1	1	5/5/5	8/4	6	4	5	16	2	Yes	Yes	Yes	PT, PF, BG

Legend: PF, PT = TQFP MR = QFN BG = TFBGA TL = VTLA⁽⁵⁾

Note 1: This device features 12 KB boot Flash memory.

2: CTS and RTS pins may not be available for all UART modules. Refer to the “**Device Pin Tables**” section for more information.

3: Some pins between the UART, SPI and I²C modules may be shared. Refer to the “**Device Pin Tables**” section for more information.

4: Refer to **34.0 “Packaging Information”** for more information.

5: 100-pin devices in the VTLA package are available upon request. Please contact your local Microchip Sales Office for details.

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PIC32MX5XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
RG0	—	90	A5	A61	I/O	ST	PORTG is a bidirectional I/O port
RG1	—	89	E6	B50	I/O	ST	
RG6	4	10	E3	A7	I/O	ST	
RG7	5	11	F4	B6	I/O	ST	
RG8	6	12	F2	A8	I/O	ST	
RG9	8	14	F3	A9	I/O	ST	
RG12	—	96	C3	A65	I/O	ST	
RG13	—	97	A3	B55	I/O	ST	
RG14	—	95	C4	B54	I/O	ST	
RG15	—	1	B2	A2	I/O	ST	
RG2	37	57	H10	B31	I	ST	PORTG input pins
RG3	36	56	J11	A38	I	ST	
T1CK	48	74	B11	B40	I	ST	Timer1 external clock input
T2CK	—	6	D1	A5	I	ST	Timer2 external clock input
T3CK	—	7	E4	B4	I	ST	Timer3 external clock input
T4CK	—	8	E2	A6	I	ST	Timer4 external clock input
T5CK	—	9	E1	B5	I	ST	Timer5 external clock input
U1CTS	43	47	L9	B26	I	ST	UART1 clear to send
U1RTS	49	48	K9	A31	O	—	UART1 ready to send
U1RX	50	52	K11	A36	I	ST	UART1 receive
U1TX	51	53	J10	B29	O	—	UART1 transmit
U3CTS	8	14	F3	A9	I	ST	UART3 clear to send
U3RTS	4	10	E3	A7	O	—	UART3 ready to send
U3RX	5	11	F4	B6	I	ST	UART3 receive
U3TX	6	12	F2	A8	O	—	UART3 transmit
U2CTS	21	40	K6	A27	I	ST	UART2 clear to send
U2RTS	29	39	L6	B22	O	—	UART2 ready to send
U2RX	31	49	L10	B27	I	ST	UART2 receive
U2TX	32	50	L11	A32	O	—	UART2 transmit
U4RX	43	47	L9	B26	I	ST	UART4 receive
U4TX	49	48	K9	A31	O	—	UART4 transmit
U6RX	8	14	F3	A9	I	ST	UART6 receive
U6TX	4	10	E3	A7	O	—	UART6 transmit
U5RX	21	40	K6	A27	I	ST	UART5 receive
U5TX	29	39	L6	B22	O	—	UART5 transmit
SCK1	—	70	D11	B38	I/O	ST	Synchronous serial clock input/output for SPI1

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input
O = Output
P = Power
I = Input

Note 1: Pin numbers are only provided for reference. See the “**Device Pin Tables**” section for device pin availability.

2: See **25.0 “Ethernet Controller”** for more information.

PIC32MX5XX/6XX/7XX

NOTES:

PIC32MX5XX/6XX/7XX

NOTES:

PIC32MX5XX/6XX/7XX

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
Watchdog Timer	0xBF80	0x0000
RTCC		0x0200
Timer1-Timer5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
I2C1-I2C5		0x5000
SPI1-SPI4		0x5800
UART1-UART6		0x6000
PMP		0x7000
ADC		0x9000
CVREF		0x9800
Comparator		0xA000
Oscillator		0xF000
Device and Revision ID		0xF200
Flash Controller		0xF400
Reset		0xF600
Interrupts	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
Prefetch		0x4000
USB		0x5040
PORTA-PORTG		0x6000
Ethernet		0x9000
Configuration	0xBFC0	0x2FF0

TABLE 7-2: INTERRUPT REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H AND PIC32MX575F512H DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets			
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0		
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000		
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000		
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000		
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000		
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000		
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000		
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000		
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000		
10E0	IPC5	31:16	—	—	—	—	—	—	—	—	—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000		
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000		
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000		
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>			—	—	—	U1IP<2:0>			U1IS<1:0>		0000	
															SPI3IP<2:0>			SPI3IS<1:0>			
															I2C3IP<2:0>			I2C3IS<1:0>			
1100	IPC7	31:16	—	—	—	U3IP<2:0>			U3IS<1:0>			—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000	
						SPI2IP<2:0>			SPI2IS<1:0>												
						I2C4IP<2:0>			I2C4IS<1:0>												
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>			—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000	
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000		
		15:0	—	—	—	—	—	—	—	—	—	—	—	U2IP<2:0>			U2IS<1:0>		0000		
														SPI4IP<2:0>			SPI4IS<1:0>				
														I2C5IP<2:0>			I2C5IS<1:0>				
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000		
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000		
1130	IPC10	31:16	—	—	—	DMA7IP<2:0> ⁽²⁾			DMA7IS<1:0> ⁽²⁾		—	—	—	DMA6IP<2:0> ⁽²⁾			DMA6IS<1:0> ⁽²⁾		0000		
		15:0	—	—	—	DMA5IP<2:0> ⁽²⁾			DMA5IS<1:0> ⁽²⁾		—	—	—	DMA4IP<2:0> ⁽²⁾			DMA4IS<1:0> ⁽²⁾		0000		
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		0000		
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000		
1150	IPC12	31:16	—	—	—	U5IP<2:0>			U5IS<1:0>		—	—	—	U6IP<2:0>			U6IS<1:0>		0000		
		15:0	—	—	—	U4IP<2:0>			U4IS<1:0>		—	—	—	—	—	—	—	—	0000		

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- Note 2:** These bits are not available on PIC32MX534/564/664/764 devices.
- Note 3:** This register does not have associated CLR, SET, and INV registers.

TABLE 7-6: INTERRUPT REGISTER MAP FOR PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L AND PIC32MX695F512L DEVICES

Virtual Address (BF88-#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000	
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000	
1010	INTSTAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>					0000		
1020	IPTMR	31:16	IPTMR<31:0>																0000	
		15:0																	0000	
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000	
		SPI3TXIF	SPI3RXIF	SPI3EIF	SPI4TXIF	SPI4RXIF	SPI4EIF													
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000	
1040	IFS1	31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	—	—	USBIF	FCEIF	DMA7IF ⁽²⁾	DMA6IF ⁽²⁾	DMA5IF ⁽²⁾	DMA4IF ⁽²⁾	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000	
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	U3TXIF	U3RXIF	U3EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000	
								SPI4TXIF	SPI4RXIF	SPI4EIF	SPI2TXIF	SPI2RXIF	SPI2EIF							I2C5MIF
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000	
		SPI3TXIE	SPI3RXIE	SPI3EIE	SPI4TXIE	SPI4RXIE	SPI4EIE													
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000	
1070	IEC1	31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	—	—	USBIE	FCEIE	DMA7IE ⁽²⁾	DMA6IE ⁽²⁾	DMA5IE ⁽²⁾	DMA4IE ⁽²⁾	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000	
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	U3TXIE	U3RXIE	U3EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000	
								SPI4TXIE	SPI4RXIE	SPI4EIE	SPI2TXIE	SPI2RXIE	SPI2EIE							
								I2C5MIE	I2C5SIE	I2C5BIE	I2C4MIE	I2C4SIE	I2C4BIE							
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>			—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>			—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>			—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>			—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>			—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>			—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>			—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>			—	—	—	T3IP<2:0>			T3IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2: These bits are not available on PIC32MX664 devices.
- 3: This register does not have associated CLR, SET, and INV registers.

9.2 Control Registers

TABLE 9-1: PREFETCH REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
4000	CHECON ^(1,2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHECOH	0000	
		15:0	—	—	—	—	—	DCSZ<1:0>			—	—	PREFEN<1:0>		—	PFMWS<2:0>			0007	
4010	CHEACC ⁽¹⁾	31:16	CHEWEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CHEIDX<3:0>					0000
4020	CHETAG ⁽¹⁾	31:16	LTAGBOOT	—	—	—	—	—	—	—	LTAG<23:16>									00xx
		15:0	LTAG<15:4>												LVALID	LLOCK	LTYPE	—	xxx2	
4030	CHEMSK ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	LMASK<15:5>												—	—	—	—	—	0000
4040	CHEW0	31:16	CHEW0<31:0>																xxxx	
		15:0	CHEW0<31:0>																xxxx	
4050	CHEW1	31:16	CHEW1<31:0>																xxxx	
		15:0	CHEW1<31:0>																xxxx	
4060	CHEW2	31:16	CHEW2<31:0>																xxxx	
		15:0	CHEW2<31:0>																xxxx	
4070	CHEW3	31:16	CHEW3<31:0>																xxxx	
		15:0	CHEW3<31:0>																xxxx	
4080	CHELRU	31:16	—	—	—	—	—	—	—	CHELRU<24:16>									0000	
		15:0	CHELRU<15:0>																0000	
4090	CHEHIT	31:16	CHEHIT<31:0>																xxxx	
		15:0	CHEHIT<31:0>																xxxx	
40A0	CHEMIS	31:16	CHEMIS<31:0>																xxxx	
		15:0	CHEMIS<31:0>																xxxx	
40C0	CHEPFABT	31:16	CHEPFABT<31:0>																xxxx	
		15:0	CHEPFABT<31:0>																xxxx	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
 2: Reset value is dependent on DEVCFGx configuration.

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

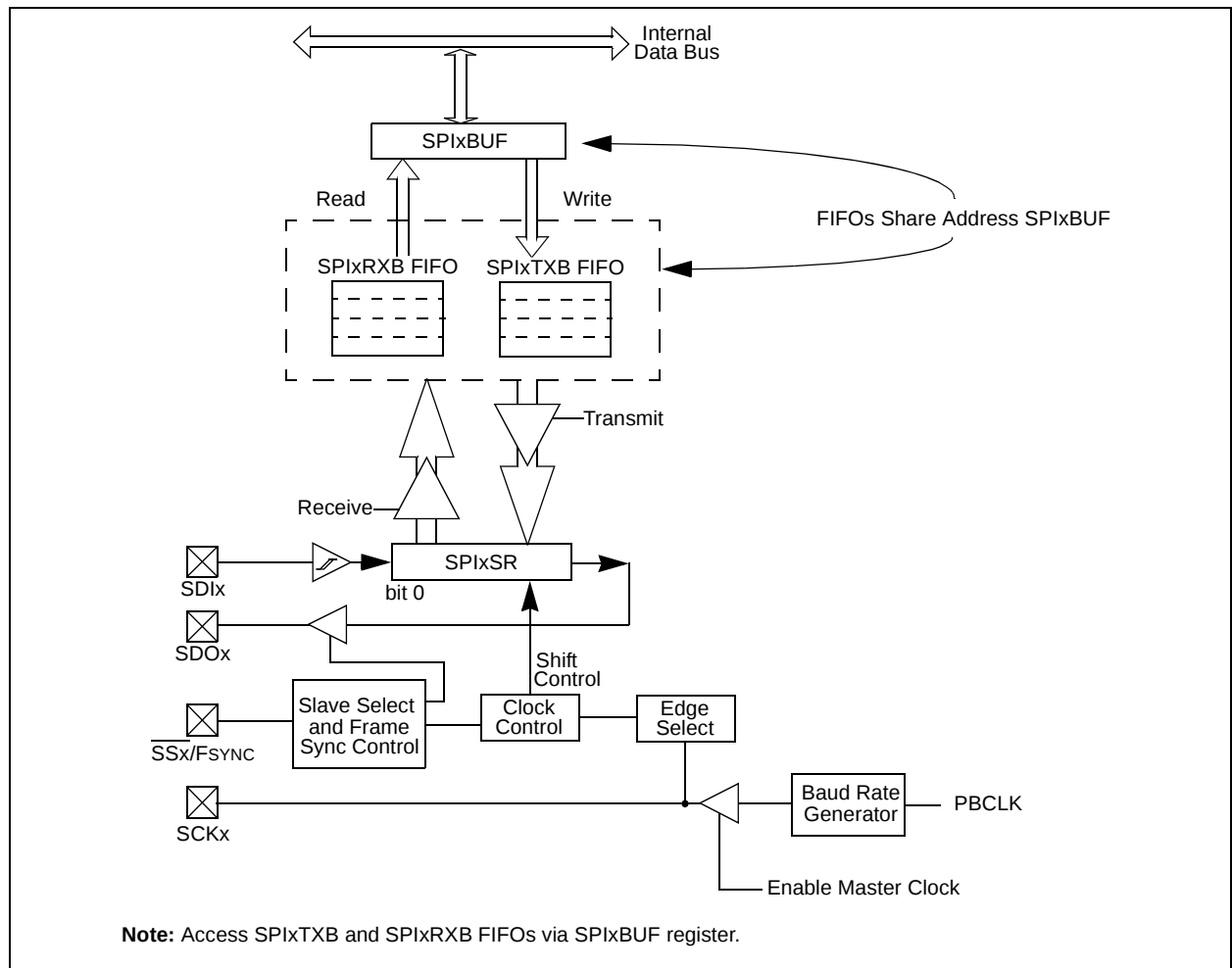
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters, etc. The PIC32 SPI module is compatible with Motorola® SPI and SIOP interfaces.

The following are some of the key features of the SPI module:

- Master mode and Slave mode support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
 - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

FIGURE 18-1: SPI MODULE BLOCK DIAGRAM



20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

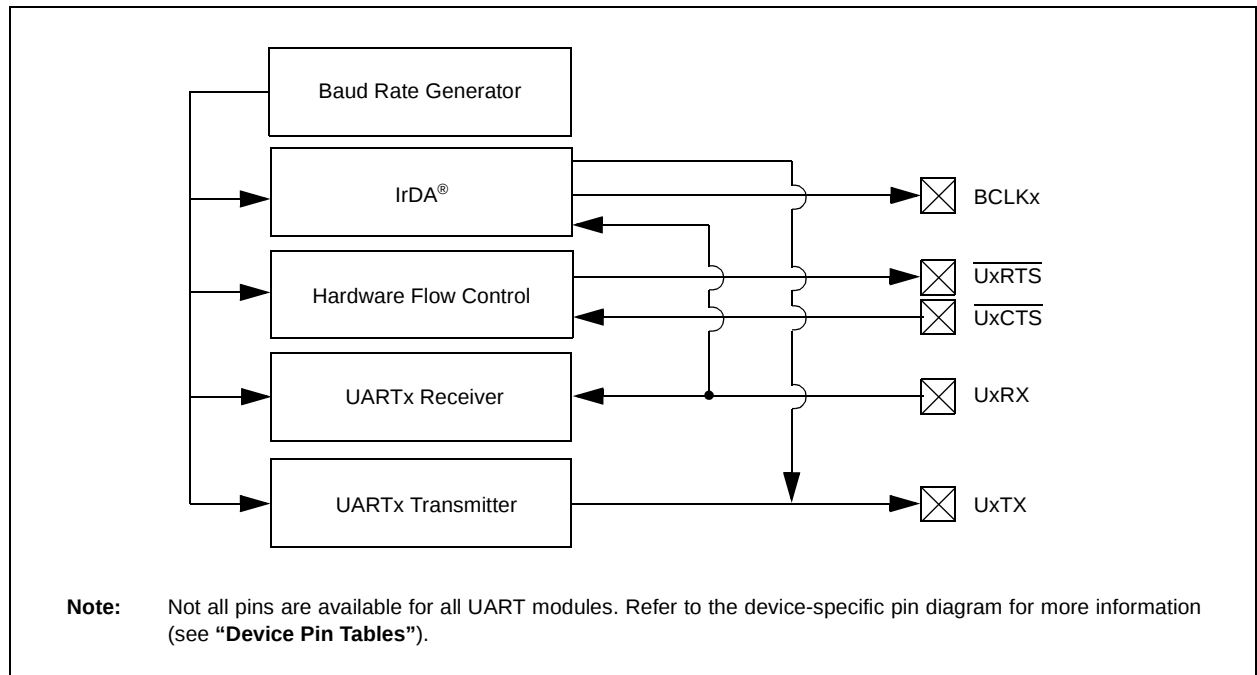
The UART module is one of the serial I/O modules available in the PIC32MX5XX/6XX/7XX family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN 1.2 and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The following are primary features of the UART module:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 20 Mbps at 80 MHz
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (ninth bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN 2.1 Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 20-1 illustrates a simplified block diagram of the UART module.

FIGURE 20-1: UART SIMPLIFIED BLOCK DIAGRAM



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REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5 **ABAUD**: Auto-Baud Enable bit
 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55);
 cleared by hardware upon completion
 0 = Baud rate measurement disabled or completed
- bit 4 **RXINV**: Receive Polarity Inversion bit
 1 = UxRX Idle state is '0'
 0 = UxRX Idle state is '1'
- bit 3 **BRGH**: High Baud Rate Enable bit
 1 = High-Speed mode – 4x baud clock enabled
 0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1 **PDSEL<1:0>**: Parity and Data Selection bits
 11 = 9-bit data, no parity
 10 = 8-bit data, odd parity
 01 = 8-bit data, even parity
 00 = 8-bit data, no parity
- bit 0 **STSEL**: Stop Selection bit
 1 = 2 Stop bits
 0 = 1 Stop bit

Note 1: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

23.1 Control Registers

TABLE 23-1: ADC REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	AD1CON1 ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE	0000
9010	AD1CON2 ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000
9020	AD1CON3 ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>								0000
9040	AD1CHS ⁽¹⁾	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9060	AD1PCFG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
9050	AD1CSSL ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16	ADC Result Word 0 (ADC1BUF0<31:0>)																0000
		15:0																	0000
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)																0000
		15:0																	0000
9090	ADC1BUF2	31:16	ADC Result Word 2 (ADC1BUF2<31:0>)																0000
		15:0																	0000
90A0	ADC1BUF3	31:16	ADC Result Word 3 (ADC1BUF3<31:0>)																0000
		15:0																	0000
90B0	ADC1BUF4	31:16	ADC Result Word 4 (ADC1BUF4<31:0>)																0000
		15:0																	0000
90C0	ADC1BUF5	31:16	ADC Result Word 5 (ADC1BUF5<31:0>)																0000
		15:0																	0000
90D0	ADC1BUF6	31:16	ADC Result Word 6 (ADC1BUF6<31:0>)																0000
		15:0																	0000
90E0	ADC1BUF7	31:16	ADC Result Word 7 (ADC1BUF7<31:0>)																0000
		15:0																	0000
90F0	ADC1BUF8	31:16	ADC Result Word 8 (ADC1BUF8<31:0>)																0000
		15:0																	0000
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)																0000
		15:0																	0000
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

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REGISTER 24-7: CîRXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **RXOVF<31:0>**: FIFO n Receive Overflow Interrupt Pending bit

1 = FIFO has overflowed

0 = FIFO has not overflowed

REGISTER 24-8: CîTMR: CAN TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CANTS<15:0>**: CAN Time Stamp Timer bits

This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (CiCON<20>) is set.

bit 15-0 **CANTSPRE<15:0>**: CAN Time Stamp Timer Prescaler bits

1111 1111 1111 1111 = CAN time stamp timer (CANTS) increments every 65,535 system clocks

.

.

.

0000 0000 0000 0000 = CAN time stamp timer (CANTS) increments every system clock

Note 1: CîTMR will be paused when CANCAP = 0.

2: The CîTMR prescaler count will be reset on any write to CîTMR (CANTSPRE will be unaffected).

REGISTER 25-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

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REGISTER 25-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER (CONTINUED)

- bit 6 **VLANPAD:** VLAN Pad Enable bit^(1,2)
1 = The MAC will pad all short frames to 64 bytes and append a valid CRC
0 = The MAC does not perform padding of short frames
- bit 5 **PADENABLE:** Pad/CRC Enable bit^(1,3)
1 = The MAC will pad all short frames
0 = The frames presented to the MAC have a valid length
- bit 4 **CRCENABLE:** CRC Enable1 bit
1 = The MAC will append a CRC to every frame whether padding was required or not. Must be set if the PADENABLE bit is set.
0 = The frames presented to the MAC have a valid CRC
- bit 3 **DELAYCRC:** Delayed CRC bit
This bit determines the number of bytes, if any, of proprietary header information that exist on the front of the IEEE 802.3 frames.
1 = Four bytes of header (ignored by the CRC function)
0 = No proprietary header
- bit 2 **HUGEFRM:** Huge Frame enable bit
1 = Frames of any length are transmitted and received
0 = Huge frames are not allowed for receive or transmit
- bit 1 **LENGTHCK:** Frame Length checking bit
1 = Both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the transmit/receive statistics vector.
0 = Length/Type field check is not performed
- bit 0 **FULLDPLX:** Full-Duplex Operation bit
1 = The MAC operates in Full-Duplex mode
0 = The MAC operates in Half-Duplex mode

Note 1: Table 25-6 provides a description of the pad function based on the configuration of this register.

2: This bit is ignored if the PADENABLE bit is cleared.

3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

TABLE 25-6: PAD OPERATION

Type	AUTOPAD	VLANPAD	PADENABLE	Action
Any	x	x	0	No pad, check CRC
Any	0	0	1	Pad to 60 Bytes, append CRC
Any	x	1	1	Pad to 64 Bytes, append CRC
Any	1	0	1	If untagged: Pad to 60 Bytes, append CRC If VLAN tagged: Pad to 64 Bytes, append CRC

TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Typical ⁽³⁾	Max.	Units	Conditions			
Operating Current (IDD) ^(1,2) for PIC32MX534/564/664/764 Family Devices							
DC20c	6	9	mA	Code executing from Flash	-40°C, +25°C, +85°C	—	4 MHz
DC20d	7	10			+105°C		
DC20e	2	—		Code executing from SRAM	—		
DC21b	19	32	mA	Code executing from Flash	—	—	25 MHz (Note 4)
DC21c	14	—		Code executing from SRAM			
DC22b	31	50	mA	Code executing from Flash	—	—	60 MHz (Note 4)
DC22c	29	—		Code executing from SRAM			
DC23c	39	65	mA	Code executing from Flash	-40°C, +25°C, +85°C	—	80 MHz
DC23d	49	70			+105°C		
DC23e	39	—		Code executing from SRAM	—		
DC25b	100	150	μA	—	+25°C	3.3V	LPRC (31 kHz) (Note 4)

Note 1: A device's I_{DD} supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for I_{DD} measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = \text{V}_{\text{DD}}$
- CPU executing while(1) statement from Flash
- RTCC and JTAG are disabled

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

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Real-Time Clock and Calendar (RTCC).....	221	DCHxDPTR (Channel 'x' Destination Pointer).....	130
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Registers		Start Address).....	128
AD1CHS (ADC Input Select)	239	DCHxDSIZ (DMA Channel 'x' Destination Size).....	129
AD1CON1 (ADC Control 1)	235	DCHxECON (DMA Channel 'x' Event Control).....	125
AD1CON2 (ADC Control 2)	237	DCHxINT (DMA Channel 'x' Interrupt Control)	126
AD1CON3 (ADC Control 3)	238	DCHxSPTR (DMA Channel 'x' Source Pointer).....	130
AD1CSSL (ADC Input Scan Select)	240	DCHxSSA (DMA Channel 'x' Source Start Address)	128
ALRMDATE (Alarm Date Value)	230	DCHxSSIZ (DMA Channel 'x' Source Size).....	129
ALRMTIME (Alarm Time Value)	229	DCRCCON (DMA CRC Control).....	121
BMXBOOTSZ (Boot Flash (IFM) Size)	61	DCRCDATA (DMA CRC Data)	123
BMXCON (Bus Matrix Configuration)	56	DCRCXOR (DMA CRCXOR Enable)	123
BMXDKPBA (Data RAM Kernel Program		DDPCON (Debug Data Port Control)	342
Base Address)	57	DEVCFG0 (Device Configuration Word 0).....	335
BMXDRMSZ (Data RAM Size)	60	DEVCFG1 (Device Configuration Word 1).....	337
BMXDUDBA (Data RAM User Data Base Address)	58	DEVCFG2 (Device Configuration Word 2).....	339
BMXDUPBA (Data RAM User Program		DEVCFG3 (Device Configuration Word 3).....	341
Base Address)	59	DEVID (Device and Revision ID).....	342
BMXPFMSZ (Program Flash (PFM) Size)	61	DMAADDR (DMA Address).....	120
BMXPUPBA (Program Flash (PFM) User Program		DMACON (DMA Controller Control)	119
Base Address)	60	DMASTAT (DMA Status).....	120
CHEACC (Cache Access)	104	EMAC1CFG1 (Ethernet Controller MAC Configuration 1)	306
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CHEHIT (Cache Hit Statistics)	109	EMAC1CLRT (Ethernet Controller MAC Collision Win-	
CHELRU (Cache LRU)	108	dow/Retry Limit).....	311
CHEMIS (Cache Miss Statistics)	109	EMAC1IPGR (Ethernet Controller MAC Non-Back-to-	
CHEMSK (Cache TAG Mask)	106	Back Interpacket Gap).....	310
CHETAG (Cache TAG)	105	EMAC1IPGT (Ethernet Controller MAC Back-to-Back In-	
CHEW0 (Cache Word 0)	106	terpacket Gap).....	309
CHEW1 (Cache Word 1)	107	EMAC1MADR (Ethernet Controller MAC MII Manage-	
CHEW2 (Cache Word 2)	107	ment Address)	317
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