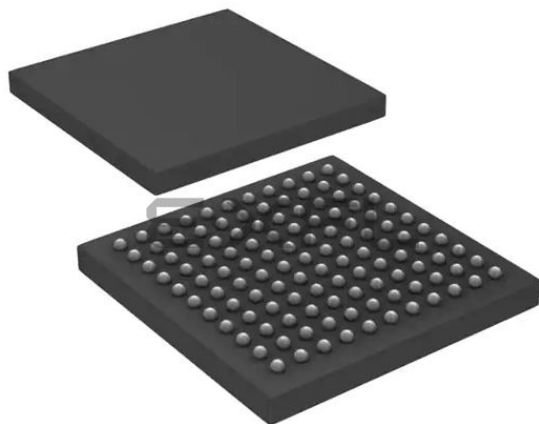




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx564f128lt-i-bg

TABLE 7: PIN NAMES FOR 100-PIN USB AND CAN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MX534F064L
 PIC32MX564F064L
 PIC32MX564F128L
 PIC32MX575F512L
 PIC32MX575F256L

100

1

Pin #	Full Pin Name
71	IC4/PMCS1/PMA14/RD11
72	SDO1/OC1/INT0/RD0
73	SOSCI/CN1/RC13
74	SOSCO/T1CK/CN0/RC14
75	Vss
76	OC2/RD1
77	OC3/RD2
78	OC4/RD3
79	IC5/PMD12/RD12
80	PMD13/CN19/RD13
81	OC5/PMWR/CN13/RD4
82	PMRD/CN14/RD5
83	PMD14/CN15/RD6
84	PMD15/CN16/RD7
85	VCAP

Pin #	Full Pin Name
86	VDD
87	C1RX/PMD11/RF0
88	C1TX/PMD10/RF1
89	PMD9/RG1
90	PMD8/RG0
91	TRCLK/RA6
92	TRD3/RA7
93	PMD0/RE0
94	PMD1/RE1
95	TRD2/RG14
96	TRD1/RG12
97	TRD0/RG13
98	PMD2/RE2
99	PMD3/RE3
100	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
AC2TX	—	7	E4	B4	O	—	Alternate CAN2 bus transmit pin
ERXD0	61	41	J7	B23	I	ST	Ethernet Receive Data 0 ⁽²⁾
ERXD1	60	42	L7	A28	I	ST	Ethernet Receive Data 1 ⁽²⁾
ERXD2	59	43	K7	B24	I	ST	Ethernet Receive Data 2 ⁽²⁾
ERXD3	58	44	L8	A29	I	ST	Ethernet Receive Data 3 ⁽²⁾
ERXERR	64	35	J5	B20	I	ST	Ethernet receive error input ⁽²⁾
ERXDV	62	12	F2	A8	I	ST	Ethernet receive data valid ⁽²⁾
ECRSdv	62	12	F2	A8	I	ST	Ethernet carrier sense data valid ⁽²⁾
ERXCLK	63	14	F3	A9	I	ST	Ethernet receive clock ⁽²⁾
EREFCLK	63	14	F3	A9	I	ST	Ethernet reference clock ⁽²⁾
ETXD0	2	88	A6	A60	O	—	Ethernet Transmit Data 0 ⁽²⁾
ETXD1	3	87	B6	B49	O	—	Ethernet Transmit Data 1 ⁽²⁾
ETXD2	43	79	A9	B43	O	—	Ethernet Transmit Data 2 ⁽²⁾
ETXD3	42	80	D8	A54	O	—	Ethernet Transmit Data 3 ⁽²⁾
ETXERR	54	89	E6	B50	O	—	Ethernet transmit error ⁽²⁾
ETXEN	1	83	D7	B45	O	—	Ethernet transmit enable ⁽²⁾
ETXCLK	55	84	C7	A56	I	ST	Ethernet transmit clock ⁽²⁾
ECOL	44	10	E3	A7	I	ST	Ethernet collision detect ⁽²⁾
ECRS	45	11	F4	B6	I	ST	Ethernet carrier sense ⁽²⁾
EMDC	30	71	C11	A46	O	—	Ethernet management data clock ⁽²⁾
EMDIO	49	68	E9	B37	I/O	—	Ethernet management data ⁽²⁾
AERXD0	43	18	G1	A11	I	ST	Alternate Ethernet Receive Data 0 ⁽²⁾
AERXD1	42	19	G2	B10	I	ST	Alternate Ethernet Receive Data 1 ⁽²⁾
AERXD2	—	28	L2	A21	I	ST	Alternate Ethernet Receive Data 2 ⁽²⁾
AERXD3	—	29	K3	B17	I	ST	Alternate Ethernet Receive Data 3 ⁽²⁾
AERXERR	55	1	B2	A2	I	ST	Alternate Ethernet receive error input ⁽²⁾
AERXDV	—	12	F2	A8	I	ST	Alternate Ethernet receive data valid ⁽²⁾
AECRSdv	44	12	F2	A8	I	ST	Alternate Ethernet carrier sense data valid ⁽²⁾
AERXCLK	—	14	F3	A9	I	ST	Alternate Ethernet receive clock ⁽²⁾
AEREFCLK	45	14	F3	A9	I	ST	Alternate Ethernet reference clock ⁽²⁾
AETXD0	59	47	L9	B26	O	—	Alternate Ethernet Transmit Data 0 ⁽²⁾
AETXD1	58	48	K9	A31	O	—	Alternate Ethernet Transmit Data 1 ⁽²⁾
AETXD2	—	44	L8	A29	O	—	Alternate Ethernet Transmit Data 2 ⁽²⁾
AETXD3	—	43	K7	B24	O	—	Alternate Ethernet Transmit Data 3 ⁽²⁾
AETXERR	—	35	J5	B20	O	—	Alternate Ethernet transmit error ⁽²⁾
AETXEN	54	67	E8	A44	O	—	Alternate Ethernet transmit enable ⁽²⁾
AETXCLK	—	66	E11	B36	I	ST	Alternate Ethernet transmit clock ⁽²⁾
AECOL	—	42	L7	A28	I	ST	Alternate Ethernet collision detect ⁽²⁾

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input P = Power
O = Output I = Input

Note 1: Pin numbers are only provided for reference. See the “**Device Pin Tables**” section for device pin availability.

2: See **25.0 “Ethernet Controller”** for more information.

PIC32MX5XX/6XX/7XX

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
Watchdog Timer	0xBF80	0x0000
RTCC		0x0200
Timer1-Timer5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
I2C1-I2C5		0x5000
SPI1-SPI4		0x5800
UART1-UART6		0x6000
PMP		0x7000
ADC		0x9000
CVREF		0x9800
Comparator		0xA000
Oscillator		0xF000
Device and Revision ID		0xF200
Flash Controller		0xF400
Reset		0xF600
Interrupts	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
Prefetch		0x4000
USB		0x5040
PORTA-PORTG		0x6000
Ethernet		0x9000
Configuration	0xBFC0	0x2FF0

5.1 Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
F400	NVMCON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	—	—	—	—	—	—	NVMOP<3:0>				0000
F410	NVMKEY	31:16	NVMKEY<31:0>															0000
		15:0																0000
F420	NVMADDR ⁽¹⁾	31:16	NVMADDR<31:0>															0000
		15:0																0000
F430	NVMDATA	31:16	NVMDATA<31:0>															0000
		15:0																0000
F440	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>															0000
		15:0																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

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NOTES:

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 IFS31	R/W-0 IFS30	R/W-0 IFS29	R/W-0 IFS28	R/W-0 IFS27	R/W-0 IFS26	R/W-0 IFS25	R/W-0 IFS24
23:16	R/W-0 IFS23	R/W-0 IFS22	R/W-0 IFS21	R/W-0 IFS20	R/W-0 IFS19	R/W-0 IFS18	R/W-0 IFS17	R/W-0 IFS16
15:8	R/W-0 IFS15	R/W-0 IFS14	R/W-0 IFS13	R/W-0 IFS12	R/W-0 IFS11	R/W-0 IFS10	R/W-0 IFS09	R/W-0 IFS08
7:0	R/W-0 IFS07	R/W-0 IFS06	R/W-0 IFS05	R/W-0 IFS04	R/W-0 IFS03	R/W-0 IFS02	R/W-0 IFS01	R/W-0 IFS00

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IFS31-IFS00:** Interrupt Flag Status bits

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 IEC31	R/W-0 IEC30	R/W-0 IEC29	R/W-0 IEC28	R/W-0 IEC27	R/W-0 IEC26	R/W-0 IEC25	R/W-0 IEC24
23:16	R/W-0 IEC23	R/W-0 IEC22	R/W-0 IEC21	R/W-0 IEC20	R/W-0 IEC19	R/W-0 IEC18	R/W-0 IEC17	R/W-0 IEC16
15:8	R/W-0 IEC15	R/W-0 IEC14	R/W-0 IEC13	R/W-0 IEC12	R/W-0 IEC11	R/W-0 IEC10	R/W-0 IEC09	R/W-0 IEC08
7:0	R/W-0 IEC07	R/W-0 IEC06	R/W-0 IEC05	R/W-0 IEC04	R/W-0 IEC03	R/W-0 IEC02	R/W-0 IEC01	R/W-0 IEC00

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IEC31-IEC00:** Interrupt Enable bits

1 = Interrupt is enabled

0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	—	CRCCH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (reverse source byte order)

00 = No swapping (source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (reflected)

0 = The LFSR CRC is calculated Most Significant bit first (not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits⁽¹⁾

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

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NOTES:

REGISTER 17-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON ⁽¹⁾	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT ⁽²⁾	OCTSEL	OCM<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Module On bit⁽¹⁾

1 = Output Compare module is enabled

0 = Output Compare module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue operation when CPU enters Idle mode

0 = Continue operation when CPU is in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit

1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source

0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit⁽²⁾

1 = PWM Fault condition has occurred (only cleared in hardware)

0 = PWM Fault condition has not occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit

1 = Timer3 is the clock source for this Output Compare module

0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits

111 = PWM mode on OCx; Fault pin enabled

110 = PWM mode on OCx; Fault pin disabled

101 = Initialize OCx pin low; generate continuous output pulses on OCx pin

100 = Initialize OCx pin low; generate single output pulse on OCx pin

011 = Compare event toggles OCx pin

010 = Initialize OCx pin high; compare event forces OCx pin low

001 = Initialize OCx pin low; compare event forces OCx pin high

000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only used when OCM<2:0> = 111. It is read as '0' in all other modes.

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REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer
- bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (has at least 1 data character)
- bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode is disabled
- bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is idle
0 = Data is being received
- bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected
- bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected
- bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to an empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed
- bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

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REGISTER 22-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)

- bit 3 **RTCWREN:** RTC Value Registers Write Enable bit⁽⁴⁾
1 = RTC Value registers can be written to by the user
0 = RTC Value registers are locked out from being written to by the user
- bit 2 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = RTC Value registers can be read without concern about a rollover ripple
- bit 1 **HALFSEC:** Half-Second Status bit⁽⁵⁾
1 = Second half period of a second
0 = First half period of a second
- bit 0 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled (clock presented onto an I/O)
0 = RTCC clock output is disabled

- Note 1:** The ON bit is only writable when RTCWREN = 1.
- 2:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
- 4:** The RTCWREN bit can only be set when the write sequence is enabled.
- 5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is only reset on a Power-on Reset (POR).

TABLE 24-1: CAN1 REGISTER SUMMARY FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B0F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>				FSEL15<4:0>			FLTEN14	MSEL14<1:0>			FSEL14<4:0>				0000
		15:0	FLTEN13	MSEL13<1:0>				FSEL13<4:0>			FLTEN12	MSEL12<1:0>			FSEL12<4:0>				0000
B100	C1FLTCON4	31:16	FLTEN19	MSEL19<1:0>				FSEL19<4:0>			FLTEN18	MSEL18<1:0>			FSEL18<4:0>				0000
		15:0	FLTEN17	MSEL17<1:0>				FSEL17<4:0>			FLTEN16	MSEL16<1:0>			FSEL16<4:0>				0000
B110	C1FLTCON5	31:16	FLTEN23	MSEL23<1:0>				FSEL23<4:0>			FLTEN22	MSEL22<1:0>			FSEL22<4:0>				0000
		15:0	FLTEN21	MSEL21<1:0>				FSEL21<4:0>			FLTEN20	MSEL20<1:0>			FSEL20<4:0>				0000
B120	C1FLTCON6	31:16	FLTEN27	MSEL27<1:0>				FSEL27<4:0>			FLTEN26	MSEL26<1:0>			FSEL26<4:0>				0000
		15:0	FLTEN25	MSEL25<1:0>				FSEL25<4:0>			FLTEN24	MSEL24<1:0>			FSEL24<4:0>				0000
B130	C1FLTCON7	31:16	FLTEN31	MSEL31<1:0>				FSEL31<4:0>			FLTEN30	MSEL30<1:0>			FSEL30<4:0>				0000
		15:0	FLTEN29	MSEL29<1:0>				FSEL29<4:0>			FLTEN28	MSEL28<1:0>			FSEL28<4:0>				0000
B140	C1RXFn (n = 0-31)	31:16	SID<10:0>											—	EXID	—	EID<17:16>	xxxx	
		15:0	EID<15:0>																xxxx
B340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0	C1FIFOBA<31:0>																0000
B350	C1FIFOCOn (n = 0-31)	31:16	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000	
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>	0000	
B360	C1FIFOINTn (n = 0-31)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
B370	C1FIFOUAn (n = 0-31)	31:16	C1FIFOUA<31:0>																0000
		15:0	C1FIFOUA<31:0>																0000
B380	C1FIFOCIn (n = 0-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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Table 25-1, Table 25-2, Table 25-3 and Table 25-4 show four interfaces and the associated pins that can be used with the Ethernet Controller.

TABLE 25-1: MII MODE DEFAULT INTERFACE SIGNALS (FMIEN = 1, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXCLK	Transmit Clock
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
ETXD2	Transmit Data
ETXD3	Transmit Data
ETXERR	Transmit Error
ERXCLK	Receive Clock
ERXDV	Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXD2	Receive Data
ERXD3	Receive Data
ERXERR	Receive Error
ECRS	Carrier Sense
ECOL	Collision Indication

TABLE 25-2: RMII MODE DEFAULT INTERFACE SIGNALS (FMIEN = 0, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
EREFCLK	Reference Clock
ECRSDV	Carrier Sense – Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXERR	Receive Error

Note: Ethernet controller pins that are not used by selected interface can be used by other peripherals.

TABLE 25-3: MII MODE ALTERNATE INTERFACE SIGNALS (FMIEN = 1, FETHIO = 0)

Pin Name	Description
AEMDC	Management Clock
AEMDIO	Management I/O
AETXCLK	Transmit Clock
AETXEN	Transmit Enable
AETXD0	Transmit Data
AETXD1	Transmit Data
AETXD2	Transmit Data
AETXD3	Transmit Data
AETXERR	Transmit Error
AERXCLK	Receive Clock
AERXDV	Receive Data Valid
AERXD0	Receive Data
AERXD1	Receive Data
AERXD2	Receive Data
AERXD3	Receive Data
AERXERR	Receive Error
AECRS	Carrier Sense
AECOL	Collision Indication

Note: The MII mode Alternate Interface is not available on 64-pin devices.

TABLE 25-4: RMII MODE ALTERNATE INTERFACE SIGNALS (FMIEN = 0, FETHIO = 0)

Pin Name	Description
AEMDC	Management Clock
AEMDIO	Management I/O
AETXEN	Transmit Enable
AETXD0	Transmit Data
AETXD1	Transmit Data
AEREFCLK	Reference Clock
AECRSDV	Carrier Sense – Receive Data Valid
AERXD0	Receive Data
AERXD1	Receive Data
AERXERR	Receive Error

25.1 Control Registers

TABLE 25-5: ETHERNET CONTROLLER REGISTER SUMMARY FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX695F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX764F128H, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	ETHCON1	31:16	PTV<15:0>																0000
		15:0	ON	—	SIDL	—	—	—	TXRTS	RXEN	AUTOFC	—	—	MANFC	—	—	—	BUFCDEC	0000
9010	ETHCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RXBUFSZ<6:0>							—	—	—	—	0000
9020	ETHTXST	31:16	TXSTADDR<31:16>																0000
		15:0	TXSTADDR<15:2>													—	—	—	0000
9030	ETHRXST	31:16	RXSTADDR<31:16>																0000
		15:0	RXSTADDR<15:2>													—	—	—	0000
9040	ETHHT0	31:16	HT<31:0>																0000
		15:0																	0000
9050	ETHHT1	31:16	HT<63:32>																0000
		15:0																	0000
9060	ETHPMM0	31:16	PMM<31:0>																0000
		15:0																	0000
9070	ETHPMM1	31:16	PMM<63:32>																0000
		15:0																	0000
9080	ETHPMCS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMCS<15:0>																0000
9090	ETHPMO	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMO<15:0>																0000
90A0	ETHRXFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	HTEN	MPEN	—	NOTPM	PMMODE<3:0>				CRC ERREN	CRC OKEN	RUNT ERREN	RUNTEN	UCEN	NOT MEEN	MCEN	BCEN	0000
90B0	ETHRXWM	31:16	—	—	—	—	—	—	—	RXFWM<7:0>									0000
		15:0	—	—	—	—	—	—	RXEWM<7:0>									0000	
90C0	ETHIEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TX BUSEIE	RX BUSEIE	—	—	—	EW MARKIE	FW MARKIE	RX DONEIE	PK TPENDIE	RX ACTIE	—	TX DONEIE	TX ABORTIE	RX BUFNAIE	RX OVFLWIE	0000
90D0	ETHIRQ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TXBUSE	RXBUSE	—	—	—	EWMARK	FWMARK	RXDONE	PKTPEND	RXACT	—	TXDONE	TXABORT	RXBUFNA	RXOVFLW	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

Note 2: Reset values default to the factory programmed value.

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REGISTER 25-13: ETHIEN: ETHERNET CONTROLLER INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
15:8	U-0	RW-0	RW-0	U-0	U-0	U-0	RW-0	RW-0
7:0	—	TXBUSEIE ⁽¹⁾	RXBUSEIE ⁽²⁾	—	—	—	EWMARKIE ⁽²⁾	FWMARKIE ⁽²⁾
	RW-0	RW-0	RW-0	U-0	RW-0	RW-0	RW-0	RW-0
	RXDONEIE ⁽²⁾	PKTPENDIE ⁽²⁾	RXACTIE ⁽²⁾	—	TXDONEIE ⁽¹⁾	TXABORTIE ⁽¹⁾	RXBUFNAIE ⁽²⁾	RXOVFLWIE ⁽²⁾

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSEIE:** Transmit BVCi Bus Error Interrupt Enable bit⁽¹⁾

1 = Enable TXBUS Error Interrupt

0 = Disable TXBUS Error Interrupt

bit 13 **RXBUSEIE:** Receive BVCi Bus Error Interrupt Enable bit⁽²⁾

1 = Enable RXBUS Error Interrupt

0 = Disable RXBUS Error Interrupt

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARKIE:** Empty Watermark Interrupt Enable bit⁽²⁾

1 = Enable EWMARK Interrupt

0 = Disable EWMARK Interrupt

bit 8 **FWMARKIE:** Full Watermark Interrupt Enable bit⁽²⁾

1 = Enable FWMARK Interrupt

0 = Disable FWMARK Interrupt

bit 7 **RXDONEIE:** Receiver Done Interrupt Enable bit⁽²⁾

1 = Enable RXDONE Interrupt

0 = Disable RXDONE Interrupt

bit 6 **PKTPENDIE:** Packet Pending Interrupt Enable bit⁽²⁾

1 = Enable PKTPEND Interrupt

0 = Disable PKTPEND Interrupt

bit 5 **RXACTIE:** RX Activity Interrupt Enable bit

1 = Enable RXACT Interrupt

0 = Disable RXACT Interrupt

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONEIE:** Transmitter Done Interrupt Enable bit⁽¹⁾

1 = Enable TXDONE Interrupt

0 = Disable TXDONE Interrupt

bit 2 **TXABORTIE:** Transmitter Abort Interrupt Enable bit⁽¹⁾

1 = Enable TXABORT Interrupt

0 = Disable TXABORT Interrupt

bit 1 **RXBUFNAIE:** Receive Buffer Not Available Interrupt Enable bit⁽²⁾

1 = Enable RXBUFNA Interrupt

0 = Disable RXBUFNA Interrupt

bit 0 **RXOVFLWIE:** Receive FIFO Overflow Interrupt Enable bit⁽²⁾

1 = Enable RXOVFLW Interrupt

0 = Disable RXOVFLW Interrupt

Note 1: This bit is only used for TX operations.

2: This bit is only used for RX operations.

REGISTER 25-18: ETHSCOLFRM: ETHERNET CONTROLLER SINGLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCOLFRMCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **SCOLFRMCNT<15:0>:** Single Collision Frame Count bits

Increment count for frames that were successfully transmitted on the second try.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

29.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 33. “Programming and Diagnostics”** (DS60001129) in the *“PIC32 Family Reference Manual”*, which are available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MX5XX/6XX/7XX family of devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. Key features include:

- Flexible device configuration
- Watchdog Timer (WDT)
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

29.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- DEVID: Device and Revision ID Register

PIC32MX5XX/6XX/7XX

TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Typical ⁽²⁾	Max.	Units	Conditions		
Power-Down Current (IPD) ⁽¹⁾ for PIC32MX534/564/664/764 Family Devices						
DC40g	12	40	μA	-40°C	2.3V	Base Power-Down Current (Note 6)
DC40h	20	120		+25°C		
DC40i	210	600		+85°C		
DC40o	400	1000		+105°C		
DC40j	20	120		+25°C	3.3V	Base Power-Down Current
DC40k	15	80		-40°C	3.6V	Base Power-Down Current
DC40l	20	120		+25°C		
DC40m	113	350 ⁽⁵⁾		+70°C		
DC40n	220	650		+85°C		
DC40p	500	1000		+105°C		
Module Differential Current for PIC32MX534/564/664/764 Family Devices						
DC41c	—	10	μA	—	2.5V	Watchdog Timer Current: ΔI _{WDT} (Notes 3,6)
DC41d	5	—			3.3V	Watchdog Timer Current: ΔI _{WDT} (Note 3)
DC41e	—	20			3.6V	Watchdog Timer Current: ΔI _{WDT} (Note 3)
DC42c	—	40	μA	—	2.5V	RTCC + Timer1 w/32 kHz Crystal: ΔI _{RTCC} (Notes 3,6)
DC42d	23	—			3.3V	RTCC + Timer1 w/32 kHz Crystal: ΔI _{RTCC} (Note 3)
DC42e	—	50			3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI _{RTCC} (Note 3)
DC43c	—	1300	μA	—	2.5V	ADC: ΔI _{ADC} (Notes 3,4,6)
DC43d	1100	—			3.3V	ADC: ΔI _{ADC} (Notes 3,4)
DC43e	—	1300			3.6V	ADC: ΔI _{ADC} (Notes 3,4)

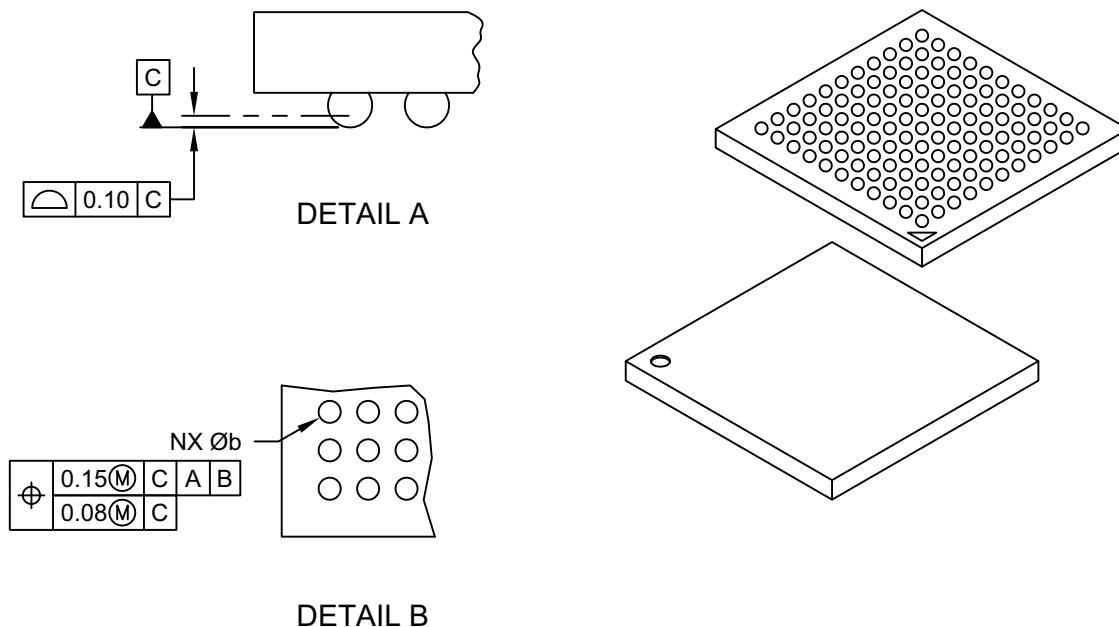
Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0)
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to V_{SS}
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

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121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N	121		
Contact Pitch	e	0.80 BSC		
Overall Height	A	1.00	1.10	1.20
Ball Height	A1	0.25	0.30	0.35
Overall Width	E	10.00 BSC		
Array Width	E1	8.00 BSC		
Overall Length	D	10.00 BSC		
Array Length	D1	8.00 BSC		
Contact Diameter	b	0.35	0.40	0.45

Notes:

1. Ball A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
3. The outer rows and columns of balls are located with respect to datums A and B.
4. Ball interface to package body: 0.37mm nominal diameter.

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