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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx575f256h-80i-pt

FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX534F064H AND PIC32MX534F064L DEVICES

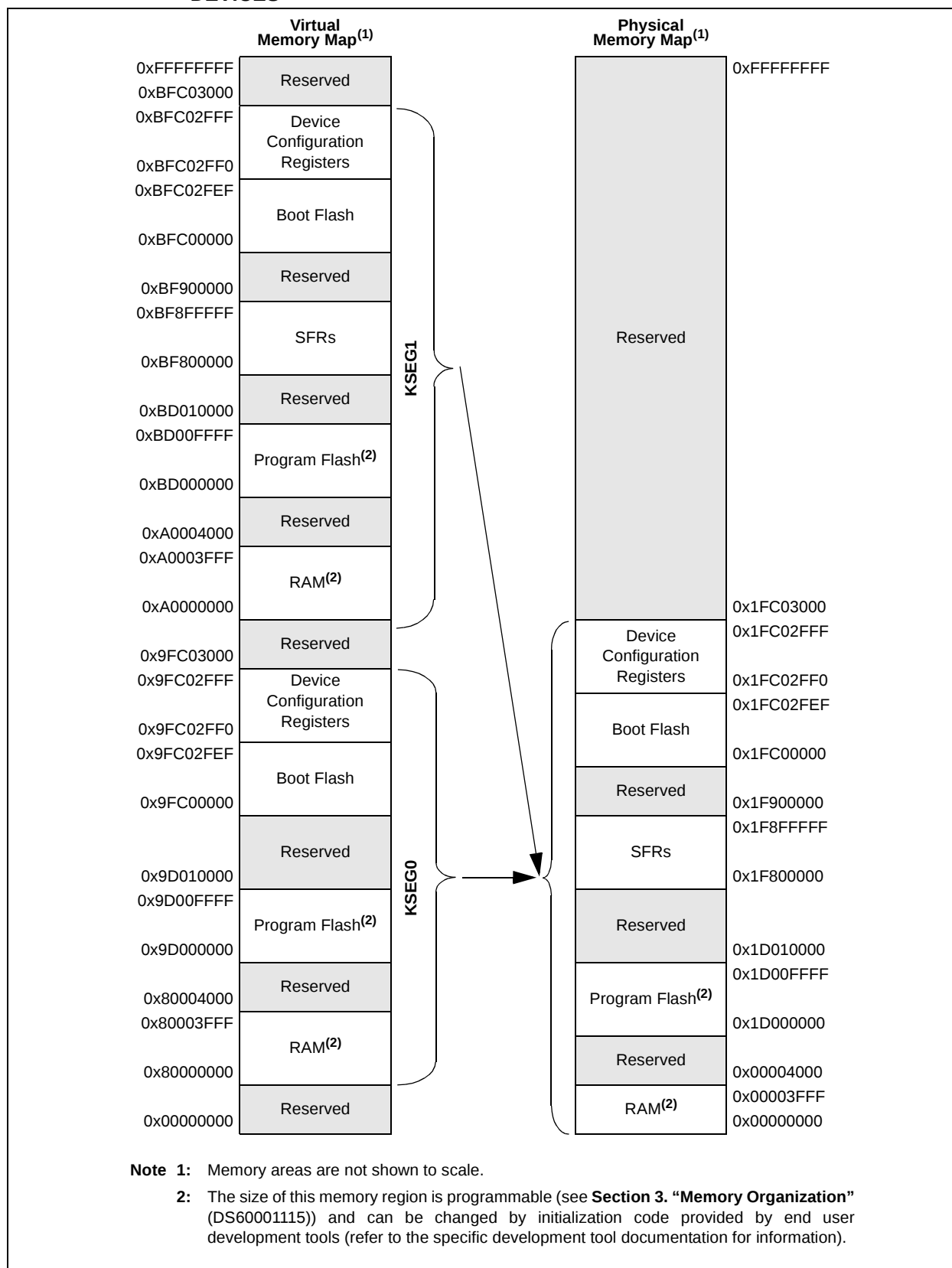


TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000	
3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000	
31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000	
31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000	
31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000	
31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>									0000
31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000	
31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>										00FF
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00		
3200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000	
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000	
3210	DCH2SSA	31:16	CHSSA<31:0>																0000	
		15:0																	0000	
3220	DCH2DSA	31:16	CHDSA<31:0>																0000	
		15:0																	0000	
3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>																0000	
3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000	
3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000	
3260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000	
3270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000	
3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- 2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
 0 = No interrupt is pending
- bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
 0 = No interrupt is pending
- bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a
 pattern match event occurs
 0 = No interrupt is pending
- bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
 0 = No interrupt is pending
- bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
 0 = No interrupt is pending
- bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
 1 = A channel address error has been detected (either the source or the destination address is invalid)
 0 = No interrupt is pending

TABLE 11-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
 - 2: This register does not have associated SET and INV registers.
 - 3: This register does not have associated CLR, SET and INV registers.
 - 4: Reset value for this bit is undefined.

PIC32MX5XX/6XX/7XX

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit
 When TCS = 1:
 1 = External clock input is synchronized
 0 = External clock input is not synchronized
 When TCS = 0:
 This bit is ignored.
- bit 1 **TCS:** Timer Clock Source Select bit
 1 = External clock from TxCKI pin
 0 = Internal peripheral clock
- bit 0 **Unimplemented:** Read as '0'

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

15.1 Control Registers

TABLE 15-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets ⁽²⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	SWDTPS<4:0>					—	WDTCLR	0000

- Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

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REGISTER 21-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2 ⁽¹⁾	CS1 ⁽³⁾	ADDR<13:8>					
	ADDR15 ⁽²⁾	ADDR14 ⁽⁴⁾						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CS2:** Chip Select 2 bit⁽¹⁾

1 = Chip Select 2 is active

0 = Chip Select 2 is inactive

bit 15 **ADDR<15>:** Destination Address bit 15⁽²⁾

bit 14 **CS1:** Chip Select 1 bit⁽³⁾

1 = Chip Select 1 is active

0 = Chip Select 1 is inactive

bit 14 **ADDR<14>:** Destination Address bit 14⁽⁴⁾

bit 13-0 **ADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.

2: When the CSF<1:0> bits (PMCON<7:6>) = 00.

3: When the CSF<1:0> bits (PMCON<7:6>) = 10.

4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

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REGISTER 22-4: RTCDATE: RTC DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<3:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **YEAR10<3:0>**: Binary-Coded Decimal Value of Years bits, 10 digits

bit 27-24 **YEAR01<3:0>**: Binary-Coded Decimal Value of Years bits, 1 digit

bit 23-20 **MONTH10<3:0>**: Binary-Coded Decimal Value of Months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>**: Binary-Coded Decimal Value of Months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>**: Binary-Coded Decimal Value of Days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>**: Binary-Coded Decimal Value of Days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **WDAY01<3:0>**: Binary-Coded Decimal Value of Weekdays bits, 1 digit; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

TABLE 24-2: CAN2 REGISTER SUMMARY FOR PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C100	C2FLTCON4	31:16	FLTEN19	MSEL19<1:0>	FSEL19<4:0>						FLTEN18	MSEL18<1:0>	FSEL18<4:0>						0000
		15:0	FLTEN17	MSEL17<1:0>	FSEL17<4:0>						FLTEN16	MSEL16<1:0>	FSEL16<4:0>						0000
C110	C2FLTCON5	31:16	FLTEN23	MSEL23<1:0>	FSEL23<4:0>						FLTEN22	MSEL22<1:0>	FSEL22<4:0>						0000
		15:0	FLTEN21	MSEL21<1:0>	FSEL21<4:0>						FLTEN20	MSEL20<1:0>	FSEL20<4:0>						0000
C120	C2FLTCON6	31:16	FLTEN27	MSEL27<1:0>	FSEL27<4:0>						FLTEN26	MSEL26<1:0>	FSEL26<4:0>						0000
		15:0	FLTEN25	MSEL25<1:0>	FSEL25<4:0>						FLTEN24	MSEL24<1:0>	FSEL24<4:0>						0000
C130	C2FLTCON7	31:16	FLTEN31	MSEL31<1:0>	FSEL31<4:0>						FLTEN30	MSEL30<1:0>	FSEL30<4:0>						0000
		15:0	FLTEN29	MSEL29<1:0>	FSEL29<4:0>						FLTEN28	MSEL28<1:0>	FSEL28<4:0>						0000
C140	C2RXFn (n = 0-31)	31:16	SID<10:0>										—		EXID	—		EID<17:16>	xxxx
		15:0	EID<15:0>																xxxx
C340	C2FIFOBA	31:16	C2FIFOBA<31:0>																0000
		15:0	C2FIFOBA<31:0>																0000
C350	C2FIFOCONn (n = 0-31)	31:16	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>						0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000	
C360	C2FIFOINTn (n = 0-31)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
C370	C2FIFOUAn (n = 0-31)	31:16	C2FIFOUA<31:0>																0000
		15:0	C2FIFOUA<31:0>																0000
C380	C2FIFOCIn (n = 0-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	C2FIFOCIn<4:0>						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)

- bit 13 **SIDLE:** CAN Stop in Idle bit
 1 = CAN Stops operation when system enters Idle mode
 0 = CAN continues operation when system enters Idle mode
- bit 12 **Unimplemented:** Read as '0'
- bit 11 **CANBUSY:** CAN Module is Busy bit
 1 = The CAN module is active
 0 = The CAN module is completely disabled
- bit 10-5 **Unimplemented:** Read as '0'
- bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
 10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
 10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
 •
 •
 •
 00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
 00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

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REGISTER 24-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN11	MSEL11<1:0>		FSEL11<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN10	MSEL10<1:0>		FSEL10<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN9	MSEL9<1:0>		FSEL9<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN8	MSEL8<1:0>		FSEL8<4:0>				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **FLTEN11:** Filter 11 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 28-24 **FSEL11<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

.

.

.

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN10:** Filter 10 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 20-16 **FSEL10<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

.

.

.

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MX5XX/6XX/7XX

Table 25-1, Table 25-2, Table 25-3 and Table 25-4 show four interfaces and the associated pins that can be used with the Ethernet Controller.

TABLE 25-1: MII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXCLK	Transmit Clock
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
ETXD2	Transmit Data
ETXD3	Transmit Data
ETXERR	Transmit Error
ERXCLK	Receive Clock
ERXDV	Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXD2	Receive Data
ERXD3	Receive Data
ERXERR	Receive Error
ECRS	Carrier Sense
ECOL	Collision Indication

TABLE 25-2: RMII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
EREFCLK	Reference Clock
ECRSDV	Carrier Sense – Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXERR	Receive Error

Note: Ethernet controller pins that are not used by selected interface can be used by other peripherals.

TABLE 25-3: MII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 0)

Pin Name	Description
AEMDC	Management Clock
AEMDIO	Management I/O
AETXCLK	Transmit Clock
AETXEN	Transmit Enable
AETXD0	Transmit Data
AETXD1	Transmit Data
AETXD2	Transmit Data
AETXD3	Transmit Data
AETXERR	Transmit Error
AERXCLK	Receive Clock
AERXDV	Receive Data Valid
AERXD0	Receive Data
AERXD1	Receive Data
AERXD2	Receive Data
AERXD3	Receive Data
AERXERR	Receive Error
AECRS	Carrier Sense
AECOL	Collision Indication

Note: The MII mode Alternate Interface is not available on 64-pin devices.

TABLE 25-4: RMII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 0)

Pin Name	Description
AEMDC	Management Clock
AEMDIO	Management I/O
AETXEN	Transmit Enable
AETXD0	Transmit Data
AETXD1	Transmit Data
AEREFCLK	Reference Clock
AECRSDV	Carrier Sense – Receive Data Valid
AERXD0	Receive Data
AERXD1	Receive Data
AERXERR	Receive Error

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REGISTER 25-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTV<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTV<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	TXRTS	RXEN ⁽¹⁾
7:0	R/W-0	U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
	AUTOFC	—	—	MANFC	—	—	—	BUFCDEC

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **PTV<15:0>**: PAUSE Timer Value bits

PAUSE Timer Value used for Flow Control.

This register should only be written when RXEN (ETHCON1<8>) is not set.

These bits are only used for Flow Control operations.

bit 15 **ON**: Ethernet ON bit

1 = Ethernet module is enabled

0 = Ethernet module is disabled

bit 14 **Unimplemented**: Read as '0'

bit 13 **SIDL**: Ethernet Stop in Idle Mode bit

1 = Ethernet module transfers are paused during Idle mode

0 = Ethernet module transfers continue during Idle mode

bit 12-10 **Unimplemented**: Read as '0'

bit 9 **TXRTS**: Transmit Request to Send bit

1 = Activate the TX logic and send the packet(s) defined in the TX EDT

0 = Stop transmit (when cleared by software) or transmit done (when cleared by hardware)

After the bit is written with a '1', it will clear to a '0' whenever the transmit logic has finished transmitting the requested packets in the Ethernet Descriptor Table (EDT). If a '0' is written by the CPU, the transmit logic finishes the current packet's transmission and then stops any further.

This bit only affects TX operations.

bit 8 **RXEN**: Receive Enable bit⁽¹⁾

1 = Enable RX logic, packets are received and stored in the RX buffer as controlled by the filter configuration

0 = Disable RX logic, no packets are received in the RX buffer

This bit only affects RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

REGISTER 25-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

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REGISTER 25-28: EMAC1MAXF: ETHERNET CONTROLLER MAC MAXIMUM FRAME LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	MACMAXF<15:8> ⁽¹⁾							
7:0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
	MACMAXF<7:0> ⁽¹⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MACMAXF<15:0>:** Maximum Frame Length bits⁽¹⁾

These bits reset to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter/longer maximum length restriction is desired, program this 16-bit field.

Note 1: If a proprietary header is allowed, this bit should be adjusted accordingly. For example, if 4-byte headers are prepended to frames, MACMAXF could be set to 1527 octets. This would allow the maximum VLAN tagged frame plus the 4-byte header.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 25-31: EMAC1MCFG: ETHERNET CONTROLLER MAC MII MANAGEMENT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RESETMGMT	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLKSEL<3:0> ⁽¹⁾				NOPRE	SCANINC

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RESETMGMT:** Test Reset MII Management bit

1 = Reset the MII Management module

0 = Normal Operation

bit 14-6 **Unimplemented:** Read as '0'

bit 5-2 **CLKSEL<3:0>:** MII Management Clock Select 1 bits⁽¹⁾

These bits are used by the clock divide logic in creating the MII Management Clock (MDC), which the IEEE 802.3 Specification defines to be no faster than 2.5 MHz. Some PHYs support clock rates up to 12.5 MHz.

bit 1 **NOPRE:** Suppress Preamble bit

1 = The MII Management will perform read/write cycles without the 32-bit preamble field. Some PHYs support suppressed preamble

0 = Normal read/write cycles are performed

bit 0 **SCANINC:** Scan Increment bit

1 = The MII Management module will perform read cycles across a range of PHYs. The read cycles will start from address 1 through the value set in EMAC1MADR<PHYADDR>

0 = Continuous reads of the same PHY

Note 1: Table 25-7 provides a description of the clock divider encoding.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE 25-7: MIIM CLOCK SELECTION

MIIM Clock Select	EMAC1MCFG<5:2>
SYSCLK divided by 4	000x
SYSCLK divided by 6	0010
SYSCLK divided by 8	0011
SYSCLK divided by 10	0100
SYSCLK divided by 14	0101
SYSCLK divided by 20	0110
SYSCLK divided by 28	0111
SYSCLK divided by 40	1000
Undefined	Any other combination

REGISTER 25-33: EMAC1MADR: ETHERNET CONTROLLER MAC MII MANAGEMENT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	—	—	—	PHYADDR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	REGADDR<4:0>				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **PHYADDR<4:0>:** MII Management PHY Address bits

This field represents the 5-bit PHY Address field of Management cycles. Up to 31 PHYs can be addressed (0 is reserved).

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **REGADDR<4:0>:** MII Management Register Address bits

This field represents the 5-bit Register Address field of Management cycles. Up to 32 registers can be accessed.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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FIGURE 32-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

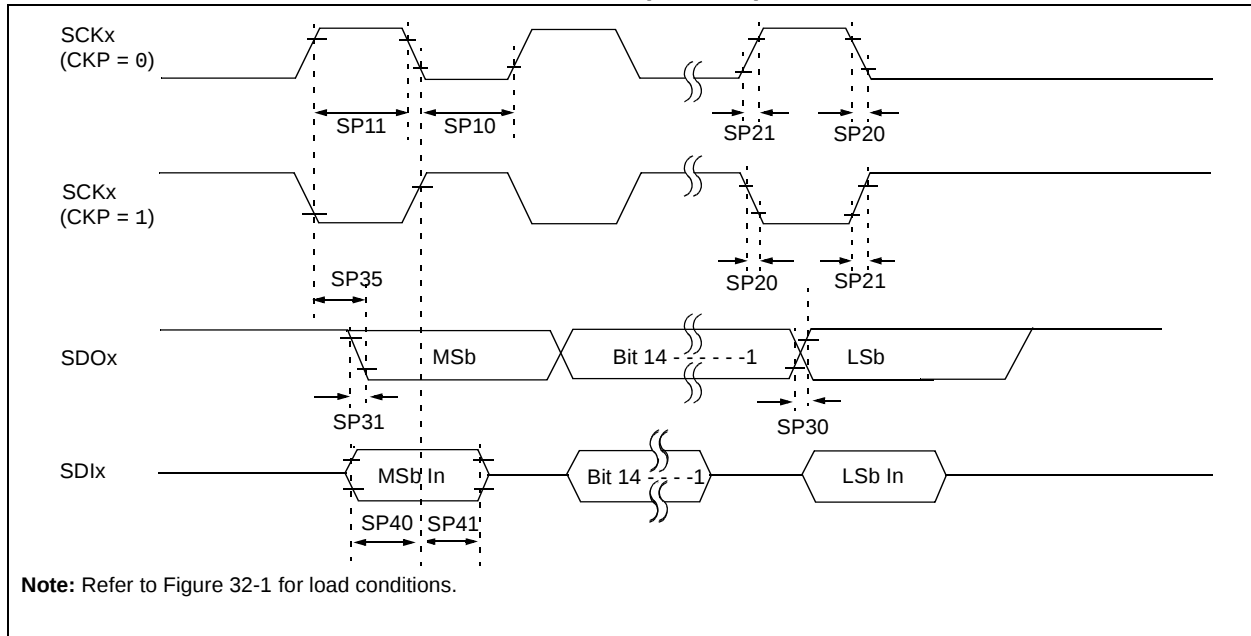


TABLE 32-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)			
				Operating temperature -40°C ≤ Ta ≤ +85°C for Industrial -40°C ≤ Ta ≤ +105°C for V-Temp			
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time ⁽³⁾	Tsck/2	—	—	ns	—
SP11	TscH	SCKx Output High Time ⁽³⁾	Tsck/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—

- Note 1:** These parameters are characterized, but not tested in manufacturing.
- 2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.
- 4:** Assumes 50 pF load on all SPIx pins.

TABLE 32-42: USB OTG ELECTRICAL SPECIFICATIONS

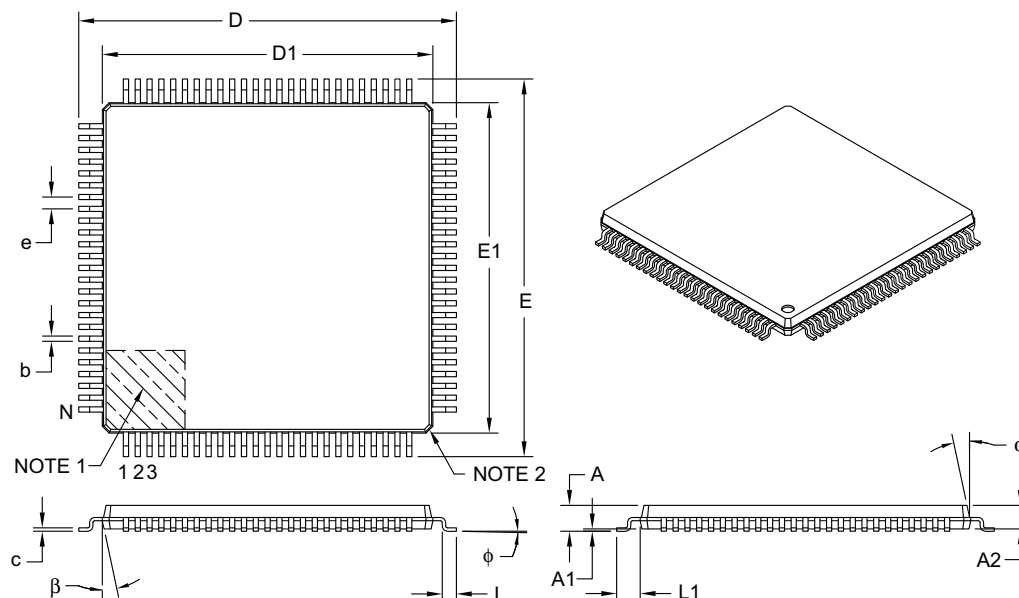
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	—
USB321	Vol	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized, but not tested in manufacturing.

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100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	100		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	16.00 BSC		
Overall Length	D	16.00 BSC		
Molded Package Width	E1	14.00 BSC		
Molded Package Length	D1	14.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B