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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I ² C, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-VQFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx575f256ht-80i-mr |

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)

| | | |
|--|----|-----|
| 121-PIN TFBGA (BOTTOM VIEW) | | L11 |
| PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L | L1 | A11 |
| Note: The TFBGA package skips from row “H” to row “J” and has no “I” row. | | A1 |

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|-------|-----------------------------------|-------|---|
| J3 | PGED2/AN7/RB7 | K8 | VDD |
| J4 | AVDD | K9 | AETXD1/SCK3/U4TX/U1RTS/CN21/RD15 |
| J5 | AN11/ERXERR/AETXERR/PMA12/RB11 | K10 | USBID/RF3 |
| J6 | TCK/RA1 | K11 | SDA3/SDI3/U1RX/RF2 |
| J7 | AN12/ERXD0/AECRS/PMA11/RB12 | L1 | PGEC2/AN6/OCFA/RB6 |
| J8 | No Connect (NC) | L2 | VREF-/CVREF-/AERXD2/PMA7/RA9 |
| J9 | No Connect (NC) | L3 | AVss |
| J10 | SCL3/SDO3/U1TX/RF8 | L4 | AN9/C2OUT/RB9 |
| J11 | D-/RG3 | L5 | AN10/CVREFOUT/PMA13/RB10 |
| K1 | PGEC1/AN1/CN3/RB1 | L6 | SCK4/U5TX/U2RTS/RF13 |
| K2 | PGED1/AN0/CN2/RB0 | L7 | AN13/ERXD1/AECOL/PMA10/RB13 |
| K3 | VREF+/CVREF+/AERXD3/PMA6/RA10 | L8 | AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15 |
| K4 | AN8/C1OUT/RB8 | L9 | AETXD0/SS3/U4RX/U1CTS/CN20/RD14 |
| K5 | No Connect (NC) | L10 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| K6 | SS4/U5RX/U2CTS/RF12 | L11 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 |
| K7 | AN14/ERXD2/AETXD3/PMALH/PMA1/RB14 | | |

Note 1: Shaded pins are 5V tolerant.

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

| Register Number | Register Name | Function |
|-----------------|-------------------------|--|
| 0-6 | Reserved | Reserved. |
| 7 | HWREna | Enables access via the RDHWR instruction to selected hardware registers. |
| 8 | BadVAddr ⁽¹⁾ | Reports the address for the most recent address-related exception. |
| 9 | Count ⁽¹⁾ | Processor cycle count. |
| 10 | Reserved | Reserved. |
| 11 | Compare ⁽¹⁾ | Timer interrupt control. |
| 12 | Status ⁽¹⁾ | Processor status and control. |
| 12 | IntCtl ⁽¹⁾ | Interrupt system status and control. |
| 12 | SRSCtl ⁽¹⁾ | Shadow register set status and control. |
| 12 | SRSMap ⁽¹⁾ | Provides mapping from vectored interrupt to a shadow set. |
| 13 | Cause ⁽¹⁾ | Cause of last general exception. |
| 14 | EPC ⁽¹⁾ | Program counter at last exception. |
| 15 | PRId | Processor identification and revision. |
| 15 | Ebase | Exception vector base register. |
| 16 | Config | Configuration register. |
| 16 | Config1 | Configuration Register 1. |
| 16 | Config2 | Configuration Register 2. |
| 16 | Config3 | Configuration Register 3. |
| 17-22 | Reserved | Reserved. |
| 23 | Debug ⁽²⁾ | Debug control and exception status. |
| 24 | DEPC ⁽²⁾ | Program counter at last debug exception. |
| 25-29 | Reserved | Reserved. |
| 30 | ErrorEPC ⁽¹⁾ | Program counter at last error. |
| 31 | DESAVE ⁽²⁾ | Debug handler scratchpad register. |

Note 1: Registers used in exception processing.

2: Registers used during debug.

PIC32MX5XX/6XX/7XX

REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |
| | BMXDUDBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXDUDBA<7:0> | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUDBA<15:10>:** DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 **BMXDUDBA<9:0>:** DRM User Data Base Address Read-Only bits

Value is always '0', which forces 1 KB increments

- Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.
- 2:** The value in this register must be less than or equal to BMXDRMSZ.

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REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|-------------------------|----------------|----------------|--------------------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | RIPL<2:0> ⁽¹⁾ | | |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | VEC<5:0> ⁽¹⁾ | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **RIPL<2:0>:** Requested Priority Level bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits⁽¹⁾

11111-00000 = The interrupt vector that is presented to the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single-vector mode.

REGISTER 7-3: TPTMR: TEMPORAL PROXIMITY TIMER REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<7:0> | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **TPTMR<31:0>:** Temporal Proximity Timer Reload bits

Used by the Temporal Proximity Timer as a reload value when the Temporal Proximity timer is triggered by an interrupt event.

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REGISTER 11-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | U-0 | R/WC-0, HS |
| | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF |

| | | |
|-------------------|-------------------------|--|
| Legend: | WC = Write '1' to clear | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit

- 1 = Change in ID state detected
- 0 = No change in ID state detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit

- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit

- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit

- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit

- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit

- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit

- 1 = Change on the session valid input detected
- 0 = No change on the session valid input detected

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REGISTER 11-11: U1CON: USB CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|---|----------------|-----------------------|-----------------------|---------------|--|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-x | R-x | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | JSTATE | SE0 | PKTDIS ⁽⁴⁾ TOKBUSY ^(1,5) | USBRST | HOSTEN ⁽²⁾ | RESUME ⁽³⁾ | PPBRST | USBEN ⁽⁴⁾ SOFEN ⁽⁵⁾ |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit

1 = JSTATE was detected on the USB

0 = JSTATE was not detected

bit 6 **SE0:** Live Single-Ended Zero flag bit

1 = Single-ended zero was detected on the USB

0 = Single-ended zero was not detected

bit 5 **PKTDIS:** Packet Transfer Disable bit⁽⁴⁾

1 = Token and packet processing disabled (set upon SETUP token received)

0 = Token and packet processing enabled

TOKBUSY: Token Busy Indicator bit^(1,5)

1 = Token being executed by the USB module

0 = No token being executed

bit 4 **USBRST:** Module Reset bit⁽⁵⁾

1 = USB reset is generated

0 = USB reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit⁽²⁾

1 = USB host capability is enabled

0 = USB host capability is disabled

bit 2 **RESUME:** RESUME Signaling Enable bit⁽³⁾

1 = RESUME signaling is activated

0 = RESUME signaling is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).

2: All host control logic is reset any time that the value of this bit is toggled.

3: Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.

4: Device mode.

5: Host mode.

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REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 8 **TRMT**: Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer
- bit 7-6 **URXISEL<1:0>**: Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (has at least 1 data character)
- bit 5 **ADDEN**: Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode is disabled
- bit 4 **RIDLE**: Receiver Idle bit (read-only)
1 = Receiver is idle
0 = Data is being received
- bit 3 **PERR**: Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected
- bit 2 **FERR**: Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected
- bit 1 **OERR**: Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to an empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed
- bit 0 **URXDA**: Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

TABLE 24-2: CAN2 REGISTER SUMMARY FOR PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

| Virtual Address (BF88_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets | | |
|-----------------------------|---------------------------------|-----------|----------------|-------------|-------------|-------------|----------|-------------|------------|----------|----------|--------------|-------------|------------|----------|-------------|-------------|----------|------------|------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | | | |
| C000 | C2CON | 31:16 | — | — | — | — | ABAT | REQOP<2:0> | | | | OPMOD<2:0> | | | CANCAP | — | — | — | — | 0480 | |
| | | 15:0 | ON | — | SIDLE | — | CANBUSY | — | — | — | — | — | — | DNCNT<4:0> | | | | 0000 | | | |
| C010 | C2CFG | 31:16 | — | — | — | — | — | — | — | — | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | | 0000 | |
| | | 15:0 | SEG2PHTS | SAM | SEG1PH<2:0> | | | | PRSEG<2:0> | | | SJW<1:0> | | BRP<5:0> | | | | | | 0000 | |
| C020 | C2INT | 31:16 | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE | 0000 | | |
| | | 15:0 | IVRIF | WAKIF | CERRIF | SERRIF | RBOVIF | — | — | — | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF | 0000 | | |
| C030 | C2VEC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | | |
| | | 15:0 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 | | |
| C040 | C2TREC | 31:16 | — | — | — | — | — | — | — | — | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN | 0000 | | |
| | | 15:0 | TERRCNT<7:0> | | | | | | | | | RERRCNT<7:0> | | | | | | | | | 0000 |
| C050 | C2FSTAT | 31:16 | FIFOIP31 | FIFOIP30 | FIFOIP29 | FIFOIP28 | FIFOIP27 | FIFOIP26 | FIFOIP25 | FIFOIP24 | FIFOIP23 | FIFOIP22 | FIFOIP21 | FIFOIP20 | FIFOIP19 | FIFOIP18 | FIFOIP17 | FIFOIP16 | 0000 | | |
| | | 15:0 | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 | 0000 | | |
| C060 | C2RXOVF | 31:16 | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 | 0000 | | |
| | | 15:0 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 | | |
| C070 | C2TMR | 31:16 | CANTS<15:0> | | | | | | | | | | | | | | | | | 0000 | |
| | | 15:0 | CANTSPRE<15:0> | | | | | | | | | | | | | | | | 0000 | | |
| C080 | C2RXM0 | 31:16 | SID<10:0> | | | | | | | | | | | — | MIDE | — | EID<17:16> | | | xxxx | |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx | | |
| C0A0 | C2RXM1 | 31:16 | SID<10:0> | | | | | | | | | | | — | MIDE | — | EID<17:16> | | | xxxx | |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx | | |
| C0B0 | C2RXM2 | 31:16 | SID<10:0> | | | | | | | | | | | — | MIDE | — | EID<17:16> | | | xxxx | |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx | | |
| C0B0 | C2RXM3 | 31:16 | SID<10:0> | | | | | | | | | | | — | MIDE | — | EID<17:16> | | | xxxx | |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx | | |
| C0C0 | C2FLTCON0 | 31:16 | FLTEN3 | MSEL3<1:0> | | | | FSEL3<4:0> | | | | FLTEN2 | MSEL2<1:0> | | | | FSEL2<4:0> | | | | 0000 |
| | | 15:0 | FLTEN1 | MSEL1<1:0> | | | | FSEL1<4:0> | | | | FLTEN0 | MSEL0<1:0> | | | | FSEL0<4:0> | | | | 0000 |
| C0D0 | C2FLTCON1 | 31:16 | FLTEN7 | MSEL7<1:0> | | | | FSEL7<4:0> | | | | FLTEN6 | MSEL6<1:0> | | | | FSEL6<4:0> | | | | 0000 |
| | | 15:0 | FLTEN5 | MSEL5<1:0> | | | | FSEL5<4:0> | | | | FLTEN4 | MSEL4<1:0> | | | | FSEL4<4:0> | | | | 0000 |
| C0E0 | C2FLTCON2 | 31:16 | FLTEN11 | MSEL11<1:0> | | | | FSEL11<4:0> | | | | FLTEN10 | MSEL10<1:0> | | | | FSEL10<4:0> | | | | 0000 |
| | | 15:0 | FLTEN9 | MSEL9<1:0> | | | | FSEL9<4:0> | | | | FLTEN8 | MSEL8<1:0> | | | | FSEL8<4:0> | | | | 0000 |
| C0F0 | C2FLTCON3 | 31:16 | FLTEN15 | MSEL15<1:0> | | | | FSEL15<4:0> | | | | FLTEN14 | MSEL14<1:0> | | | | FSEL14<4:0> | | | | 0000 |
| | | 15:0 | FLTEN13 | MSEL13<1:0> | | | | FSEL13<4:0> | | | | FLTEN12 | MSEL12<1:0> | | | | FSEL12<4:0> | | | | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

REGISTER 24-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)

- bit 9 **TXHALFIF**: FIFO Transmit FIFO Half Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 1 = FIFO is \leq half full
 0 = FIFO is $>$ half full
 TXEN = 0: (FIFO configured as a receive buffer)
 Unused, reads '0'
- bit 8 **TXEMPTYIF**: Transmit FIFO Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 1 = FIFO is empty
 0 = FIFO is not empty, at least 1 message queued to be transmitted
 TXEN = 0: (FIFO configured as a receive buffer)
 Unused, reads '0'
- bit 7-4 **Unimplemented**: Read as '0'
- bit 3 **RXOVFLIF**: Receive FIFO Overflow Interrupt Flag bit
 TXEN = 1: (FIFO configured as a transmit buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a receive buffer)
 1 = Overflow event has occurred
 0 = No overflow event occurred
- bit 2 **RXFULLIF**: Receive FIFO Full Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a receive buffer)
 1 = FIFO is full
 0 = FIFO is not full
- bit 1 **RXHALFIF**: Receive FIFO Half Full Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a receive buffer)
 1 = FIFO is \geq half full
 0 = FIFO is $<$ half full
- bit 0 **RXEMPTYIF**: Receive Buffer Not Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a receive buffer)
 1 = FIFO is not empty, has at least 1 message
 0 = FIFO is empty

Note 1: This bit is read-only and reflects the status of the FIFO.

REGISTER 25-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)

bit 7 **AUTOFC:** Automatic Flow Control bit

1 = Automatic Flow Control is enabled

0 = Automatic Flow Control is disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **MANFC:** Manual Flow Control bit

1 = Manual Flow Control is enabled

0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every $128 * PTV<15:0>/2$ TX clock cycles until the bit is cleared.

Note: For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **BUFCDEC:** Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

This bit is only used for RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

REGISTER 25-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|------------------------|-----------------------|-----------------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BUFCNT<7:0> | | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ETHBUSY ⁽¹⁾ | TXBUSY ⁽²⁾ | RXBUSY ⁽²⁾ | — | — | — | — | — |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>)) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

Note: BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ETHBUSY:** Ethernet Module busy bit⁽¹⁾

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction

0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

bit 6 **TXBUSY:** Transmit Busy bit⁽²⁾

1 = TX logic is receiving data

0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

Note 1: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.

2: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

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REGISTER 25-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER (CONTINUED)

bit 5 **RXBUSY:** Receive Busy bit⁽²⁾

1 = RX logic is receiving data

0 = RX logic is idle

This bit indicates that a packet is currently being received. A change in this status bit is not necessarily reflected by the RXDONE interrupt, as RX packets may be aborted or rejected by the RX filter.

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.

2: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

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TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE}) (CONTINUED)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp | | | |
|--|------------------------|------|--|---------------------|------|----------------------------------|
| Parameter No. | Typical ⁽²⁾ | Max. | Units | Conditions | | |
| Idle Current (I _{IDLE}) ⁽¹⁾ for PIC32MX534/564/664/764 Family Devices | | | | | | |
| DC30a | 1.5 | 5 | mA | -40°C, +25°C, +85°C | — | 4 MHz |
| DC30c | 3.5 | 6 | | +105°C | | |
| DC31a | 7 | 11 | | -40°C, +25°C, +85°C | | |
| DC32a | 13 | 20 | mA | -40°C, +25°C, +85°C | — | 60 MHz (Note 3) |
| DC33a | 17 | 25 | mA | -40°C, +25°C, +85°C | — | 80 MHz |
| DC33c | 20 | 27 | | +105°C | | |
| DC34c | — | 40 | μA | -40°C | 2.3V | LPRC (31 kHz) (Note 3) |
| DC34d | | 75 | | +25°C | | |
| DC34e | | 800 | | +85°C | | |
| DC34f | | 1000 | | +105°C | | |
| DC35c | 30 | — | μA | -40°C | 3.3V | |
| DC35d | 55 | | | +25°C | | |
| DC35e | 230 | | | +85°C | | |
| DC35f | 800 | | | +105°C | | |
| DC36c | — | 43 | μA | -40°C | 3.6V | |
| DC36d | | 106 | | +25°C | | |
| DC36e | | 800 | | +85°C | | |
| DC36f | | 1000 | | +105°C | | |

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0)
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to V_{SS}
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
- 2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** This parameter is characterized, but not tested in manufacturing.
- 4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

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TABLE 32-13: COMPARATOR SPECIFICATIONS

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 3): 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|--------------------|--------|------------------------------------|--|---------|------|-------|--|
| Param. No. | Symbol | Characteristics | Min. | Typical | Max. | Units | Comments |
| D300 | VIOFF | Input Offset Voltage | — | ±7.5 | ±25 | mV | AVDD = VDD, AVSS = VSS |
| D301 | VICM | Input Common Mode Voltage | 0 | — | VDD | V | AVDD = VDD, AVSS = VSS (Note 2) |
| D302 | CMRR | Common Mode Rejection Ratio | 55 | — | — | dB | Max VICM = (VDD - 1)V (Note 2) |
| D303 | TRESP | Response Time | — | 150 | 400 | ns | AVDD = VDD, AVSS = VSS (Notes 1, 2) |
| D304 | ON2OV | Comparator Enabled to Output Valid | — | — | 10 | μs | Comparator module is configured before setting the comparator ON bit (Note 2) |
| D305 | IVREF | Internal Voltage Reference | 0.57 | 0.6 | 0.63 | V | For devices without BGSEL<1:0> |
| | | | 1.14 | 1.2 | 1.26 | V | BGSEL<1:0> = 00 |
| | | | 0.57 | 0.6 | 0.63 | V | BGSEL<1:0> = 01 |

Note 1: Response time measured with one comparator input at $(VDD - 1.5)/2$, while the other input transitions from VSS to VDD.

2: These parameters are characterized but not tested.

3: The Comparator module is functional at $VBOR_{MIN} < VDD < VDD_{MIN}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 32-9: OCx/PWM MODULE TIMING CHARACTERISTICS

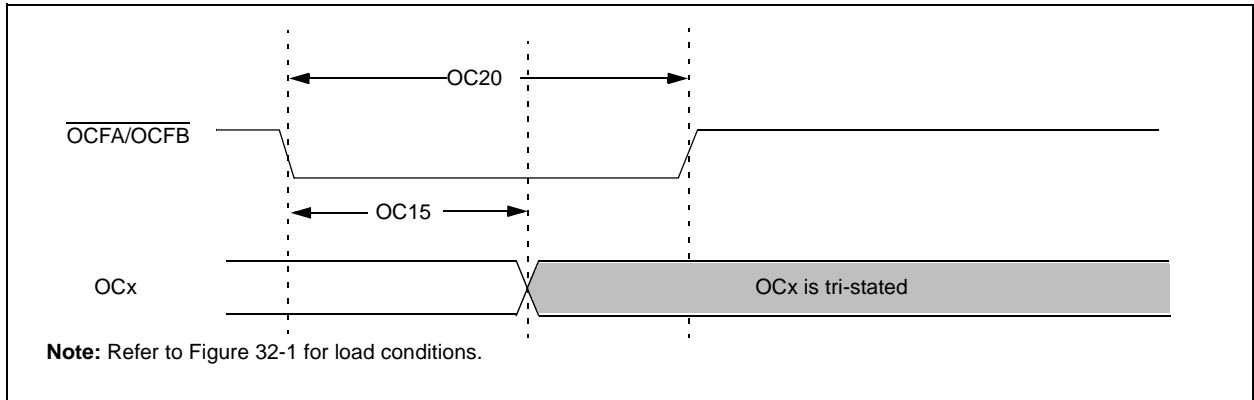


TABLE 32-27: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|--------------------|------------------|--------------------------------|---|------------------------|-----|-------|------------|
| Param No. | Symbol | Characteristics ⁽¹⁾ | Min | Typical ⁽²⁾ | Max | Units | Conditions |
| OC15 | T _{FD} | Fault Input to PWM I/O Change | — | — | 50 | ns | — |
| OC20 | T _{FLT} | Fault Input Pulse Width | 50 | — | — | ns | — |

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|--------------------|----------------------|---|---|------------------------|------|-------|------------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | Min. | Typical ⁽²⁾ | Max. | Units | Conditions |
| SP51 | TssH2doZ | \overline{SSx} ↑ to SDOx Output High-Impedance ⁽⁴⁾ | 5 | — | 25 | ns | — |
| SP52 | Tsch2ssH TscL2ssH | \overline{SSx} ↑ after SCKx Edge | Tsck + 20 | — | — | ns | — |
| SP60 | TssL2doV | SDOx Data Output Valid after \overline{SSx} Edge | — | — | 25 | ns | — |

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 32-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

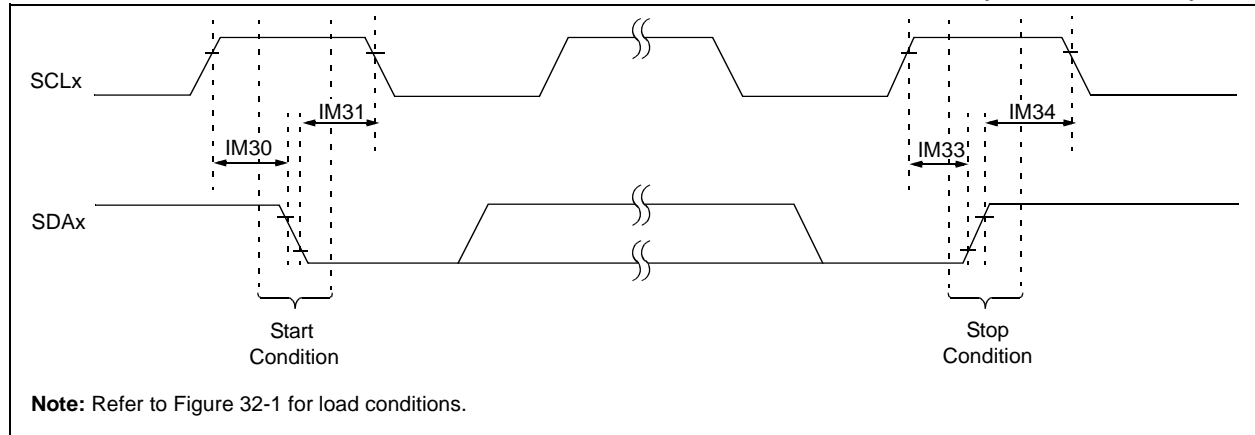
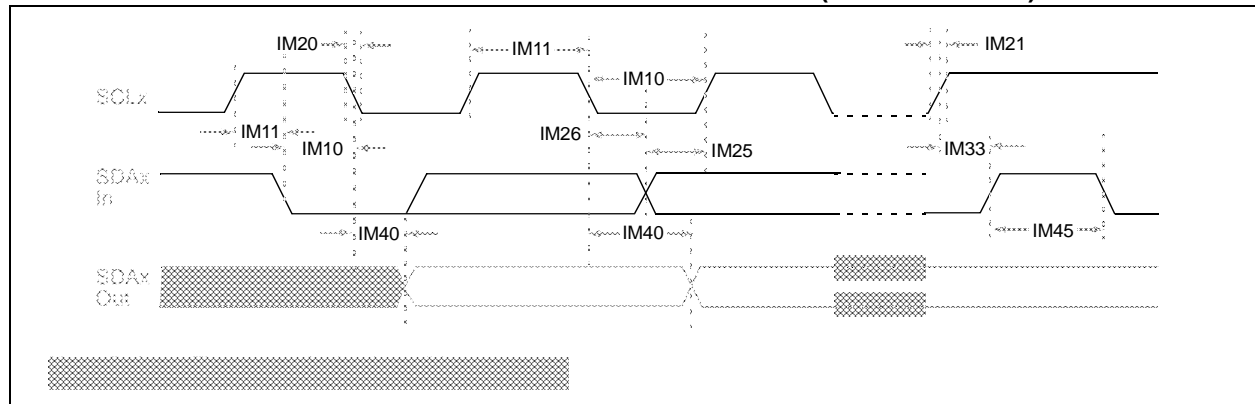


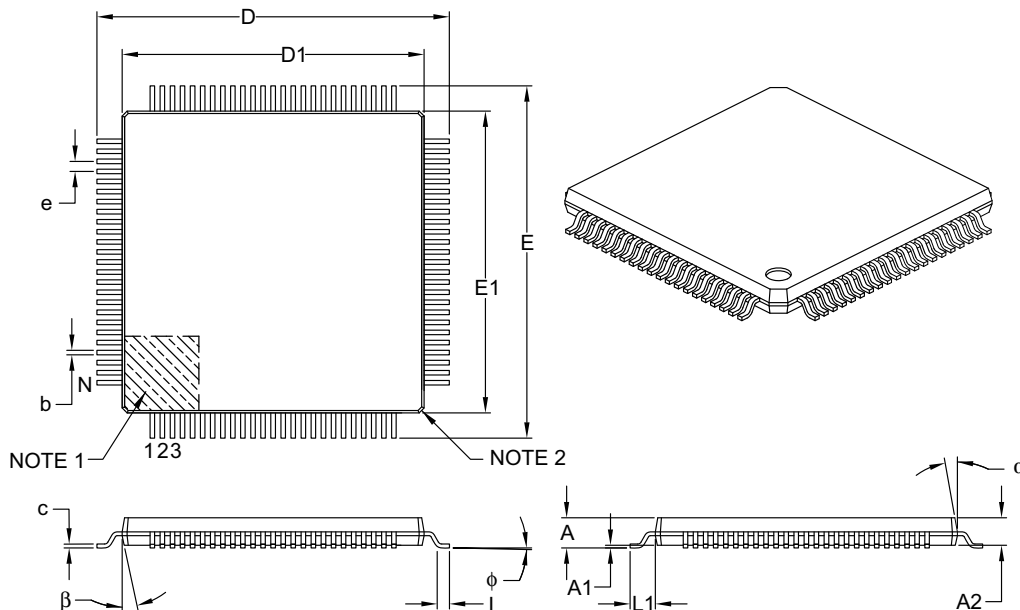
FIGURE 32-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



PIC32MX5XX/6XX/7XX

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packages>



| Units | | MILLIMETERS | | |
|--------------------------|----------|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | 100 | | |
| Lead Pitch | e | 0.40 BSC | | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | 1.00 REF | | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | 14.00 BSC | | |
| Overall Length | D | 14.00 BSC | | |
| Molded Package Width | E1 | 12.00 BSC | | |
| Molded Package Length | D1 | 12.00 BSC | | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.13 | 0.18 | 0.23 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

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