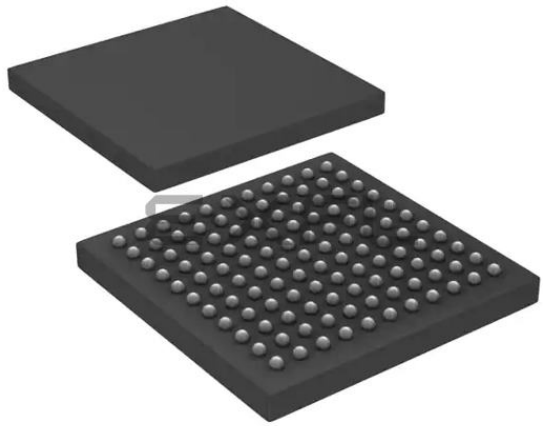
# Microchip Technology - PIC32MX575F256L-80V/BG Datasheet



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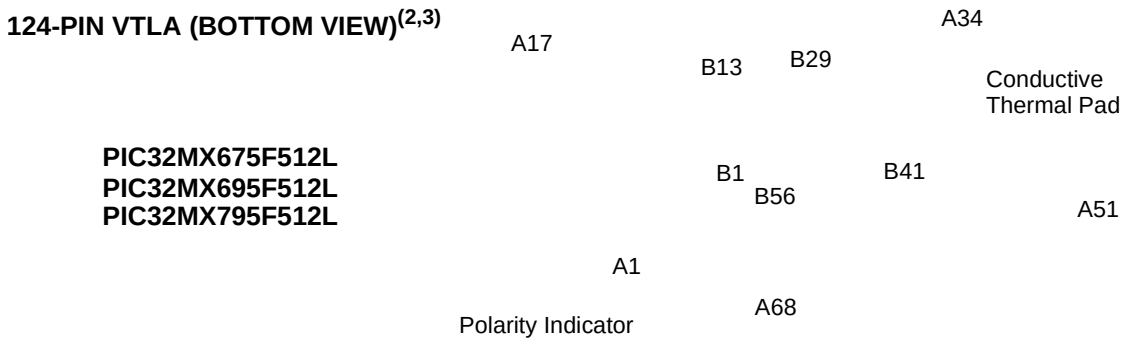
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | - |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-TFBGA |
| Supplier Device Package | 121-TFBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx575f256l-80v-bg |

**TABLE 13: PIN NAMES FOR 124-PIN USB, ETHERNET, AND CAN DEVICES (CONTINUED)**

**124-PIN VTLA (BOTTOM VIEW)(2,3)**




| Package Bump # | Full Pin Name | Package Bump # | Full Pin Name |
|---|---|---|---|
| B8 | VSS | B33 | TDO/RA5 |
| B9 | TMS/RA0 | B34 | OSC1/CLKI/RC12 |
| B10 | AERXD1/INT2/RE9 | B35 | No Connect (NC) |
| B11 | AN4/C1IN-/CN6/RB4 | B36 | AETXCLK/SCL1/INT3/RA14 |
| B12 | VSS | B37 | RTCC/EMDIO/AEMDIO/IC1/RD8 |
| B13 | AN2/C2IN-/CN4/RB2 | B38 | SCK1/IC3/PMCS2/PMA15/RD10 |
| B14 | PGED1/AN0/CN2/RB0 | B39 | SDO1/OC1/INT0/RD0 |
| B15 | No Connect (NC) | B40 | SOSCO/T1CK/CN0/RC14 |
| B16 | PGED2/AN7/RB7 | B41 | VSS |
| B17 | VREF+/CVREF+/AERXD3/PMA6/RA10 | B42 | OC3/RD2 |
| B18 | AVSS | B43 | ETXD2/IC5/PMD12/RD12 |
| B19 | AN9/C2OUT/RB9 | B44 | OC5/PMWR/CN13/RD4 |
| B20 | AN11/ERXERR/AETXERR/PMA12/RB11 | B45 | ETXEN/PMD14/CN15/RD6 |
| B21 | VDD | B46 | VSS |
| B22 | AC1TX/SCK4/U5TX/U2RTS/RF13 | B47 | No Connect (NC) |
| B23 | AN12/ERXD0/AECRS/PMA11/RB12 | B48 | VCAP |
| B24 | AN14/ERXD2/AETXD3/PMALH/PMA1/RB14 | B49 | C1RX(1)/ETXD1/PMD11/RF0 |
| B25 | VSS | B50 | C2TX(1)/ETXERR/PMD9/RG1 |
| B26 | AETXD0/SS3/U4RX/U1CTS/CN20/RD14 | B51 | TRCLK/RA6 |
| B27 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 | B52 | PMD0/RE0 |
| B28 | No Connect (NC) | B53 | VDD |
| B29 | SCL3/SDO3/U1TX/RF8 | B54 | TRD2/RG14 |
| B30 | VUSB3V3 | B55 | TRD0/RG13 |
| B31 | D+/RG2 | B56 | PMD3/RE3 |

**Note 1:** This pin is only available on PIC32MX795F512L devices.
**2:** Shaded package bumps are 5V tolerant.
**3:** It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

## 1.0 DEVICE OVERVIEW

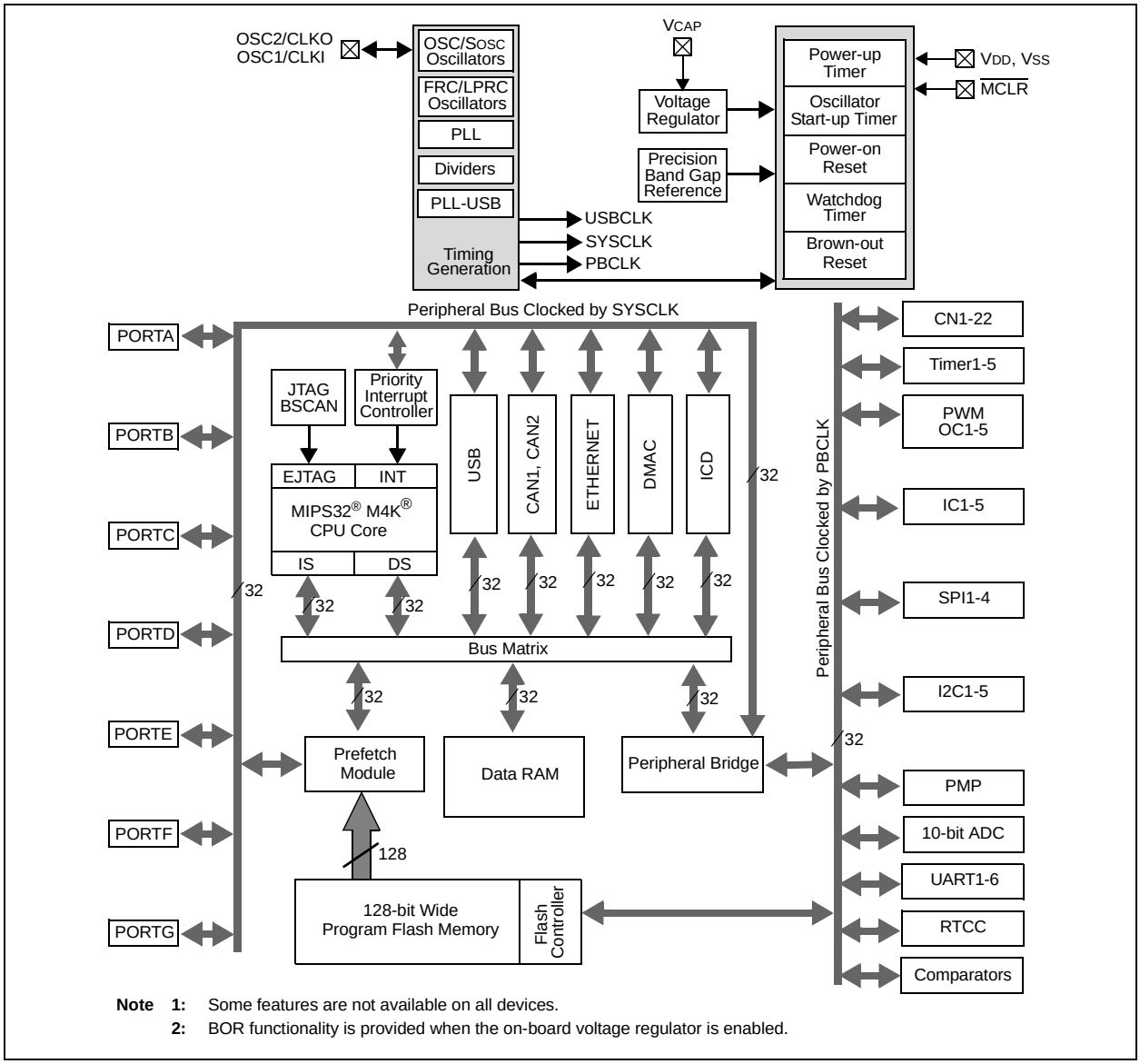
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX5XX/6XX/7XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX5XX/6XX/7XX family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: BLOCK DIAGRAM(1,2)**




**Note 1:** Some features are not available on all devices.
**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB® REAL ICE™.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) (DS50001765)
- *"MPLAB® ICD 3 Design Advisory"* (DS50001764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide" (*DS50001616)
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) (DS50001749)

## 2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

## 2.7 Trace

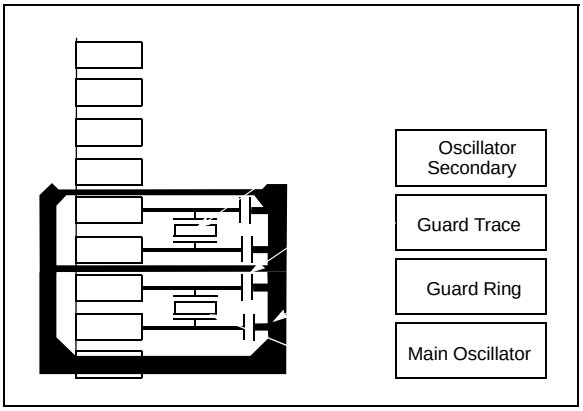
The trace pins can be connected to a hardware-trace-enabled programmer to provide a compress real time instruction trace. When used for trace the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22Ω series resistor between the trace pins and the trace connector.

## 2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. Refer to **Section 8.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

**FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT**



**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | R/W-y | R/W-y | R/W-y | R/W-0 | R/W-0 | R/W-1 |
| | — | — | PLLODIV<2:0> | | | FRCDIV<2:0> | | |
| 23:16 | U-0 | R-0 | R-1 | R/W-y | R/W-y | R/W-y | R/W-y | R/W-y |
| | — | SOSCRDY | PBDIVRDY | PBDIV<1:0> | | PLLMULT<2:0> | | |
| 15:8 | U-0 | R-0 | R-0 | R-0 | U-0 | R/W-y | R/W-y | R/W-y |
| | — | COSC<2:0> | | | — | NOSC<2:0> | | |
| 7:0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-y | R/W-0 |
| | CLKLOCK | ULOCK | SLOCK | SLPEN | CF | UFRCEN | SOSCEN | OSWEN |

| **Legend:** | y = Value set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

111 = PLL output divided by 256
110 = PLL output divided by 64
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 1

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2 (default setting)
000 = FRC divided by 1

bit 23 **Unimplemented:** Read as '0'

bit 22 **SOSCRDY:** Secondary Oscillator (SOSC) Ready Indicator bit

1 = Indicates that the Secondary Oscillator is running and is stable
0 = Secondary Oscillator is still warming up or is turned off

bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit

1 = PBDIV<1:0> bits can be written
0 = PBDIV<1:0> bits cannot be written

bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits

11 = PBCLK is SYSCLK divided by 8 (default)
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

## 9.0 PREFETCH CACHE

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Prefetch Cache"** (DS60001119) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

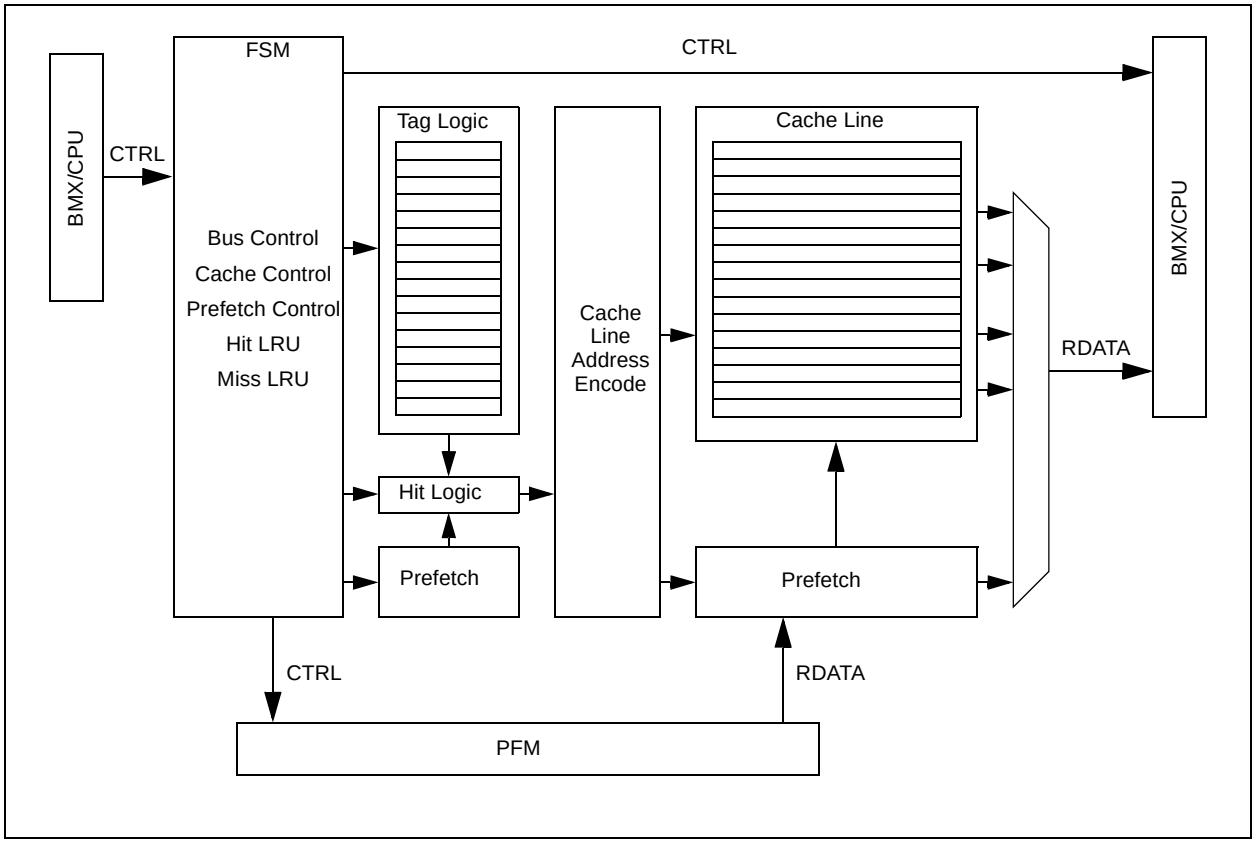
Prefetch cache increases performance for applications executing out of the cacheable program Flash memory regions by implementing instruction caching, constant data caching and instruction prefetching.

### 9.1 Features

- 16 fully-associative lockable cache lines
- 16-byte cache lines
- Up to four cache lines allocated to data
- Two cache lines with address mask to hold repeated instructions
- Pseudo-LRU replacement policy
- All cache lines are software writable
- 16-byte parallel memory fetch
- Predictive instruction prefetch

A simplified block diagram of the Prefetch Cache module is illustrated in Figure 9-1.

**FIGURE 9-1: PREFETCH CACHE MODULE BLOCK DIAGRAM**



**REGISTER 9-8: CHEW3: CACHE WORD 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW3<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW3<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW3<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW3<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEW3<31:0>:** Word 3 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
Readable only if the device is not code-protected.

**Note:** This register is a window into the cache data array and is only readable if the device is not code-protected.

**REGISTER 9-9: CHELRU: CACHE LRU REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 |
| | — | — | — | — | — | — | — | CHELRU<24> |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHELRU<23:16> | | | | | | | |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHELRU<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHELRU<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-25 **Unimplemented:** Write '0'; ignore read

bit 24-0 **CHELRU<24:0>:** Cache Least Recently Used State Encoding bits
Indicates the pseudo-LRU state of the cache.

**REGISTER 10-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.
**Note:** This must be the physical address of the source.

**REGISTER 10-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.
**Note:** This must be the physical address of the destination.

## 13.0 TIMER1

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the low-power Secondary Oscillator (SOSC) for Real-Time Clock (RTC) applications. The following modes are supported:

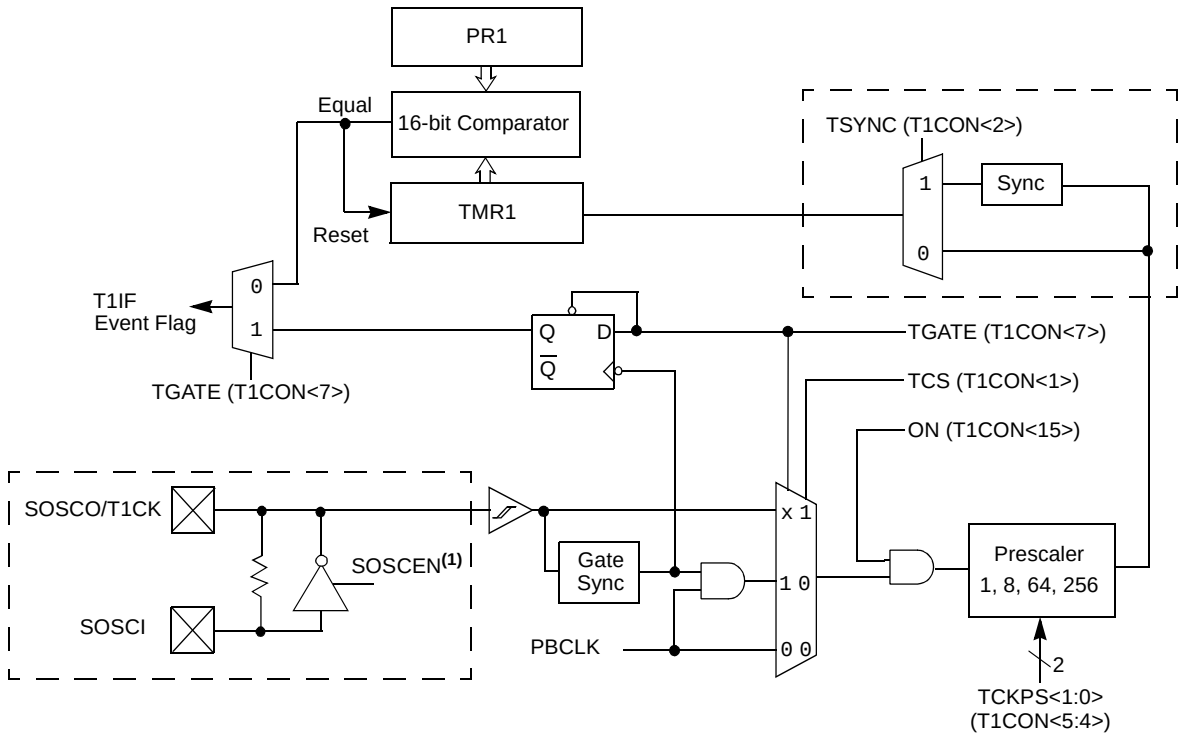
- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

## 13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the SOSC to function as a Real-Time Clock (RTC)

A simplified block diagram of the Timer1 module is illustrated in Figure 13-1.

**FIGURE 13-1: TIMER1 BLOCK DIAGRAM**




**Note 1:** The default state of the SOSCEN (OSCCON<1>) during a device Reset is controlled by the FSOSCEN bit in Configuration Word, DEVCFG1.

**REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)**

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(2)

11111111 = Alarm will trigger 256 times

•

•

•

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

**Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

**2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

**3:** This assumes a CPU read will execute in less than 32 PBCLKs.

| **Note:** | This register is only reset on a Power-on Reset (POR). |
|---|---|

**TABLE 23-1: ADC REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9120 | ADC1BUFB | 31:16 | ADC Result Word B (ADC1BUFB<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9130 | ADC1BUFC | 31:16 | ADC Result Word C (ADC1BUFC<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9140 | ADC1BUFD | 31:16 | ADC Result Word D (ADC1BUFD<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9150 | ADC1BUFE | 31:16 | ADC Result Word E (ADC1BUFE<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9160 | ADC1BUFF | 31:16 | ADC Result Word F (ADC1BUFF<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**REGISTER 24-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5 (CONTINUED)**

bit 15 **FLTEN21:** Filter 21 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL21<1:0>:** Filter 21 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL21<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN20:** Filter 20 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL20<1:0>:** Filter 20 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL20<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXNEMPTYIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | TXNFULLIF(1) | TXHALFIF | TXEMPTYIF(1) |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | RXOVFLIF | RXFULLIF(1) | RXHALFIF(1) | RXNEMPTYIF(1) |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

**Note 1:** This bit is read-only and reflects the status of the FIFO.

Table 25-1, Table 25-2, Table 25-3 and Table 25-4 show four interfaces and the associated pins that can be used with the Ethernet Controller.

**TABLE 25-1: MII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 1)**

| Pin Name | Description |
|---|---|
| EMDC | Management Clock |
| EMDIO | Management I/O |
| ETXCLK | Transmit Clock |
| ETXEN | Transmit Enable |
| ETXD0 | Transmit Data |
| ETXD1 | Transmit Data |
| ETXD2 | Transmit Data |
| ETXD3 | Transmit Data |
| ETXERR | Transmit Error |
| ERXCLK | Receive Clock |
| ERXDV | Receive Data Valid |
| ERXD0 | Receive Data |
| ERXD1 | Receive Data |
| ERXD2 | Receive Data |
| ERXD3 | Receive Data |
| ERXERR | Receive Error |
| ECRS | Carrier Sense |
| ECOL | Collision Indication |

**TABLE 25-2: RMII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 1)**

| Pin Name | Description |
|---|---|
| EMDC | Management Clock |
| EMDIO | Management I/O |
| ETXEN | Transmit Enable |
| ETXD0 | Transmit Data |
| ETXD1 | Transmit Data |
| EREFCLK | Reference Clock |
| ECRSDV | Carrier Sense – Receive Data Valid |
| ERXD0 | Receive Data |
| ERXD1 | Receive Data |
| ERXERR | Receive Error |

**Note:** Ethernet controller pins that are not used by selected interface can be used by other peripherals.

**TABLE 25-3: MII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 0)**

| Pin Name | Description |
|---|---|
| AEMDC | Management Clock |
| AEMDIO | Management I/O |
| AETXCLK | Transmit Clock |
| AETXEN | Transmit Enable |
| AETXD0 | Transmit Data |
| AETXD1 | Transmit Data |
| AETXD2 | Transmit Data |
| AETXD3 | Transmit Data |
| AETXERR | Transmit Error |
| AERXCLK | Receive Clock |
| AERXDV | Receive Data Valid |
| AERXD0 | Receive Data |
| AERXD1 | Receive Data |
| AERXD2 | Receive Data |
| AERXD3 | Receive Data |
| AERXERR | Receive Error |
| AECRS | Carrier Sense |
| AECOL | Collision Indication |

**Note:** The MII mode Alternate Interface is not available on 64-pin devices.

**TABLE 25-4: RMII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 0)**

| Pin Name | Description |
|---|---|
| AEMDC | Management Clock |
| AEMDIO | Management I/O |
| AETXEN | Transmit Enable |
| AETXD0 | Transmit Data |
| AETXD1 | Transmit Data |
| AEREFCLK | Reference Clock |
| AECRSDV | Carrier Sense – Receive Data Valid |
| AERXD0 | Receive Data |
| AERXD1 | Receive Data |
| AERXERR | Receive Error |

**REGISTER 25-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | TXBUSE | RXBUSE | — | — | — | EWMARK | FWMARK |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXDONE | PKTPEND | RXACT | — | TXDONE | TXABORT | RXBUFNA | RXOVFLW |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSE:** Transmit BVCI Bus Error Interrupt bit

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the TX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 13 **RXBUSE:** Receive BVCI Bus Error Interrupt bit

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the RX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARK:** Empty Watermark Interrupt bit

1 = Empty Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a '0' or a '1' has no effect.

bit 8 **FWMARK:** Full Watermark Interrupt bit

1 = Full Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 7 **RXDONE:** Receive Done Interrupt bit

1 = RX packet was successfully received
0 = No interrupt pending

This bit is set whenever an RX packet is successfully received. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

**Note:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

**TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT ($I_{PD}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Power-Down Current ($I_{PD}$)(1) for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| DC40 | 10 | 40 | μA | -40°C | 2.3V | Base Power-Down Current **(Note 6)** |
| DC40a | 36 | 100 | | +25°C | | |
| DC40b | 400 | 720 | | +85°C | | |
| DC40h | 900 | 1800 | | +105°C | | |
| DC40c | 41 | 120 | | +25°C | 3.3V | Base Power-Down Current |
| DC40d | 22 | 80 | | -40°C | 3.6V | Base Power-Down Current **(Note 6)** |
| DC40e | 42 | 120 | | +25°C | | |
| DC40g | 315 | 400(5) | | +70°C | | |
| DC40f | 410 | 800 | | +85°C | | |
| DC40i | 1000 | 2000 | | +105°C | | |
| **Module Differential Current for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| DC41 | — | 10 | μA | — | 2.3V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Notes 3,6)** |
| DC41a | 5 | — | | | 3.3V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Note 3)** |
| DC41b | — | 20 | | | 3.6V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Note 3,6)** |
| DC42 | — | 40 | μA | — | 2.3V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Notes 3,6)** |
| DC42a | 23 | — | | | 3.3V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Note 3)** |
| DC42b | — | 50 | | | 3.6V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Note 3,6)** |
| DC43 | — | 1300 | μA | — | 2.5V | ADC: $\Delta I_{ADC}$ **(Notes 3,4,6)** |
| DC43a | 1100 | — | | | 3.3V | ADC: $\Delta I_{ADC}$ **(Notes 3,4)** |
| DC43b | — | 1300 | | | 3.6V | ADC: $\Delta I_{ADC}$ **(Notes 3,4,6)** |

**Note 1:** The test conditions for $I_{PD}$ current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base $I_{PD}$ current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.

**6:** This parameter is characterized, but not tested in manufacturing.

**TABLE 32-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | IIL | **Input Leakage Current(3)** | | | | | |
| DI50 | | I/O Ports | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI51 | | Analog Input Pins | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI55 | | $\overline{MCLR}$(2) | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD |
| DI56 | | OSC1 | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, XT and HS modes |
| DI60a | IICL | **Input Low Injection Current** | 0 | — | -5(7,10) | mA | This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA. |
| DI60b | IICH | **Input High Injection Current** | 0 | — | +5(8,9,10) | mA | This parameter applies to all pins, with the exception of all 5V tolerant pins, SOSCI, and RB10. Maximum IICH current for these exceptions is 0 mA. |
| DI60c | ∑IICT | **Total Input Injection Current (sum of all I/O and control pins)** | -20(11) | — | +20(11) | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins ( \| IICL + \| IICH \| ) ≤ ∑IICT |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** This parameter is characterized, but not tested in manufacturing.

**5:** See the **"Device Pin Tables"** section for the 5V-tolerant pins.

**6:** The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.

**7:** VIL source < (VSS - 0.3). Characterized but not tested.

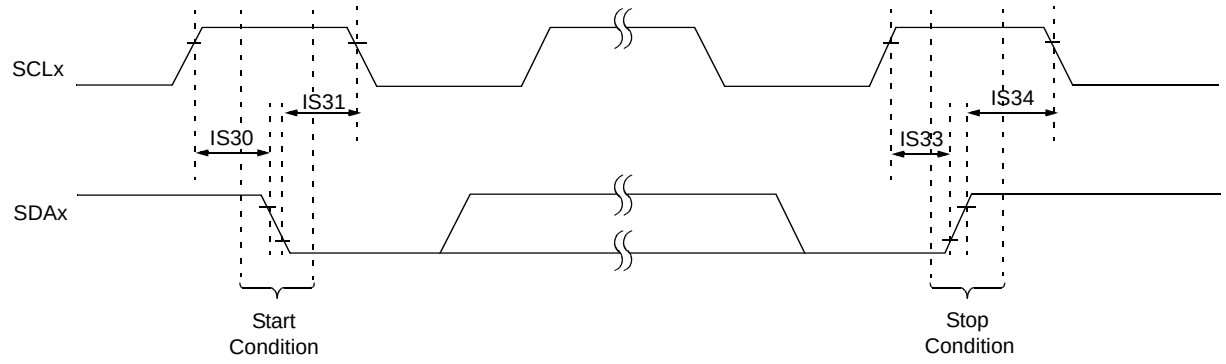
**8:** VIH source > (VDD + 0.3) for non-5V tolerant pins only.

**9:** Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

**10:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

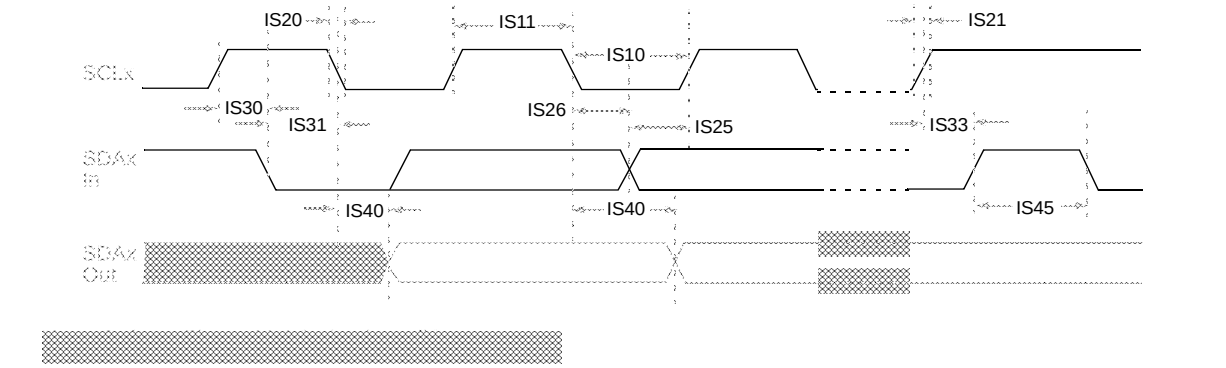
**11:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 8**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

**FIGURE 32-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**



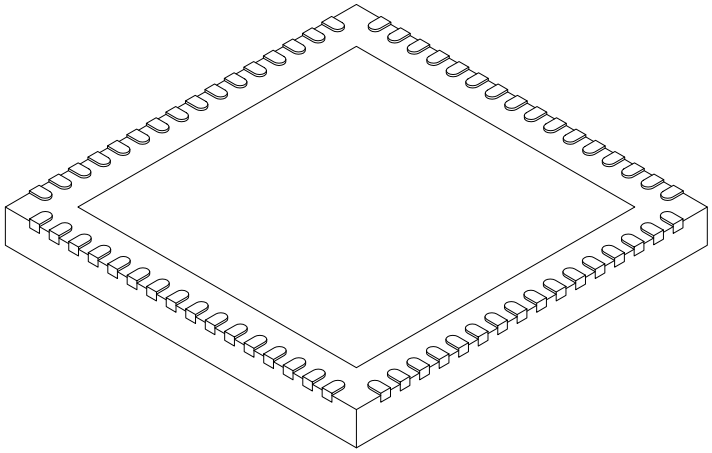

**Note:** Refer to Figure 32-1 for load conditions.

**FIGURE 32-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**



**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]**
**With 7.15 x 7.15 Exposed Pad [QFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 64 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 9.00 BSC | |
| Exposed Pad Width | E2 | 7.05 | 7.15 | 7.50 |
| Overall Length | D | | 9.00 BSC | |
| Exposed Pad Length | D2 | 7.05 | 7.15 | 7.50 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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**TABLE B-4: SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **7.0 "Interrupt Controller"** | • Updated the following Interrupt Sources in Table 7-1:<br>- Changed IC2AM – I2C4 Master Event to: IC4M – I2C4 Master Event<br>- Changed IC3AM – I2C5 Master Event to: IC5M – I2C4 Master Event<br>- Changed U1E – UART1A Error to: U1E – UART1 Error<br>- Changed U4E – UART1B Error to: U4E – UART4 Error<br>- Changed U1RX – UART1A Receiver to: U1RX – UART1 Receiver<br>- Changed U4RX – UART1B Receiver to: U4RX – UART4 Receiver<br>- Changed U1TX – UART1A Transmitter to: U1TX – UART1 Transmitter<br>- Changed U4TX – UART1B Transmitter to: U4TX – UART4 Transmitter<br>- Changed U6E – UART2B Error to: U6E – UART6 Error<br>- Changed U6RX – UART2B Receiver to: U6RX – UART6 Receiver<br>- Changed U6TX – UART2B Transmitter to: U6TX – UART6 Transmitter<br>- Changed U5E – UART3B Error to: U5E – UART5 Error<br>- Changed U5RX – UART3B Receiver to: U5RX – UART5 Receiver<br>- Changed U5TX – UART3B Transmitter to: U5TX – UART5 Transmitter |
| **1.0 "Oscillator Configuration"** | Updated Figure 1-1 |
| **1.0 "Output Compare"** | Updated Figure 1-1 |
| **1.0 "Ethernet Controller"** | Added a note on using the Ethernet controller pins (see note above Table 1-3) |
| **1.0 "Comparator Voltage Reference ($CV_{REF}$)"** | Updated the note in Figure 1-1 |
| **1.0 "Special Features"** | Updated the bit description for bit 10 in Register 1-2<br>Added notes 1 and 2 to Register 1-4 |
| **1.0 "Electrical Characteristics"** | Updated the Absolute Maximum Ratings:<br>• Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD}$ < 2.3V - 0.3V to +3.6V was updated<br>• Voltage on $V_{BUS}$ with respect to $V_{SS}$ - 0.3V to +5.5V was added<br>Updated the maximum value of DC16 as 2.1 in Table 1-4<br>Updated the Typical values for the following parameters: DC20b, DC20c, DC21c, DC22c and DC23c (see Table 1-5)<br>Updated Table 1-11:<br>• Removed the following DC Characteristics: Programming temperature 0°C ≤ TA ≤ +70°C (25°C recommended)<br>• Updated the Minimum value for the Parameter number D131 as 2.3<br>• Removed the Conditions for the following Parameter numbers: D130, D131, D132, D135, D136 and D137<br>• Updated the condition for the parameter number D130a and D132a<br>Updated the Minimum, Typical and Maximum values for parameter D305 in Table 1-13<br>Added note 2 to Table 1-18<br>Updated the Minimum and Maximum values for parameter F20b (see Table 1-19)<br>Updated the following figures:<br>• Figure 1-4<br>• Figure 1-9<br>• Figure 1-22<br>• Figure 1-23 |
| **Appendix A: "Migrating from PIC32MX3XX/4XX to PIC32MX5XX/ 6XX/7XX Devices"** | Removed the A.3 Pin Assignments sub-section. |

**TABLE B-7: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **32.0 “Electrical Characteristics”** | Note 4 in the Operating Current specification was updated (see Table 32-5).<br>Note 3 in the Idle Current specification was updated (see Table 32-6).<br>Note 6 references in the Power-Down Current specification were updated (see Table 32-7).<br>The Program Memory parameters, D135, D136, and D137, and Note 4 were updated (see Table 32-11).<br>The Voltage Reference Specifications were updated (see Table 32-14).<br>Parameter DO50 (Cosco) was added to the Capacitive Loading Requirements on Output Pins (see Table 32-16).<br>The EJTAG Timing Characteristics were updated (see Figure 32-28).<br>The maximum value for parameters ET13 and ET14 were updated in the Ethernet Module Specifications (see Table 32-35).<br>Parameter PM7 (TDHOLD) was updated (see Table 32-40). |
| **34.0 “Packaging Information”** | Packaging diagrams were updated. |
| **Product Identification System** | The Speed and Program Memory Size were updated and Note 1 was added. |