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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx575f512l-80v-bg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)

1	21-PIN TFBGA (BOTTOM VIEW	/)	L1	11
	PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L		L1	A11
No	te: The TFBGA package skips from row	/ "H" to ro	w "J" and has no "I" row. A1	
Pin #	Full Pin Name	Pin #	Full Pin Name	
J3	PGED2/AN7/RB7	K8	VDD	
J4	AVdd	K9	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15	
J5	AN11/ERXERR/AETXERR/PMA12/RB11	K10	USBID/RF3	
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2	
J7	AN12/ERXD0/AECRS/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6	
J8	No Connect (NC)	L2	VREF-/CVREF-/AERXD2/PMA7/RA9	
J9	No Connect (NC)	L3	AVss	
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9	
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10	
K1	PGEC1/AN1/CN3/RB1	L6	SCK4/U5TX/U2RTS/RF13	
K2	PGED1/AN0/CN2/RB0	L7	AN13/ERXD1/AECOL/PMA10/RB13	
K3	VREF+/CVREF+/AERXD3/PMA6/RA10	L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15	
K4	AN8/C1OUT/RB8	L9	AETXD0/SS3/U4RX/U1CTS/CN20/RD14	
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4	
K6	SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5	
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14			

Note 1: Shaded pins are 5V tolerant.

Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

- Note 1: To access the documents listed below, browse to the documentation section of the PIC32MX795F512L product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list. In addition to parameters, features, and other documentation, the resulting page provides links to the related family
- Section 1. "Introduction" (DS60001127)
- Section 2. "CPU" (DS60001113)
- Section 4. "Prefetch Cache" (DS60001119)
- Section 3. "Memory Organization" (DS60001115)

reference manual sections.

- Section 5. "Flash Program Memory" (DS60001121)
- Section 6. "Oscillator Configuration" (DS60001112)
- Section 7. "Resets" (DS60001118)
- Section 8. "Interrupt Controller" (DS60001108)
- Section 9. "Watchdog Timer and Power-up Timer (DS60001114)
- Section 10. "Power-Saving Features" (DS60001130)
- Section 12. "I/O Ports" (DS60001120)
- Section 13. "Parallel Master Port (PMP)" (DS60001128)
- Section 14. "Timers" (DS60001105)
- Section 15. "Input Capture" (DS60001122)
- Section 16. "Output Capture" (DS60001111)
- Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104)
- Section 19. "Comparator" (DS60001110)
- Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109)
- Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107)
- Section 23. "Serial Peripheral Interface (SPI)" (DS60001106)
- Section 24. "Inter-Integrated Circuit (I2C)" (DS60001116)
- Section 27. "USB On-The-Go (OTG)" (DS60001126)
- Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125)
- Section 31. "Direct Memory Access (DMA) Controller" (DS60001117)
- Section 32. "Configuration" (DS60001124)
- Section 33. "Programming and Diagnostics" (DS60001129)
- Section 34. "Controller Area Network (CAN)" (DS60001154)
- Section 35. "Ethernet Controller" (DS60001155)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
31.24	—	—	—	—	—	—	—	—				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
23:16	—	—	—	—	—	—	—	—				
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0				
15:8	BMXDUDBA<15:8>											
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0				
7:0				BMXDU	DBA<7:0>							

REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER

Legend:

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUDBA<15:10>: DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 BMXDUDBA<9:0>: DRM User Data Base Address Read-Only bits Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
21.24	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
31.24	LTAGBOOT	—	—	—	—	-	—	—					
22.16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
23.10	LTAG<19:12>												
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
15.0	LTAG<11:4>												
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-0	R/W-0	R/W-1	U-0					
7.0		LTAG-	<3:0>		LVALID	LLOCK	LTYPE	—					

REGISTER 9-3: CHETAG: CACHE TAG REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31 LTAGBOOT: Line Tag Address Boot bit

- 1 = The line is in the 0x1D000000 (physical) area of memory
- 0 = The line is in the 0x1FC00000 (physical) area of memory

bit 30-24 Unimplemented: Write '0'; ignore read

bit 23-4 LTAG<19:0>: Line Tag Address bits

LTAG<19:0> bits are compared against physical address to determine a hit. Because its address range and position of PFM in kernel space and user space, the LTAG PFM address is identical for virtual addresses, (system) physical addresses, and PFM physical addresses.

bit 3 LVALID: Line Valid bit

- 1 = The line is valid and is compared to the physical address for hit detection
- 0 = The line is not valid and is not compared to the physical address for hit detection

bit 2 LLOCK: Line Lock bit

- 1 = The line is locked and will not be replaced
- 0 = The line is not locked and can be replaced

bit 1 LTYPE: Line Type bit

- 1 = The line caches instruction words
- 0 = The line caches data words
- bit 0 Unimplemented: Write '0'; ignore read

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

ess										Bi	its								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
35E0		31:16	-	-	—	—	—	—	-	—	_	—	—	—	—	—	-	—	0000
001.0	DOINOOIZ	15:0								CHSSIZ	Z<15:0>								0000
2000		31:16	—	—	_	_	_	- 1	—	—	_	_	_	_	-	_	_	_	0000
3600	DCH/DSIZ	15:0	CHDSIZ<15:0> 0000																
2040		31:16	_	_	-	-	-	-	_	-	_	-	-	_	—	-	_	_	0000
3610	DCH/SPIR	15:0	CHSPTR<15:0> 0												0000				
2620		31:16	_	_	_	-	-	-	_	_	_	—	-	_	—	_	_	_	0000
3020	DCHIDPIK	15:0								CHDPT	R<15:0>								0000
2020		31:16	_	_	—	_	-	—	_	-	_	—	_	_	—	_	—	_	0000
3630	DCH/CSIZ	15:0								CHCSIZ	Z<15:0>								0000
2040		31:16	_	_	-	-	-	-	_	-	_	-	-	_	-	-	_	_	0000
3640	DCH/CPIR	15:0								CHCPT	R<15:0>								0000
2650		31:16	_	—	—	—	_	_	—	—	—	—	_	—	—	_	_	_	0000
3050		15:0		_	_	_	_	_	_	—				CHPDA	AT<7:0>				0000

PIC32MX5XX/6XX/7XX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
 - 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
 - 0 = No interrupt is pending
- bit 4 CHDHIF: Channel Destination Half Full Interrupt Flag bit
 - 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
 0 = No interrupt is pending

bit 3 CHBCIF: Channel Block Transfer Complete Interrupt Flag bit

- 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
- 0 = No interrupt is pending

bit 2 CHCCIF: Channel Cell Transfer Complete Interrupt Flag bit

- 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
- 0 = No interrupt is pending
- bit 1 CHTAIF: Channel Transfer Abort Interrupt Flag bit
 - 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
 - 0 = No interrupt is pending

bit 0 CHERIF: Channel Address Error Interrupt Flag bit

- 1 = A channel address error has been detected (either the source or the destination address is invalid)
- 0 = No interrupt is pending

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—		—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10		_	_	_			_	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—		—	—	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	DPPULUP DMPULUP		DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

REGISTER 11-4: U10TGCON: USB OTG CONTROL REGISTER

Legend:

bit 7

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

DPPULUP: D+ Pull-Up Enable bit 1 = D+ data line pull-up resistor is enabled 0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

- 1 = D- data line pull-up resistor is enabled
 0 = D- data line pull-up resistor is disabled
- bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
 - 1 = D+ data line pull-down resistor is enabled
 - 0 = D+ data line pull-down resistor is disabled

bit 4 DMPULDWN: D- Pull-Down Enable bit

- 1 = D- data line pull-down resistor is enabled
- 0 = D- data line pull-down resistor is disabled

bit 3 VBUSON: VBUS Power-on bit

- 1 = VBUS line is powered
- 0 = VBUS line is not powered
- bit 2 **OTGEN:** OTG Functionality Enable bit
 - 1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
 - 0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 VBUSCHG: VBUS Charge Enable bit

- 1 = VBUS line is charged through a pull-up resistor
- 0 = VBUS line is not charged through a resistor

bit 0 VBUSDIS: VBUS Discharge Enable bit

- 1 = VBUS line is discharged through a pull-down resistor
- 0 = VBUS line is not discharged through a resistor

TABLE 12-5: PORTD REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

ess	Register Name ⁽¹⁾	e								Bi	ts								9
Virtual Add (BF88_#		Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6000	TDICD	31:16	_	_	_	_	-	—	_	_	_	_	_	_	_	_	_	_	0000
6000	I RISD	15:0		_		_	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	OFFF
6000		31:16	_	—	_	—		—	-		_	_	_	_	_	_	_	_	0000
0000	FORTD	15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0		31:16		—	_	—		_			_	_	_	_	_	-		_	0000
00E0	LAID	15:0	-	_	_	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60E0	0000	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0050	ODCD	15:0	_	_	_	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 12-6: PORTD REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F512L, AND PIC32MX795F512L DEVICES

ess		Ó								В	ts								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6000	TRICD	31:16	-	_	_	-	—	—	—	—	-	—	_	_	—	—	_	_	0000
6000	TRISD	15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
6000		31:16	_	_	_	_	_	—	_	_		_	_	_	—	—	_	_	0000
00D0	FORTD	15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
6050		31:16	—	—	—	—			—	_	_	—	—	—	—	—	—	—	0000
OUEU	LAID	15:0	LAT15	LAT14	LAT13	LAT12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
6050	0000	31:16	_	_	_	_		_	_	_	_	_	_	_	_	_	_	_	0000
00F0	UDUD	15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

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Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

PIC32MX5XX/6XX/7XX

NOTES:

REGISTER 22-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)

- bit 3 RTCWREN: RTC Value Registers Write Enable bit⁽⁴⁾
 - 1 = RTC Value registers can be written to by the user
 - 0 = RTC Value registers are locked out from being written to by the user
- bit 2 RTCSYNC: RTCC Value Registers Read Synchronization bit
 - 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
 - 0 = RTC Value registers can be read without concern about a rollover ripple
- bit 1 HALFSEC: Half-Second Status bit⁽⁵⁾
 - 1 = Second half period of a second
- 0 = First half period of a second
- bit 0 RTCOE: RTCC Output Enable bit
 - 1 = RTCC clock output is enabled (clock presented onto an I/O)
 - 0 = RTCC clock output is disabled
- **Note 1:** The ON bit is only writable when RTCWREN = 1.
 - 2: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
 - 4: The RTCWREN bit can only be set when the write sequence is enabled.
 - 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is only reset on a Power-on Reset (POR).

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31.24	FLTEN19	MSEL1	9<1:0>	FSEL19<4:0>						
22,46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	FLTEN18	MSEL1	8<1:0>	FSEL18<4:0>						
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15.6	FLTEN17	TEN17 MSEL17<1:0>				FSEL17<4:0:	>			
7.0	R/W-0	R/W-0	R/W-0 R/W-0		R/W-0	R/W-0	R/W-0	R/W-0		
7.0	FLTEN16	MSEL1	6<1:0>	FSEL16<4:0>						

REGISTER 24-14: CIFLTCON4: CAN FILTER CONTROL REGISTER 4

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN19: Filter 19 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL19<1:0>: Filter 19 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 28-24	FSEL19<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN18: Filter 18 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 22-21	MSEL18<1:0>: Filter 18 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 20-16	FSEL18<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31.24	HT<31:24>										
22.46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23.10	HT<23:16>										
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15.0	HT<15:8>										
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0				HT<	7:0>						

REGISTER 25-5: ETHHT0: ETHERNET CONTROLLER HASH TABLE 0 REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 HT<31:0>: Hash Table Bytes 0-3 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 25-6: ETHHT1: ETHERNET CONTROLLER HASH TABLE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24	HT<63:56>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23.10	HT<55:48>										
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
10.0	HT<47:40>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0				HT<3	9:32>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 HT<63:32>: Hash Table Bytes 4-7 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 25-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER (CONTINUED) bit 7 **CRCERREN:** CRC Error Collection Enable bit 1 = The received packet CRC must be invalid for the packet to be accepted 0 = Disable CRC Error Collection filtering This bit allows the user to collect all packets that have an invalid CRC. CRCOKEN: CRC OK Enable bit bit 6 1 = The received packet CRC must be valid for the packet to be accepted 0 = Disable CRC filtering This bit allows the user to reject all packets that have an invalid CRC. RUNTERREN: Runt Error Collection Enable bit bit 5 1 = The received packet must be a runt packet for the packet to be accepted 0 = Disable Runt Error Collection filtering This bit allows the user to collect all packets that are runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes (when CRCOKEN = 0) or any packet with a size of less than 64 bytes that has a valid CRC (when CRCOKEN = 1). bit 4 RUNTEN: Runt Enable bit 1 = The received packet must not be a runt packet for the packet to be accepted 0 = Disable Runt filtering This bit allows the user to reject all runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes. bit 3 UCEN: Unicast Enable bit 1 = Enable Unicast Filtering 0 = Disable Unicast Filtering This bit allows the user to accept all unicast packets whose Destination Address matches the Station Address. bit 2 NOTMEEN: Not Me Unicast Enable bit 1 = Enable Not Me Unicast Filtering 0 = Disable Not Me Unicast Filtering This bit allows the user to accept all unicast packets whose Destination Address does not match the Station Address. bit 1 MCEN: Multicast Enable bit 1 = Enable Multicast Filtering 0 = Disable Multicast Filtering This bit allows the user to accept all Multicast Address packets.

bit 0 BCEN: Broadcast Enable bit

- 1 = Enable Broadcast Filtering
- 0 = Disable Broadcast Filtering

This bit allows the user to accept all Broadcast Address packets.

- **Note 1:** XOR = True when either one or the other conditions are true, but not both.
 - 2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
 - 3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

```
Note 1:
          This register is only used for RX operations.
      2:
          The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.
```

PIC32MX5XX/6XX/7XX

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0						
31:24		_	—	—	—	—	—	—
00.40	U-0	U-0						
23.10		_	—	—	—	—	—	—
15.0	U-0	U-0						
15.0		_	—	—	—	—	—	—
7.0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
7.0			_	_	_	TESTBP	TESTPAUSE ⁽¹⁾	SHRTQNTA ⁽¹⁾

REGISTER 25-30: EMAC1TEST: ETHERNET CONTROLLER MAC TEST REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 Unimplemented: Read as '0'

- bit 2 TESTBP: Test Backpressure bit
 - 1 = The MAC will assert backpressure on the link. Backpressure causes preamble to be transmitted, raising carrier sense. A transmit packet from the system will be sent during backpressure.
 0 = Normal operation

bit 1 **TESTPAUSE:** Test PAUSE bit⁽¹⁾

- 1 = The MAC Control sub-layer will inhibit transmissions, just as if a PAUSE Receive Control frame with a non-zero pause time parameter was received
- 0 = Normal operation

bit 0 SHRTQNTA: Shortcut PAUSE Quanta bit⁽¹⁾

- 1 = The MAC reduces the effective PAUSE Quanta from 64 byte-times to 1 byte-time
- 0 = Normal operation
- **Note 1:** This bit is only for testing purposes.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

26.1 Control Registers

TABLE 26-1: COMPARATOR REGISTER MAP

ess										Bi	its								ú
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
4 0 0 0		31:16		—	—	—	—	_	—	—	—	—	—	—	—	—	—	—	0000
A000	CIVITCON	15:0	ON	COE	CPOL	_	—	_	_	COUT	EVPO	L<1:0>	—	CREF	_	_	CCH	<1:0>	00C3
4010	CM2CON	31:16	-	_	_	_	—	_	_	_	_	—	_	_	_	—	—	_	0000
AUTU	CIVIZCON	15:0	ON	COE	CPOL	—	-	—	—	COUT	EVPO	L<1:0>	—	CREF	—	-	CCH	<1:0>	00C3
A060	CMSTAT	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
A000	CIVISTAT	15:0	_	_	SIDL	_	_	_	_	_	_	_	_	_	_	_	C2OUT	C10UT	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

27.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them. A block diagram of the module is illustrated in Figure 27-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/Vss or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

Key features of the CVREF module include:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- · Output can be connected to a pin





			Standard Operating Conditions: 2.3V to 3.6V								
DC CHA	RACTER	ISTICS	(unless otherwi	se stated)							
			Operating tempe	rature -40 -40	ר ≤ 10 ≤ 10 ≤ י ר < ד∆ < י	+85°C I +105°C	for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions				
	VIL	Input Low Voltage									
DI10		I/O Pins:									
		with TTL Buffer	Vss		0.15 Vdd	V					
		with Schmitt Trigger Buffer	Vss		0.2 Vdd	V					
DI15		MCLR ⁽²⁾	Vss	_	0.2 Vdd	V					
DI16		OSC1 (XT mode)	Vss	_	0.2 Vdd	V	(Note 4)				
DI17		OSC1 (HS mode)	Vss		0.2 Vdd	V	(Note 4)				
DI18		SDAx, SCLx	Vss		0.3 Vdd	V	SMBus disabled				
							(Note 4)				
DI19		SDAx, SCLx	Vss		0.8	V	SMBus enabled				
							(Note 4)				
	Vih	Input High Voltage									
DI20		I/O Pins not 5V-tolerant(3)	0.65 VDD		VDD	V	(Note 4,6)				
		I/O Pins 5V-tolerant with PMP ⁽⁵⁾	0.25 VDD + 0.8V	—	5.5	V	(Note 4,6)				
		I/O Pins 5V-tolerant ⁽⁵⁾	0.65 Vdd	_	5.5	V					
DI28		SDAx, SCLx	0.65 VDD		5.5	V	SMBus disabled				
							(Note 4,6)				
DI29		SDAx, SCLx	2.1		5.5	V	SMBus enabled,				
							$2.3V \le VPIN \le 5.5$				
-	-						(Note 4,6)				
0130	ICNPU	Change Notification	_	—	-50	μA	VDD = 3.3V, VPIN = VSS				
DIGA		Pull-up Current		50							
DI31	ICNPD	Change Notification Pull-down Current ⁽⁴⁾	—	50	_	μA	טטע = 3.3V, VPIN = VDD				

TABLE 32-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- **3:** Negative current is defined as current sourced by the pin.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: See the "Device Pin Tables" section for the 5V-tolerant pins.
- 6: The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pullups are guaranteed to be recognized as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.
- 7: VIL source < (VSS 0.3). Characterized but not tested.
- 8: VIH source > (VDD + 0.3) for non-5V tolerant pins only.
- **9:** Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.
- **10:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (Vss 0.3)).
- 11: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If Note 7, IICL = (((Vss 0.3) VIL source) / Rs). If Note 8, IICH = ((IICH source (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (Vss 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.



TABLE 32-29: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

АС СНА	ARACTERIS	TICS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-Temp						
Param. No.	Symbol	Min.	Тур. ⁽²⁾	Max.	Units	Conditions			
SP10	TscL	SCKx Output Low Time ⁽³⁾	Tsck/2	—		ns	—		
SP11	TscH	SCKx Output High Time ⁽³⁾	Tsck/2	—	_	ns	—		
SP20	TscF	SCKx Output Fall Time ⁽⁴⁾		—		ns	See parameter DO32		
SP21	TscR	SCKx Output Rise Time ⁽⁴⁾		_		ns	See parameter DO31		
SP30	TDOF	SDOx Data Output Fall Time ⁽⁴⁾	_	—	_	ns	See parameter DO32		
SP31	TDOR	SDOx Data Output Rise Time ⁽⁴⁾		_		ns	See parameter DO31		
SP35	TscH2doV,	SDOx Data Output Valid after	_	—	15	ns	VDD > 2.7V		
	TscL2doV	SCKx Edge	_	—	20	ns	Vdd < 2.7V		
SP36	TDOV2SC, TDOV2SCL	SDOx Data Output Setup to First SCKx Edge	15	—		ns	—		
SP40	0 TDIV2SCH, Setup Time of SDIx Data Input to		15	_		ns	VDD > 2.7V		
	TDIV2scL	SCKx Edge	20	—	_	ns	VDD < 2.7V		
SP41	TscH2DIL,	Hold Time of SDIx Data Input	15	_	_	ns	VDD > 2.7V		
	TscL2DIL	to SCKx Edge	20	_	_	ns	Vdd < 2.7V		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- **3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPIx pins.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimensio	on Limits	MIN	NOM	MAX		
Contact Pitch	E	0.50 BSC				
Contact Pad Spacing	C1		11.40			
Contact Pad Spacing	C2		11.40			
Contact Pad Width (X64)	X1			0.30		
Contact Pad Length (X64)	Y1			1.50		
Distance Between Pads	G	0.20				

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

APPENDIX B: REVISION HISTORY

Revision A (August 2009)

This is the initial released version of this document.

Revision B (November 2009)

The revision includes the following global update:

Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits.

Other major changes are referenced by their respective chapter/section in Table B-1.

Section Name	Update Description
"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"	Added the following devices: - PIC32MX575F256L - PIC32MX695F512L - PIC32MX695F512H
	The 100-pin TQFP pin diagrams have been updated to reflect the current pin name locations (see the " Pin Diagrams " section).
	Added the 121-pin Ball Grid Array (XBGA) pin diagram.
	Updated Table 1: "PIC32 USB and CAN – Features"
	Added the following tables:
	 Table 4: "Pin Names: PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L and PIC32MX575F512L Devices"
	 Table 5: "Pin Names: PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L and PIC32MX695F512L Devices"
	 Table 6: "Pin Names: PIC32MX775F256L, PIC32MX775F512L and PIC32MX795F512L Devices"
	Updated the following pins as 5V tolerant:
	- 64-pin QFN: Pin 36 (D-/RG3) and Pin 37 (D+/RG2)
	- 64-pin TQFP: Pin 36 (D-/RG3) and Pin 37 (D+/RG2)
	- 100-pin TQFP: Pin 56 (D-/RG3) and Pin 57 (D+/RG2)
1.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	Removed the last sentence of 1.3.1 "Internal Regulator Mode".
	Removed Section 2.3.2 "External Regulator Mode"

TABLE B-1: MAJOR SECTION UPDATES