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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx575f512lt-80i-pt

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Note 1: If the USB module is not used, this pin must be connected to VDD.

2: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 3Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2}$$
 (i.e., ADC conversion rate/2)
$$f = \frac{1}{(2\pi\sqrt{LC})}$$
$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

3: Aluminum or electrolytic capacitors should not be used. ESR $\leq 3\Omega$ from -40°C to 125°C @ SYSCLK frequency (i.e., MIPS).

2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 μF to 47 μF . This capacitor should be located as close to the device as possible.

2.3 Capacitor on Internal Voltage Regulator (VCAP)

2.3.1 INTERNAL REGULATOR MODE

A low-ESR (1 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 32.0 "Electrical Characteristics"** for additional information on CEFC specifications.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

- 2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.
- **3:** No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R	R	R	R	R	R	R	R			
31:24		BMXPFMSZ<31:24>									
00.40	R	R	R	R	R	R	R	R			
23.10	BMXPFMSZ<23:16>										
45.0	R	R	R	R	R	R	R	R			
15:8	BMXPFMSZ<15:8>										
7.0	R	R	R	R	R	R	R	R			
7:0				BMXPF	MSZ<7:0>						

REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BMXPFMSZ<31:0>: Program Flash Memory (PFM) Size bits

Static value that indicates the size of the PFM in bytes: 0x00010000 = device has 64 KB Flash 0x00020000 = device has 128 KB Flash 0x00040000 = device has 256 KB Flash 0x00080000 = device has 512 KB Flash

REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31.24	R	R	R	R	R	R	R	R			
31.24		BMXBOOTSZ<31:24>									
00.40	R	R	R	R	R	R	R	R			
23:16	BMXBOOTSZ<23:16>										
15.0	R	R	R	R	R	R	R	R			
10.0	BMXBOOTSZ<15:8>										
7.0	R	R	R	R	R	R	R	R			
7:0				BMXBO	OTSZ<7:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits Static value that indicates the size of the Boot PFM in bytes: 0x00003000 = device has 12 KB boot Flash

6.0 RESETS

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 7. "Resets" (DS60001118) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- Power-on Reset (POR)
- Master Clear Reset pin (MCLR)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.



FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM

TABLE 7-5: INTERRUPT REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L PIC32MX575F512L AND PIC32MX575F256L DEVICES (CONTINUED)

ess		0		Bits																						
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets							
1000		31:16		—	—		INT4IP<2:0>	•	INT4IS	6<1:0>		—	—		OC4IP<2:0>		OC4IS	S<1:0>	0000							
1000	IPC4	15:0	_	_	—		IC4IP<2:0>		IC4IS	<1:0>	_	—	—		T4IP<2:0>		T4IS-	<1:0>	0000							
4050		31:16	—	_	-		SPI1IP<2:0>		SPI1IS	S<1:0>	—	-	_		OC5IP<2:0>		OC5IS	6<1:0>	0000							
TUEU	IPC5	15:0	_	—	—		IC5IP<2:0>		IC5IS	<1:0>	_	—	—		T5IP<2:0>		T5IS-	<1:0>	0000							
		31:16	_	_	_		AD1IP<2:0>		AD1IS	S<1:0>		—	_		CNIP<2:0>		CNIS	<1:0>	0000							
10E0	IPC6														U1IP<2:0>		U1IS	<1:0>								
IUFU	IFCO	15:0	—	-	-		I2C1IP<2:0>		I2C1IP<2:0>		I2C1IS<1:0>		I2C1IS<1:0>		I2C1IS<1:0>	I2C1IS<1:0>		I2C1IS<1:0>		—	-		SPI3IP<2:0>		SPI3IS<1:0>	0000
														I2C3IP<2:0>		12C315	S<1:0>									
							U3IP<2:0>		U3IS	<1:0>																
1100	IPC7	31:16	—	—	—	SPI2IP<2:0>		SPI2IS	S<1:0>	-	—	-	(CMP2IP<2:0	>	CMP2IS<1:0>		0000								
							I2C4IP<2:0>		12C418	S<1:0>									_							
		15:0	—		-	(CMP1IP<2:0	>	CMP1I	S<1:0>	—	-		PMPIP<2:0>		PMPIS	6<1:0>	0000								
		31:16	—	-	-	F	RTCCIP<2:0	>	RTCCI	S<1:0>	—	-	—	FSCMIP<2:0>		FSCMI	S<1:0>	0000								
1110	IPC8														U2IP<2:0>		U2IS	<1:0>	_							
		15:0	—	-	-		I2C2IP<2:0>	•	12C218	S<1:0>	—	-	-		SPI4IP<2:0>		SPI4IS	S<1:0>	0000							
															I2C5IP<2:0>		12C518	S<1:0>	_							
1120	IPC9	31:16	—	-	-	0	DMA3IP<2:0	>	DMA3I	S<1:0>	—	-	—	l	DMA2IP<2:0	>	DMA2I	S<1:0>	0000							
20		15:0	—	-	-	0	DMA1IP<2:0	>	DMA1I	S<1:0>	—	-	—	l	DMA0IP<2:0	>	DMA0I	S<1:0>	0000							
1130	IPC10	31:16	—	—	—	DI	MA7IP<2:0>	(2)	DMA7IS	S<1:0> ⁽²⁾	—	—	—	D	MA6IP<2:0>	(2)	DMA6IS	<1:0> ⁽²⁾	0000							
1100	11 010	15:0	—	_	_	DMA5IP<2:0> ⁽²⁾		DMA5IS	S<1:0> ⁽²⁾		_	_	D	MA4IP<2:0>	(2)	DMA4IS	<1:0> ⁽²⁾	0000								
11/0		31:16	—	_	_		—	_		_	_	_	_	CAN1IP<2:0>		CAN1I	S<1:0>	0000								
1140		15:0	—	—	—		USBIP<2:0> l		USBIS	<1:0> — — FCEIP<2:0>		FCEIP<2:0>		FCEIS	6<1:0>	0000										
1150		31:16	—	_	_		U5IP<2:0>		U5IS	<1:0>	_	—	—		U6IP<2:0>		U6IS	<1:0>	0000							
1150	11 012	15:0	_	_	_		U4IP<2:0>		U4IS	<1:0>	_	_	_	_	_		_		0000							

PIC32MX5XX/6XX/7XX

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: These bits are not available on PIC32MX534/564 devices.

3: This register does not have associated CLR, SET, and INV registers.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 18-16 PLLMULT<2:0>: Phase-Locked Loop (PLL) Multiplier bits

- 111 = Clock is multiplied by 24
- 110 = Clock is multiplied by 21
- 101 = Clock is multiplied by 20
- 100 = Clock is multiplied by 19
- 011 = Clock is multiplied by 18
- 010 =Clock is multiplied by 17
- 001 =Clock is multiplied by 16
- 000 =Clock is multiplied by 15
- bit 15 Unimplemented: Read as '0'
- bit 14-12 COSC<2:0>: Current Oscillator Selection bits
 - 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC (FRC) Oscillator divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (Posc) (XT, HS or EC)
 - 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast RC (FRC) Oscillator
- bit 11 Unimplemented: Read as '0'
- bit 10-8 NOSC<2:0>: New Oscillator Selection bits
 - 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC Oscillator (FRC) divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (XT, HS or EC)
 - 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast Internal RC Oscillator (FRC)
 - On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).
- bit 7 CLKLOCK: Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):

- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):

Clock and PLL selections are never locked and may be modified.

- bit 6 ULOCK: USB PLL Lock Status bit
 - 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
 - 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled
- bit 5 SLOCK: PLL Lock Status bit
 - 1 = PLL module is in lock or PLL module start-up timer is satisfied
 - 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 SLPEN: Sleep Mode Enable bit

- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed
- bit 3 **CF:** Clock Fail Detect bit
 - 1 = FSCM has detected a clock failure
 - 0 = No clock failure has been detected

Note: Writes to this register require an unlock sequence. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31.24	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	—	—		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CHSSIZ<15:8>									
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0				CHSSIZ	<7:0>					

REGISTER 10-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSSIZ<15:0>: Channel Source Size bits

1111111111111111 = 65,535 byte source size

REGISTER 10-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	—	—	—	—	—	—	—	—		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
10.0	CHDSIZ<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				CHDSIZ	<7:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16	Unimplemented: Read as '0'
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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	—	—	—	_	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	_	_	—	_	—	_		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
10.0	CHCSIZ<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0				CHCSIZ	2<7:0>					

REGISTER 10-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHCSIZ<15:0>: Channel Cell-Size bits

111111111111111 = 65,535 bytes transferred on an event

REGISTER 10-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	U-0 U		U-0	U-0	U-0	U-0	U-0	U-0				
31.24		—	—	_	—			_				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
23:16		—	—	—	—	—		—				
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0				
15:8	CHCPTR<15:8>											
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0				
7:0				CHCPTF	R<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

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REGISTER 11-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—	—	—	—	—	—	—	
22.16	U-0	U-0	U-0	U-0	U-0 U-0		U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15.0			—	—	—	_	—	—	
	R/W-0 R/W-0 R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0			RESUMEIE		TRNIF	SOFIE	LIERRIE(1)	URSTIE ⁽²⁾	
	OTALLIL		I CEOUMEIE	IDELIE		COLL	OLIVIL	DETACHIE ⁽³⁾	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7	STALLIE: STALL Handshake Interrupt Enable bit
	1 = STALL interrupt is enabled
	0 = STALL interrupt is disabled
bit 6	ATTACHIE: ATTACH Interrupt Enable bit
	1 = ATTACH interrupt is enabled
	0 = ATTACH interrupt is disabled
bit 5	RESUMEIE: RESUME Interrupt Enable bit
	1 = RESUME interrupt is enabled
	0 = RESUME interrupt is disabled
bit 4	IDLEIE: Idle Detect Interrupt Enable bit
	1 = Idle interrupt is enabled
	0 = Idle interrupt is disabled
bit 3	TRNIE: Token Processing Complete Interrupt Enable bit
	1 = TRNIF interrupt is enabled
	0 = IRNIF interrupt is disabled
bit 2	SOFIE: SOF Token Interrupt Enable bit
	1 = SOFIF interrupt is enabled
	0 = SOFIF interrupt is disabled
bit 1	UERRIE: USB Error Interrupt Enable bit
	1 = USB Error interrupt is enabled
	0 = 0.5B Error interrupt is disabled
bit 0	URSTIE: USB Reset Interrupt Enable bit ⁽²⁾
	1 = URSTIF interrupt is enabled
	0 = 0RSTIF Interrupt is disabled DETACHIE: USB Datash Interrupt Enable hit(3)
	$\perp = DATICHIF Interrupt is enabled$

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

- 2: Device mode.
- 3: Host mode.

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0 U-0		U-0	U-0	U-0	U-0	U-0	U-0
51.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—		—		—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—		—		—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0				CNT	<7:0>			

REGISTER 11-16: U1SOF: USB SOF THRESHOLD REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-0 CNT<7:0>: SOF Threshold Value bits
 - Typical values of the threshold are: 01001010 = 64-byte packet 00101010 = 32-byte packet 00011010 = 16-byte packet

00010010 = 8-byte packet

REGISTER 11-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
21.24	U-0 U-0		U-0	U-0	U-0	U-0	U-0	U-0				
31.24	—	—	—	—	—	—	—	—				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
23.10	—	—	—	—	—	—	—	—				
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
15.6	—	—	—	—	—	—	—	—				
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0				
7.0	BDTPTRL<15:9>											

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-8 Unimplemented: Read as '0'

bit 7-1 BDTPTRL<15:9>: BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 Unimplemented: Read as '0'

12.2 Control Registers

TABLE 12-1: PORTA REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F512L, PIC32MX775F512L, PIC32MX775F512L, PIC32MX775F512L, PIC32MX795F512L, PIC32MX79F5F512L, PIC32MX79FF512L, PIC32MX79FF512MX79FF512L, PIC32MX79FF512MX79FF512MX79FF512L, PIC32

ess										Bi	its								ú
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6000	TDICA	31:16		—	_			—	_		—	—	_	_	_	_	_	_	0000
6000	IRISA	15:0	TRISA15	TRISA14	-			TRISA10	TRISA9		TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
6010		31:16		_	-			—	_		_	_	_		—		_	_	0000
0010	FURIA	15:0	RA15	RA14	_			RA10	RA9		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
6020		31:16	_	—	—	-	_	_	—		—	—	_	—	—	_	—	—	0000
0020	LAIA	15:0	LATA15	LATA14	-			LATA10	LATA9		LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6020	00004	31:16	_	_	_		_	_	_		_	_	_	_	_	_		_	0000
6030	ODCA	15:0	ODCA15	ODCA14	_	-	1	ODCA10	ODCA9	_	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 12-2:PORTB REGISTER MAP

ess		0								В	its								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6040	TDICD	31:16	—	_	_	_	—	_		—	—	_	—	—	—	—	_	—	0000
6040	IRISD	15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6050		31:16	_	_	_	_	_	_		_	_	_	_	_	_	_	_	_	0000
0050	FORTB	15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
6060		31:16	_	-	_	_		-				_					_		0000
0000	LAID	15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
6070	ODCB	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0070	ODCB	15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 12-7: PORTE REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H,

PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES Virtual Address (BF88_#) Bits Resets Bit Range Register Name⁽¹⁾ 31/15 30/14 29/13 28/12 27/11 26/10 25/9 24/8 23/7 22/6 21/5 20/4 19/3 18/2 17/1 16/0 ₹ 31:16 _ 0000 _ 6100 TRISE 15:0 TRISE7 TRISE6 TRISE5 TRISE4 TRISE3 TRISE2 TRISE1 TRISE0 00FF _ _ _ _ _ _ 31:16 0000 PORTE 6110 15:0 _ _ _ _ _ _ RE7 RE6 RE5 RE4 RE3 RE2 RE1 RE0 xxxx _ _ 0000 31:16 _ _ _ _ 6120 LATE 15:0 _ _ _ _ _ _ _ _ LATE7 LATE6 LATE5 LATE4 LATE3 LATE2 LATE1 LATE0 xxxx 31:16 0000 _ _ _ _ _ _ _ _ 6130 ODCE 15:0 _ _ _ ODCE7 0DCE6 ODCE5 ODCE4 ODCE3 ODCE2 ODCE1 ODCE0 0000 Leaend:

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more Note 1: information.

TABLE 12-8: PORTE REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾			Bits													s		
		Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
C100	TDIOF	31:16	_	—	_	—	—	—	_	-	—	_	_	_	_	_	_	_	0000
6100	IRISE	15:0	_	—	_	_	_	_	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
6110		31:16	_	_		_	-	_	_		_	_	_	-	_	_	_	_	0000
0110	FORTE	15:0	_	_		-		-	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120		31:16	_	_		-			_				—	_		_	_	-	0000
0120	LATE	15:0		_	-	-	-	-	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6120	ODCE	31:16	_		_	_	_	_	_	_	—	_	_	_	_	_	_	_	0000
6130	ODCE	15:0	_	_	_	_	_	_	ODCE9	ODCE8	ODCE7	0DCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—		—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—		—	—
15.0	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
10.0	ON ⁽¹⁾	—	SIDL	TWDIS	TWIP	-	—	—
7.0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
7:0	TGATE		TCKP	S<1:0>		TSYNC	TCS	

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Timer On bit⁽¹⁾
 - 1 = Timer is enabled 0 = Timer is disabled

bit 14 Unimplemented: Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation when device is in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit

- 1 = Writes to TMR1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 TWIP: Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:

1 = Asynchronous write to TMR1 register in progress

0 = Asynchronous write to TMR1 register complete

In Synchronous Timer mode:

This bit is read as '0'.

- bit 10-8 **Unimplemented:** Read as '0'
- bit 7 TGATE: Timer Gated Time Accumulation Enable bit

<u>When TCS = 1:</u> This bit is ignored.

When TCS = 0:

- 1 = Gated time accumulation is enabled
- 0 =Gated time accumulation is disabled
- bit 6 Unimplemented: Read as '0'
- bit 5-4 TCKPS<1:0>: Timer Input Clock Prescale Select bits
 - 11 = 1:256 prescale value
 - 10 = 1:64 prescale value
 - 01 = 1:8 prescale value
 - 00 = 1:1 prescale value
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
31:24		HR104	<3:0>		HR01<3:0>					
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
23:10		MIN10	<3:0>		MIN01<3:0>					
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15:8		SEC10	<3:0>			SEC01<3:0>				
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
7:0	_	_	_	_	_	_	_	_		
Legend:										
R = Read	able bit		W = Writable	e bit	U = Unimplemented bit, read as '0'					

REGISTER 22-3: RTCTIME: RTC TIME VALUE REGISTER

			ipicificitica bit, read as o		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		
bit 31-28 HR10<3:0>: Binary-	Coded Decimal Value of Hou	rs bits, 10 digits; contains a	value from 0 to 2		

bit 31-28 HR10<3:0>: Binary-Coded Decimal Value of Hours bits, 10 digits; contains a value from 0 to 2
bit 27-24 HR01<3:0>: Binary-Coded Decimal Value of Hours bits, 1 digit; contains a value from 0 to 9
bit 23-20 MIN10<3:0>: Binary-Coded Decimal Value of Minutes bits, 10 digits; contains a value from 0 to 5
bit 19-16 MIN01<3:0>: Binary-Coded Decimal Value of Minutes bits, 1 digit; contains a value from 0 to 9
bit 15-12 SEC10<3:0>: Binary-Coded Decimal Value of Seconds bits, 10 digits; contains a value from 0 to 5
bit 11-8 SEC01<3:0>: Binary-Coded Decimal Value of Seconds bits, 1 digit; contains a value from 0 to 9
bit 7-0 Unimplemented: Read as '0'

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

23.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104) in the "PIC32 Family Reference Manual", which is available from Microchip web the site (www.microchip.com/PIC32).

The PIC32MX5XX/6XX/7XX 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 16 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold (S&H) circuit
- Automatic Channel Scan mode
- Selectable conversion trigger source

- 16-word conversion result buffer
- · Selectable buffer fill modes
- Eight conversion result format options
- · Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 23-1. The 10-bit ADC has up to 16 analog input pins, designated AN0-AN15. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

The analog inputs are connected through two multiplexers to one S&H. The analog input multiplexers can be switched between two sets of analog inputs between conversions. Unipolar differential conversions are possible on all channels, other than the pin used as the reference, using a reference input pin (see Figure 23-1).

The Analog Input Scan mode sequentially converts user-specified channels. A control register specifies which analog input channels will be included in the scanning sequence.

The 10-bit ADC is connected to a 16-word result buffer. Each 10-bit result is converted to one of eight 32-bit output formats when it is read from the result buffer.



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0							
31:24	—	—	—	—	—	—	—	_	
00.40	U-0	U-0							
23:16	—	—	—	—	—	—	—	_	
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
15:8	ON ⁽¹⁾	—	SIDL	—	—	FORM<2:0>			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC	
7:0		SSRC<2:0>		CLRASAM	_	ASAM	SAMP ⁽²⁾	DONE ⁽³⁾	

REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit⁽¹⁾
 - 1 = ADC module is operating
 - 0 = ADC module is not operating
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode
- bit 12-11 Unimplemented: Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits

- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing the SAMP bit ends sampling and starts conversion
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write a '0' to end sampling and start conversion. If SSRC<2:0> ≠ '000', this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

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REGISTER 25-17: ETHFRMTXOK: ETHERNET CONTROLLER FRAMES TRANSMITTED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31.24	—	—	—	—	—	—	—	—			
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	—	—			
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15.0	FRMTXOKCNT<15:8>										
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0				FRMTXOK	(CNT<7:0>						

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 **FRMTXOKCNT<15:0>:** Frame Transmitted OK Count bits Increment counter for frames successfully transmitted.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

TABLE 32-35: ETHERNET MODULE SPECIFICATIONS

АС СНА	RACTERISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param. No.	Characteristic	Min.	Typical	Max.	Units	Conditions	
MIIM Tin	ning Requirements						
ET1	MDC Duty Cycle	40		60	%	—	
ET2	MDC Period	400	—	_	ns	—	
ET3	MDIO Output Setup and Hold	10	—	10	ns	See Figure 32-19	
ET4	MDIO Input Setup and Hold	0	—	300	ns	See Figure 32-20	
MII Timi	ng Requirements						
ET5	TX Clock Frequency	—	25	_	MHz	—	
ET6	TX Clock Duty Cycle	35	_	65	%	—	
ET7	ETXDx, ETEN, ETXERR Output Delay	0		25	ns	See Figure 32-21	
ET8	RX Clock Frequency	—	25		MHz	—	
ET9	RX Clock Duty Cycle	35		65	%	—	
ET10	ERXDx, ERXDV, ERXERR Setup and Hold	10		30	ns	See Figure 32-22	
RMII Tin	ning Requirements						
ET11	Reference Clock Frequency	_	50		MHz	—	
ET12	Reference Clock Duty Cycle	35	_	65	%	_	
ET13	ETXDx, ETEN, Setup and Hold	2	—	4	ns	—	
ET14	ERXDx, ERXDV, ERXERR Setup and Hold	2	—	4	ns	—	

Note 1: The Ethernet module is functional at VBORMIN < VDD < 2.9V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 32-19: MDIO SOURCED BY THE PIC32 DEVICE



FIGURE 32-20: MDIO SOURCED BY THE PHY



PIC32MX5XX/6XX/7XX

FIGURE 32-25: PARALLEL SLAVE PORT TIMING



АС СНА	ARACTERIS	STICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-Temp} \end{array}$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions	
PS1	TdtV2wrH	Data In Valid before \overline{WR} or \overline{CS} Inactive (setup time)	20	_	—	ns	_	
PS2	TwrH2dtl	WR or CS Inactive to Data-In Invalid (hold time)	40	—	—	ns	_	
PS3	TrdL2dtV	RD and CS Active to Data-Out Valid	—	—	60	ns	_	
PS4	TrdH2dtl	RD Active or CS Inactive to Data-Out Invalid	0	—	10	ns	_	
PS5	Tcs	CS Active Time	Трв + 40	_		ns	—	
PS6	Twr	WR Active Time	Трв + 25	—	_	ns	—	
PS7	Trd	RD Active Time	Трв + 25	_	_	ns	_	

TABLE 32-39: PARALLEL SLAVE PORT REQUIREMENTS

Note 1: These parameters are characterized, but not tested in manufacturing.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]



DETAIL 1

	Units					
Dimension	Limits	MIN	NOM	MAX		
Number of Leads	N		64			
Lead Pitch	е		0.50 BSC			
Overall Height	Α	-	-	1.20		
Molded Package Thickness	A2	0.95	1.00	1.05		
Standoff	A1	0.05	-	0.15		
Foot Length	L	0.45	0.60	0.75		
Footprint	L1	L1 1.00 REF				
Foot Angle	ø	0°	3.5°	7°		
Overall Width	E		12.00 BSC			
Overall Length	D		12.00 BSC			
Molded Package Width	E1		10.00 BSC			
Molded Package Length	D1		10.00 BSC			
Lead Thickness	С	0.09	-	0.20		
Lead Width	b	0.17	0.22	0.27		
Mold Draft Angle Top	α	11°	12°	13°		
Mold Draft Angle Bottom	β	11°	12°	13°		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or

protrusions shall not exceed 0.25mm per side. 4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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TABLE B-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
4.0 "Memory Organization" (Continued)	Made the following bit name changes in the I2C1, I2C3, I2C4 and I2C5 Register Map (Table 4-11):
	 I2C3BRG SFR: I2C1BRG was changed to I2C3BRG I2C4BRG SFR: I2C1BRG was changed to I2C4BRG I2C5BRG SFR: I2C1BRG was changed to I2C5BRG I2C4TRN SFR: I2CT1DATA was changed to I2CT2ADATA I2C4RCV SFR: I2CR2DATA was changed to I2CR2ADATA I2C5TRN SFR: I2CT1DATA was changed to I2CT3ADATA I2C5RCV SFR: I2CR1DATA was changed to I2CR3ADATA
	Added the RTSMD bit and UEN<1:0> bits to the UART1A, UART1B, UART2A, UART2B, UART3A and UART3B Register Map (Table 4-13)
	Added the SIDL bit to the DMA Global Register Map (Table 4-17).
	Changed the CM bit to CMR in the System Control Register Map (Table 4-23).
	Added the following devices to the I2C2, SPI1, PORTA, PORTC, PORTD, PORTE, PORTF, PORTG, Change Notice and Pull-up Register Maps (Table 4-12, Table 4-14, Table 4-24, Table 4-27, Table 4-29, Table 4-31, Table 4-33, Table 4-35 and Table 4-36):
	 PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX664F064L PIC32MX664F128L PIC32MX764F128L
	Added the following devices to the PORTC, PORTD, PORTE, PORTF, PORTG, Change Notice and Pull-up Register Maps (Table 4-26, Table 4-28, Table 4-30, Table 4-32, Table 4-34 and Table 4-37):
	 PIC32MX534F064H PIC32MX564F064H PIC32MX564F128H PIC32MX664F064H PIC32MX664F128H PIC32MX764F128H
	Added the following devices to the CAN1 Register Map (Table 4-45):
	 PIC32MX534F064H PIC32MX564F064H PIC32MX564F128H PIC32MX764F128H PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX764F128L
	Added the following devices to the Ethernet Controller Register Map (Table 4-47):
	 PIC32MX664F064H PIC32MX664F128H PIC32MX764F128H PIC32MX664F064L PIC32MX664F128L PIC32MX664F128L