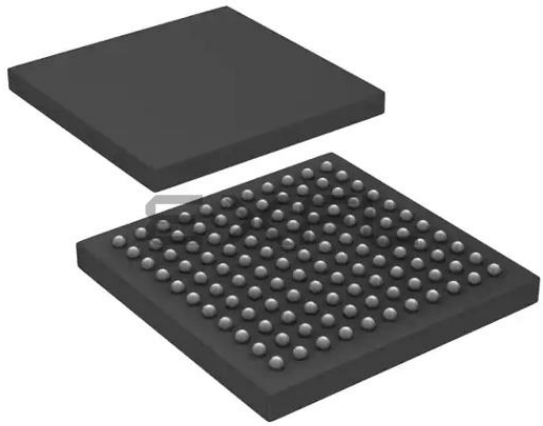
Microchip Technology - PIC32MX664F064L-I/BG Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx664f064l-i-bg

TABLE 10: PIN NAMES FOR USB AND CAN DEVICES

121-PIN TFBGA (BOTTOM VIEW)

L11

PIC32MX534F064L
PIC32MX564F064L
PIC32MX564F128L
PIC32MX575F256L
PIC32MX575F512L

L1

A11

Note: The TFBGA package skips from row "H" to row "J" and has no "I" row.

A1

Pin #	Full Pin Name	Pin #	Full Pin Name
A1	PMD4/RE4	E2	T4CK/RC3
A2	PMD3/RE3	E3	SCK2/U6TXU6TX/U3RTS/PMA5/CN8/RG6
A3	TRD0/RG13	E4	T3CK/RC2
A4	PMD0/RE0	E5	VDD
A5	PMD8/RG0	E6	PMD9/RG1
A6	C1TX/PMD10/RF1	E7	VSS
A7	VDD	E8	SDA1/INT4/RA15
A8	VSS	E9	RTCC/IC1/RD8
A9	IC5/PMD12/RD12	E10	SS1/IC2/RD9
A10	OC3/RD2	E11	SCL1/INT3/RA14
A11	OC2/RD1	F1	MCLR
B1	No Connect (NC)	F2	SCL4/SDO2/U3TX/PMA3/CN10/RG8
B2	RG15	F3	SS2/U6RX/U3CTS/PMA2/CN11/RG9
B3	PMD2/RE2	F4	SDA4/SDI2/U3RX/PMA4/CN9/RG7
B4	PMD1/RE1	F5	VSS
B5	TRD3/RA7	F6	No Connect (NC)
B6	C1RX/PMD11/RF0	F7	No Connect (NC)
B7	VCAP	F8	VDD
B8	PMRD/CN14/RD5	F9	OSC1/CLKI/RC12
B9	OC4/RD3	F10	VSS
B10	VSS	F11	OSC2/CLKO/RC15
B11	SOSCO/T1CK/CN0/RC14	G1	INT1/RE8
C1	PMD6/RE6	G2	INT2/RE9
C2	VDD	G3	TMS/RA0
C3	TRD1/RG12	G4	No Connect (NC)
C4	TRD2/RG14	G5	VDD
C5	TRCLK/RA6	G6	VSS
C6	No Connect (NC)	G7	VSS
C7	PMD15/CN16/RD7	G8	No Connect (NC)
C8	OC5/PMWR/CN13/RD4	G9	TDO/RA5
C9	VDD	G10	SDA2/RA3
C10	SOSCI/CN1/RC13	G11	TDI/RA4
C11	IC4/PMCS1/PMA14/RD11	H1	AN5/C1IN+/VBUSON/CN7/RB5
D1	T2CK/RC1	H2	AN4/C1IN-/CN6/RB4
D2	PMD7/RE7	H3	VSS
D3	PMD5/RE5	H4	VDD
D4	VSS	H5	No Connect (NC)
D5	VSS	H6	VDD
D6	No Connect (NC)	H7	No Connect (NC)
D7	PMD14/CN15/RD6	H8	VBUS
D8	PMD13/CN19/RD13	H9	VUSB3V3
D9	SDO1/OC1/INT0/RD0	H10	D+/RG2
D10	No Connect (NC)	H11	SCL2/RA2
D11	SCK1/IC3/PMCS2/PMA15/RD10	J1	AN3/C2IN+/CN5/RB3
E1	T5CK/SDI1/RC4	J2	AN2/C2IN-/CN4/RB2

Note 1: Shaded pins are 5V tolerant.

1.0 DEVICE OVERVIEW

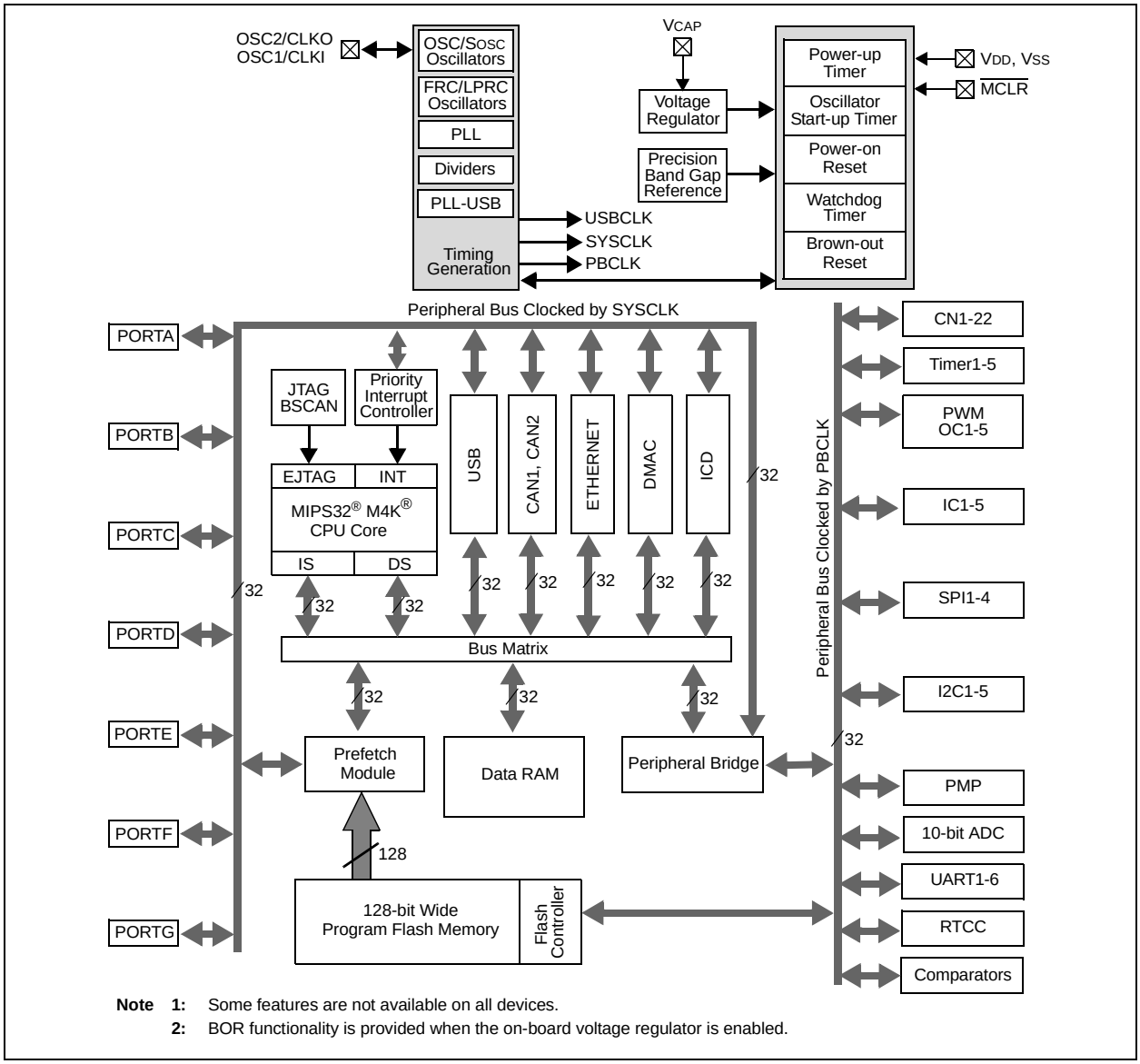
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX5XX/6XX/7XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX5XX/6XX/7XX family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM(1,2)



Note 1: Some features are not available on all devices.
2: BOR functionality is provided when the on-board voltage regulator is enabled.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
AC2TX	—	7	E4	B4	O	—	Alternate CAN2 bus transmit pin
ERXD0	61	41	J7	B23	I	ST	Ethernet Receive Data 0[2]
ERXD1	60	42	L7	A28	I	ST	Ethernet Receive Data 1[2]
ERXD2	59	43	K7	B24	I	ST	Ethernet Receive Data 2[2]
ERXD3	58	44	L8	A29	I	ST	Ethernet Receive Data 3[2]
ERXERR	64	35	J5	B20	I	ST	Ethernet receive error input[2]
ERXDV	62	12	F2	A8	I	ST	Ethernet receive data valid[2]
ECRSDV	62	12	F2	A8	I	ST	Ethernet carrier sense data valid[2]
ERXCLK	63	14	F3	A9	I	ST	Ethernet receive clock[2]
EREFCLK	63	14	F3	A9	I	ST	Ethernet reference clock[2]
ETXD0	2	88	A6	A60	O	—	Ethernet Transmit Data 0[2]
ETXD1	3	87	B6	B49	O	—	Ethernet Transmit Data 1[2]
ETXD2	43	79	A9	B43	O	—	Ethernet Transmit Data 2[2]
ETXD3	42	80	D8	A54	O	—	Ethernet Transmit Data 3[2]
ETXERR	54	89	E6	B50	O	—	Ethernet transmit error[2]
ETXEN	1	83	D7	B45	O	—	Ethernet transmit enable[2]
ETXCLK	55	84	C7	A56	I	ST	Ethernet transmit clock[2]
ECOL	44	10	E3	A7	I	ST	Ethernet collision detect[2]
ECRS	45	11	F4	B6	I	ST	Ethernet carrier sense[2]
EMDC	30	71	C11	A46	O	—	Ethernet management data clock[2]
EMDIO	49	68	E9	B37	I/O	—	Ethernet management data[2]
AERXD0	43	18	G1	A11	I	ST	Alternate Ethernet Receive Data 0[2]
AERXD1	42	19	G2	B10	I	ST	Alternate Ethernet Receive Data 1[2]
AERXD2	—	28	L2	A21	I	ST	Alternate Ethernet Receive Data 2[2]
AERXD3	—	29	K3	B17	I	ST	Alternate Ethernet Receive Data 3[2]
AERXERR	55	1	B2	A2	I	ST	Alternate Ethernet receive error input[2]
AERXDV	—	12	F2	A8	I	ST	Alternate Ethernet receive data valid[2]
AECRSDV	44	12	F2	A8	I	ST	Alternate Ethernet carrier sense data valid[2]
AERXCLK	—	14	F3	A9	I	ST	Alternate Ethernet receive clock[2]
AEREFCLK	45	14	F3	A9	I	ST	Alternate Ethernet reference clock[2]
AETXD0	59	47	L9	B26	O	—	Alternate Ethernet Transmit Data 0[2]
AETXD1	58	48	K9	A31	O	—	Alternate Ethernet Transmit Data 1[2]
AETXD2	—	44	L8	A29	O	—	Alternate Ethernet Transmit Data 2[2]
AETXD3	—	43	K7	B24	O	—	Alternate Ethernet Transmit Data 3[2]
AETXERR	—	35	J5	B20	O	—	Alternate Ethernet transmit error[2]
AETXEN	54	67	E8	A44	O	—	Alternate Ethernet transmit enable[2]
AETXCLK	—	66	E11	B36	I	ST	Alternate Ethernet transmit clock[2]
AECOL	—	42	L7	A28	I	ST	Alternate Ethernet collision detect[2]

Legend: CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = TTL input buffer; Analog = Analog input; O = Output; P = Power; I = Input

Note 1: Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

2: See **25.0 "Ethernet Controller"** for more information.

6.0 RESETS

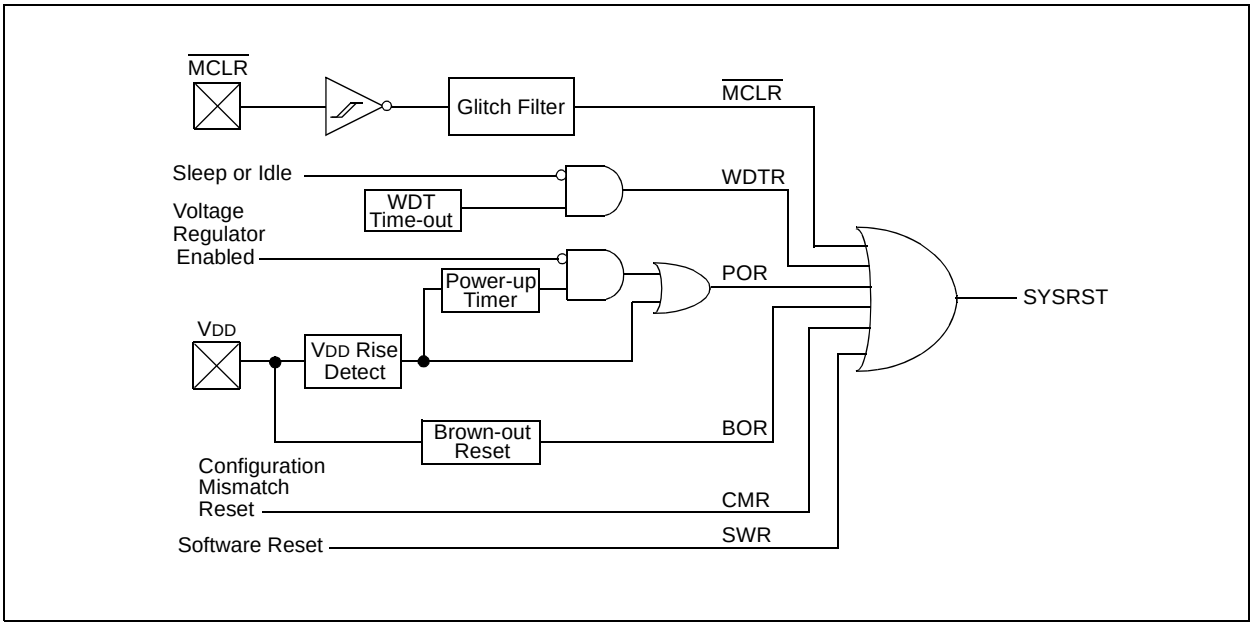
Note:	This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- Power-on Reset (POR)
- Master Clear Reset pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



8.1 Control Registers

TABLE 8-1: OSCILLATOR REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets(2)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F000	OSCCON	31:16	—	—	PLLODIV<2:0>			FRCDIV<2:0>			—	SOSCRDY	—	PBDIV<1:0>		PLLMULT<2:0>			0000
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK	SLOCK	SLPEN	CF	UFRCEN	SOSCEN	OSWEN	0000
F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
32A0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
32B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
32C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
32D0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
32E0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
32F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
3360	DCH4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3370	DCH4ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3380	DCH4INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3390	DCH4SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
33A0	DCH4DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
35F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

15.1 Control Registers

TABLE 15-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets(2)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					—	WDTCLR	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

17.1 Control Registers

TABLE 17-1: OUTPUT COMPARE 1-OUTPUT COMPARE 5 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
3020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
3200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
3220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
3400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
3420	OC3RS	31:16	OC3RS<31:0>																xxxx
		15:0																	xxxx
3600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
3620	OC4RS	31:16	OC4RS<31:0>																xxxx
		15:0																	xxxx
3800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
3820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

REGISTER 17-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT(2)	OCTSEL	OCM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Module On bit(1)
- 1 = Output Compare module is enabled
- 0 = Output Compare module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when CPU enters Idle mode
- 0 = Continue operation when CPU is in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(2)
- 1 = PWM Fault condition has occurred (only cleared in hardware)
- 0 = PWM Fault condition has not occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit
- 1 = Timer3 is the clock source for this Output Compare module
- 0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only used when OCM<2:0> = 111. It is read as '0' in all other modes.

REGISTER 18-2: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	U-0	R-0	U-0	U-0	R-0
	—	—	—	—	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Set in hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (only valid when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (only valid when ENHBUF = 1)

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (only valid when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE:** RX FIFO Empty bit (only valid when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to an empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

REGISTER 24-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 25-16: ETHRXOVFLOW: ETHERNET CONTROLLER RECEIVE OVERFLOW STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVFLWCNT<15:0>:** Dropped Receive Frames Count bits

Increment counter for frames accepted by the RX filter and subsequently dropped due to internal receive error (RXFIFO overrun). This event also sets the RXOVFLW bit (ETHIRQ<0>) interrupt flag.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 25-29: EMAC1SUPP: ETHERNET CONTROLLER MAC PHY SUPPORT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
	—	—	—	—	RESETRMII(1)	—	—	SPEEDRMII(1)
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMII:** Reset RMII Logic bit(1)
1 = Reset the MAC RMII module
0 = Normal operation.

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPEEDRMII:** RMII Speed bit(1)
This bit configures the Reduced MII logic for the current operating speed.
1 = RMII is running at 100 Mbps
0 = RMII is running at 10 Mbps

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is only used for the RMII module.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 25-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR6<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR5<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits
These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits
These bits hold the fifth transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

26.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

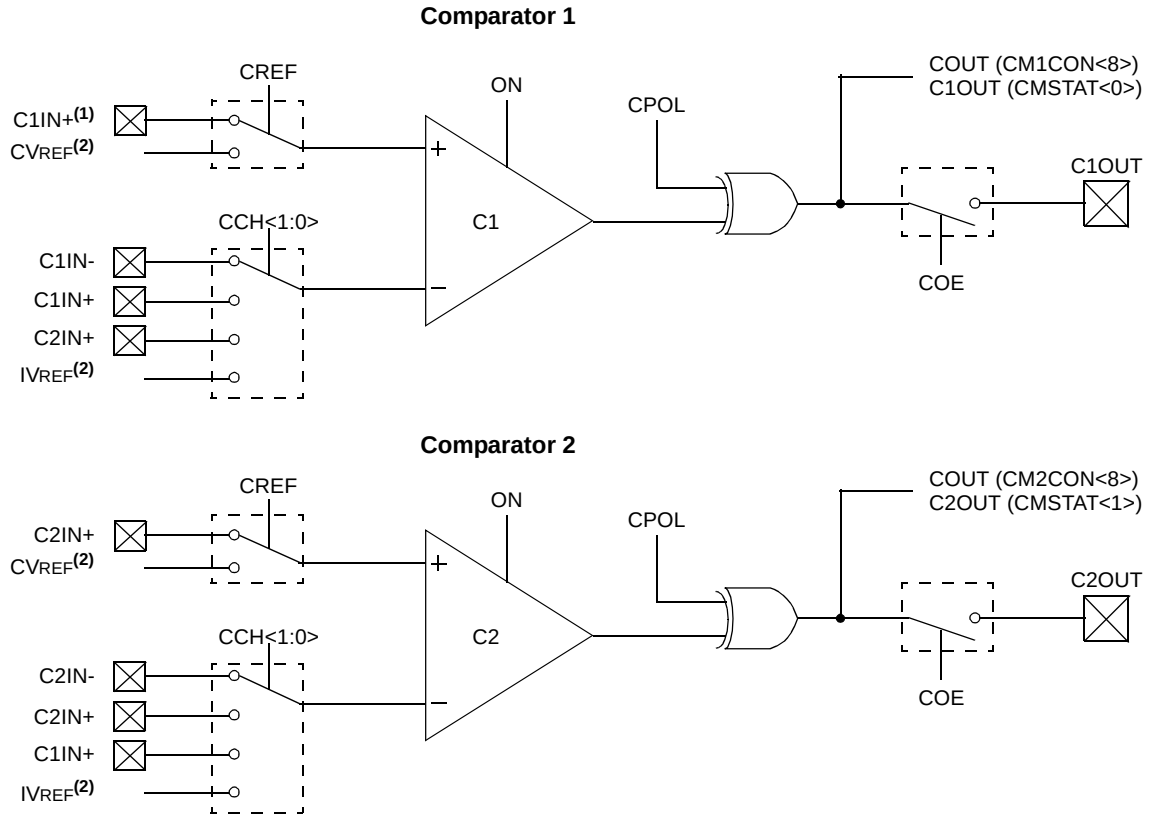
The Comparator module contains two comparators that can be configured in a variety of ways.

Key features of the Comparator module include:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the Comparator module is illustrated in Figure 26-1.

FIGURE 26-1: COMPARATOR MODULE BLOCK DIAGRAM



Note 1: On devices with a USB module, and when the module is enabled, this pin is controlled by the USB module, and therefore, is not available as a comparator input.

2: Internally connected. See **Section 27.0 "Comparator Voltage Reference (CVREF)"**.

TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Typical(3)**	**Max.**	**Units**	**Conditions**			
Operating Current (IDD)(1,2,4) for PIC32MX575/675/695/775/795 Family Devices							
DC20	6	9	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	4 MHz
DC20b	7	10			+105ºC		
DC20a	4	—		Code executing from SRAM	—		
DC21	37	40	mA	Code executing from Flash	—	—	25 MHz
DC21a	25	—		Code executing from SRAM			
DC22	64	70	mA	Code executing from Flash	—	—	60 MHz
DC22a	61	—		Code executing from SRAM			
DC23	85	98	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	80 MHz
DC23b	90	120			+105ºC		
DC23a	85	—		Code executing from SRAM	—		
DC25a	125	150	µA	—	+25°C	3.3V	LPRC (31 kHz)

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

TABLE 32-18: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 2.3V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	3.92	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes
OS51	FSYS	On-Chip VCO System Frequency	60	—	120	MHz	—
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	—
OS53	DCLK	CLKO Stability(2) (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 80 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{80}{20}}} = \frac{D_{CLK}}{2}$$

TABLE 32-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz(1) for PIC32MX575/675/695/775/795 Family Devices						
F20a	FRC	-2	—	+2	%	—
Internal FRC Accuracy @ 8.00 MHz(1) for PIC32MX534/564/664/764 Family Devices						
F20b	FRC	-0.9	—	+0.9	%	—

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

TABLE B-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
4.0 "Memory Organization"	Updated all register tables to include the Virtual Address and All Resets columns. Updated the title of Figure 4-4 to include the PIC32MX575F256L device. Updated the title of Figure 4-6 to include the PIC32MX695F512L and PIC32MX695F512H devices. Also changed PIC32MX795F512L to PIC32MX795F512**H**. Updated the title of Table 4-3 to include the PIC32MX695F512H device. Updated the title of Table 4-5 to include the PIC32MX575F5256L device. Updated the title of Table 4-6 to include the PIC32MX695F512L device. Reversed the order of Table 4-11 and Table 4-12. Reversed the order of Table 4-14 and Table 4-15. Updated the title of Table 4-15 to include the PIC32MX575F256L and PIC32MX695F512L devices. Updated the title of Table 4-45 to include the PIC32MX575F256L device. Updated the title of Table 4-47 to include the PIC32MX695F512H and PIC32MX695F512L devices.
1.0 "I/O Ports"	Updated the second paragraph of **1.1.2 "Digital Inputs"** and removed Table 12-1.
22.0 "10-bit Analog-to-Digital Converter (ADC)"	Updated the ADC Conversion Clock Period Block Diagram (see Figure 22-2).
1.0 "Special Features"	Removed references to the ENVREG pin in **1.3 "On-Chip Voltage Regulator"**. Updated the first sentence of **1.3.1 "On-Chip Regulator and POR"** and **1.3.2 "On-Chip Regulator and BOR"**. Updated the Connections for the On-Chip Regulator (see Figure 1-2).
1.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings and added Note 3. Added Thermal Packaging Characteristics for the 121-pin XBGA package (see Table 1-3). Updated the Operating Current (I_{DD}) DC Characteristics (see Table 1-5). Updated the Idle Current (I_{IDLE}) DC Characteristics (see Table 1-6). Updated the Power-Down Current (I_{PD}) DC Characteristics (see Table 1-7). Removed Note 1 from the Program Flash Memory Wait State Characteristics (see Table 1-12). Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics, changing SP52 to SP35 between the MSb and Bit 14 on SDOx (see Figure 1-13).
1.0 "Packaging Information"	Added the 121-pin XBGA package marking information and package details.
"Product Identification System"	Added the definition for BG (121-lead 10x10x1.1 mm, XBGA). Added the definition for Speed.