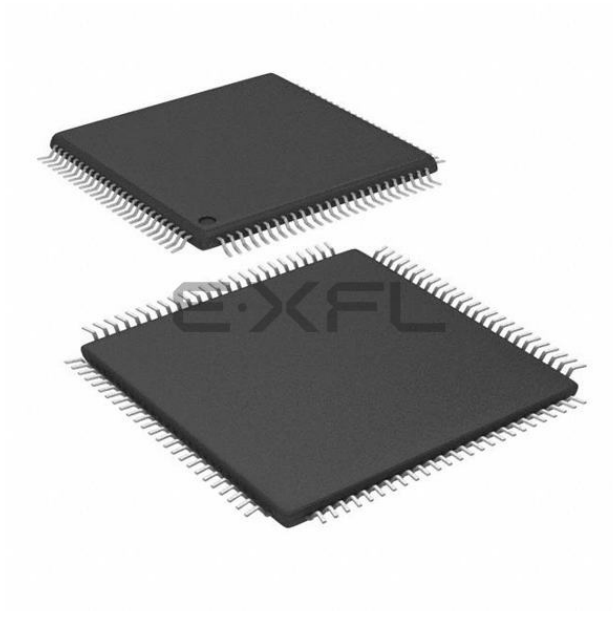

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Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx664f064l-v-pt

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1) 64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA	Pin Type	Buffer Type	Description
RG0	—	90	A5	A61	I/O	ST	PORTG is a bidirectional I/O port
RG1	—	89	E6	B50	I/O	ST	
RG6	4	10	E3	A7	I/O	ST	
RG7	5	11	F4	B6	I/O	ST	
RG8	6	12	F2	A8	I/O	ST	
RG9	8	14	F3	A9	I/O	ST	
RG12	—	96	C3	A65	I/O	ST	
RG13	—	97	A3	B55	I/O	ST	
RG14	—	95	C4	B54	I/O	ST	
RG15	—	1	B2	A2	I/O	ST	
RG2	37	57	H10	B31	I	ST	PORTG input pins
RG3	36	56	J11	A38	I	ST	
T1CK	48	74	B11	B40	I	ST	Timer1 external clock input
T2CK	—	6	D1	A5	I	ST	Timer2 external clock input
T3CK	—	7	E4	B4	I	ST	Timer3 external clock input
T4CK	—	8	E2	A6	I	ST	Timer4 external clock input
T5CK	—	9	E1	B5	I	ST	Timer5 external clock input
$\overline{\text{U1CTS}}$	43	47	L9	B26	I	ST	UART1 clear to send
$\overline{\text{U1RTS}}$	49	48	K9	A31	O	—	UART1 ready to send
U1RX	50	52	K11	A36	I	ST	UART1 receive
U1TX	51	53	J10	B29	O	—	UART1 transmit
$\overline{\text{U3CTS}}$	8	14	F3	A9	I	ST	UART3 clear to send
$\overline{\text{U3RTS}}$	4	10	E3	A7	O	—	UART3 ready to send
U3RX	5	11	F4	B6	I	ST	UART3 receive
U3TX	6	12	F2	A8	O	—	UART3 transmit
$\overline{\text{U2CTS}}$	21	40	K6	A27	I	ST	UART2 clear to send
$\overline{\text{U2RTS}}$	29	39	L6	B22	O	—	UART2 ready to send
U2RX	31	49	L10	B27	I	ST	UART2 receive
U2TX	32	50	L11	A32	O	—	UART2 transmit
U4RX	43	47	L9	B26	I	ST	UART4 receive
U4TX	49	48	K9	A31	O	—	UART4 transmit
U6RX	8	14	F3	A9	I	ST	UART6 receive
U6TX	4	10	E3	A7	O	—	UART6 transmit
U5RX	21	40	K6	A27	I	ST	UART5 receive
U5TX	29	39	L6	B22	O	—	UART5 transmit
SCK1	—	70	D11	B38	I/O	ST	Synchronous serial clock input/output for SPI1

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

2: See **25.0 "Ethernet Controller"** for more information.

TABLE 7-5: INTERRUPT REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L PIC32MX575F512L AND PIC32MX575F256L DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	SPI1TXIF	SPI1RXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	IC3EIF	IC2EIF	IC1EIF	—	—	CAN1IF	USBIF	FCEIF	DMA7IF(2)	DMA6IF(2)	DMA5IF(2)	DMA4IF(2)	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	SPI1TXIE	SPI1RXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	IC3EIE	IC2EIE	IC1EIE	—	—	CAN1IE	USBIE	FCEIE	DMA7IE(2)	DMA6IE(2)	DMA5IE(2)	DMA4IE(2)	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: These bits are not available on PIC32MX534/564 devices.

3: This register does not have associated CLR, SET, and INV registers.

TABLE 7-5: INTERRUPT REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L PIC32MX575F512L AND PIC32MX575F256L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>		—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		—	—	—	U1IP<2:0> SPI3IP<2:0> I2C3IP<2:0>			U1IS<1:0> SPI3IS<1:0> I2C3IS<1:0>		0000
1100	IPC7	31:16	—	—	—	U3IP<2:0> SPI2IP<2:0> I2C4IP<2:0>			U3IS<1:0> SPI2IS<1:0> I2C4IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>		—	—	—	U2IP<2:0> SPI4IP<2:0> I2C5IP<2:0>			U2IS<1:0> SPI4IS<1:0> I2C5IS<1:0>		0000
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
1130	IPC10	31:16	—	—	—	DMA7IP<2:0>(2)			DMA7IS<1:0>(2)		—	—	—	DMA6IP<2:0>(2)			DMA6IS<1:0>(2)		0000
		15:0	—	—	—	DMA5IP<2:0>(2)			DMA5IS<1:0>(2)		—	—	—	DMA4IP<2:0>(2)			DMA4IS<1:0>(2)		0000
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000
1150	IPC12	31:16	—	—	—	U5IP<2:0>			U5IS<1:0>		—	—	—	U6IP<2:0>			U6IS<1:0>		0000
		15:0	—	—	—	U4IP<2:0>			U4IS<1:0>		—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: These bits are not available on PIC32MX534/564 devices.

3: This register does not have associated CLR, SET, and INV registers.

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

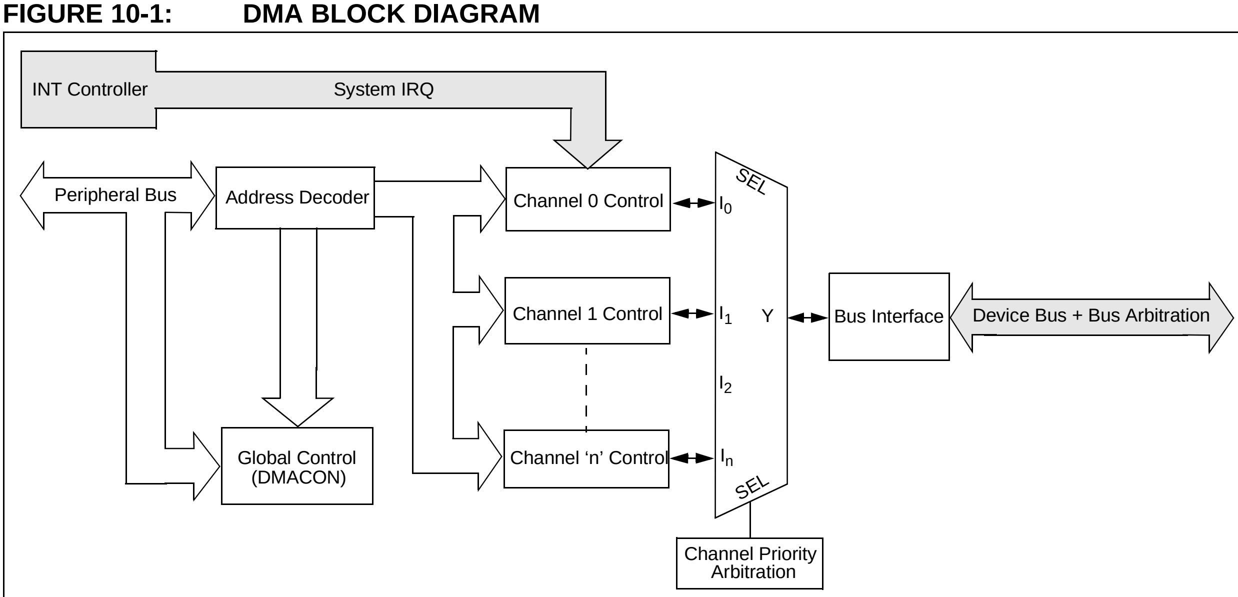
Note:	This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as SPI, UART, PMP, etc.) or memory itself.

Following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



REGISTER 11-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write ‘1’ to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **IDIF:** ID State Change Indicator bit
1 = Change in ID state detected
0 = No change in ID state detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
1 = 1 millisecond timer has expired
0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
1 = USB line state has been stable for 1 ms, but different from last time
0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
1 = VBUS voltage has dropped below the session end level
0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
1 = A change on the session end input was detected
0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
1 = Change on the session valid input detected
0 = No change on the session valid input detected

REGISTER 11-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
	ENDPT<3:0>				DIR	PPBI	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits
(Represents the number of the BDT, updated by the last USB transfer.)
1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last Buffer Descriptor Direction Indicator bit
1 = Last transaction was a transmit transfer (TX)
0 = Last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong Buffer Descriptor Pointer Indicator bit
1 = The last transaction was to the Odd buffer descriptor bank
0 = The last transaction was to the Even buffer descriptor bank

bit 1-0 **Unimplemented:** Read as ‘0’

Note: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when U1IR<TRNIF> is active. Clearing the U1IR<TRNIF> bit advances the FIFO. Data in register is invalid when U1IR<TRNIF> = 0.

REGISTER 11-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
	UTEYE	UOEMON	—	USBSIDL	—	—	—	UASUSPND

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit
1 = Eye-Pattern Test is enabled
0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB $\overline{\text{OE}}$ Monitor Enable bit
1 = $\overline{\text{OE}}$ signal is active; it indicates intervals during which the D+/D- lines are driving
0 = $\overline{\text{OE}}$ signal is inactive

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **USBSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 3-1 **Unimplemented:** Read as ‘0’

bit 0 **UASUSPND:** Automatic Suspend Enable bit
1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 11-5.
0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock.

REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON(1,2)	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	—	SWDTPS<4:0>					WDTWINEN	WDTCLR

Legend:	y = Values set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Watchdog Timer Enable bit(1,2)
1 = Enables the WDT if it is not enabled by the device configuration
0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as ‘0’

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit
1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit
1 = Writing a ‘1’ will clear the WDT
0 = Software cannot force this bit to a ‘0’

Note 1: A read of this bit results in a ‘1’ if the Watchdog Timer is enabled by the device configuration or software.

2: When using the 1:1 PBCLK divisor, the user’s software should not read or write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

REGISTER 17-1: OCxCON: OUTPUT COMPARE ‘x’ CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON[(1)]	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT[(2)]	OCTSEL	OCM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Output Compare Module On bit[(1)]
1 = Output Compare module is enabled
0 = Output Compare module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters Idle mode
0 = Continue operation when CPU is in Idle mode

bit 12-6 **Unimplemented:** Read as ‘0’

bit 5 **OC32:** 32-bit Compare Mode bit
1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit[(2)]
1 = PWM Fault condition has occurred (only cleared in hardware)
0 = PWM Fault condition has not occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit
1 = Timer3 is the clock source for this Output Compare module
0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
111 = PWM mode on OCx; Fault pin enabled
110 = PWM mode on OCx; Fault pin disabled
101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
100 = Initialize OCx pin low; generate single output pulse on OCx pin
011 = Compare event toggles OCx pin
010 = Initialize OCx pin high; compare event forces OCx pin low
001 = Initialize OCx pin low; compare event forces OCx pin high
000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using the 1:1 PBCLK divisor, the user’s software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

2: This bit is only used when OCM<2:0> = 111. It is read as ‘0’ in all other modes.

REGISTER 22-3: RTCTIME: RTC TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **HR10<3:0>:** Binary-Coded Decimal Value of Hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary-Coded Decimal Value of Hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary-Coded Decimal Value of Minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary-Coded Decimal Value of Minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary-Coded Decimal Value of Seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary-Coded Decimal Value of Seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as ‘0’

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

REGISTER 22-4: RTCDATE: RTC DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<3:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **YEAR10<3:0>:** Binary-Coded Decimal Value of Years bits, 10 digits

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1 digit

bit 23-20 **MONTH10<3:0>:** Binary-Coded Decimal Value of Months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary-Coded Decimal Value of Days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary-Coded Decimal Value of Days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **WDAY01<3:0>:** Binary-Coded Decimal Value of Weekdays bits,1 digit; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

REGISTER 24-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘0’.

REGISTER 24-19: CiFIFOBA: CAN MESSAGE BUFFER BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CiFIFOBA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CiFIFOBA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CiFIFOBA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0(1)	R-0(1)
	CiFIFOBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CiFIFOBA<31:0>:** CAN FIFO Base Address bits

These bits define the base address of all message buffers. Individual message buffers are located based on the size of the previous message buffers. This address is a physical address. Bits <1:0> are read-only and read as ‘0’, forcing the messages to be 32-bit word-aligned in device RAM.

Note 1: This bit is unimplemented and will always read ‘0’, which forces word-alignment of messages.

Note:	This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

REGISTER 25-13: ETHIEN: ETHERNET CONTROLLER INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	TXBUSEIE(1)	RXBUSEIE(2)	—	—	—	EWMARKIE(2)	FWMARKIE(2)
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONEIE(2)	PKTPENDIE(2)	RXACTIE(2)	—	TXDONEIE(1)	TXABORTIE(1)	RXBUFNAIE(2)	RXOVFLWIE(2)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14 **TXBUSEIE:** Transmit BVCI Bus Error Interrupt Enable bit(1)
1 = Enable TXBUS Error Interrupt
0 = Disable TXBUS Error Interrupt

bit 13 **RXBUSEIE:** Receive BVCI Bus Error Interrupt Enable bit(2)
1 = Enable RXBUS Error Interrupt
0 = Disable RXBUS Error Interrupt

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **EWMARKIE:** Empty Watermark Interrupt Enable bit(2)
1 = Enable EWMARK Interrupt
0 = Disable EWMARK Interrupt

bit 8 **FWMARKIE:** Full Watermark Interrupt Enable bit(2)
1 = Enable FWMARK Interrupt
0 = Disable FWMARK Interrupt

bit 7 **RXDONEIE:** Receiver Done Interrupt Enable bit(2)
1 = Enable RXDONE Interrupt
0 = Disable RXDONE Interrupt

bit 6 **PKTPENDIE:** Packet Pending Interrupt Enable bit(2)
1 = Enable PKTPEND Interrupt
0 = Disable PKTPEND Interrupt

bit 5 **RXACTIE:** RX Activity Interrupt Enable bit
1 = Enable RXACT Interrupt
0 = Disable RXACT Interrupt

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **TXDONEIE:** Transmitter Done Interrupt Enable bit(1)
1 = Enable TXDONE Interrupt
0 = Disable TXDONE Interrupt

bit 2 **TXABORTIE:** Transmitter Abort Interrupt Enable bit(1)
1 = Enable TXABORT Interrupt
0 = Disable TXABORT Interrupt

bit 1 **RXBUFNAIE:** Receive Buffer Not Available Interrupt Enable bit(2)
1 = Enable RXBUFNA Interrupt
0 = Disable RXBUFNA Interrupt

bit 0 **RXOVFLWIE:** Receive FIFO Overflow Interrupt Enable bit(2)
1 = Enable RXOVFLW Interrupt
0 = Disable RXOVFLW Interrupt

Note 1: This bit is only used for TX operations.
2: This bit is only used for RX operations.

REGISTER 25-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFCNT<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ETHBUSY(1)	TXBUSY(2)	RXBUSY(2)	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

Note: BUFCNT will not be cleared when ON is set to ‘0’. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **ETHBUSY:** Ethernet Module busy bit(1)

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction
0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

bit 6 **TXBUSY:** Transmit Busy bit(2)

1 = TX logic is receiving data
0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

Note 1: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
2: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

REGISTER 25-18: ETHSCOLFRM: ETHERNET CONTROLLER SINGLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCOLFRMCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **SCOLFRMCNT<15:0>:** Single Collision Frame Count bits
Increment count for frames that were successfully transmitted on the second try.

Note 1: This register is only used for TX operations.
2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are ‘0’.
3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 26-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	C2OUT	C1OUT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Control bit
1 = All Comparator modules are disabled while in Idle mode
0 = All Comparator modules continue to operate while in Idle mode

bit 12-2 **Unimplemented:** Read as ‘0’

bit 1 **C2OUT:** Comparator Output bit
1 = Output of Comparator 2 is a ‘1’
0 = Output of Comparator 2 is a ‘0’

bit 0 **C1OUT:** Comparator Output bit
1 = Output of Comparator 1 is a ‘1’
0 = Output of Comparator 1 is a ‘0’

27.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note:	This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

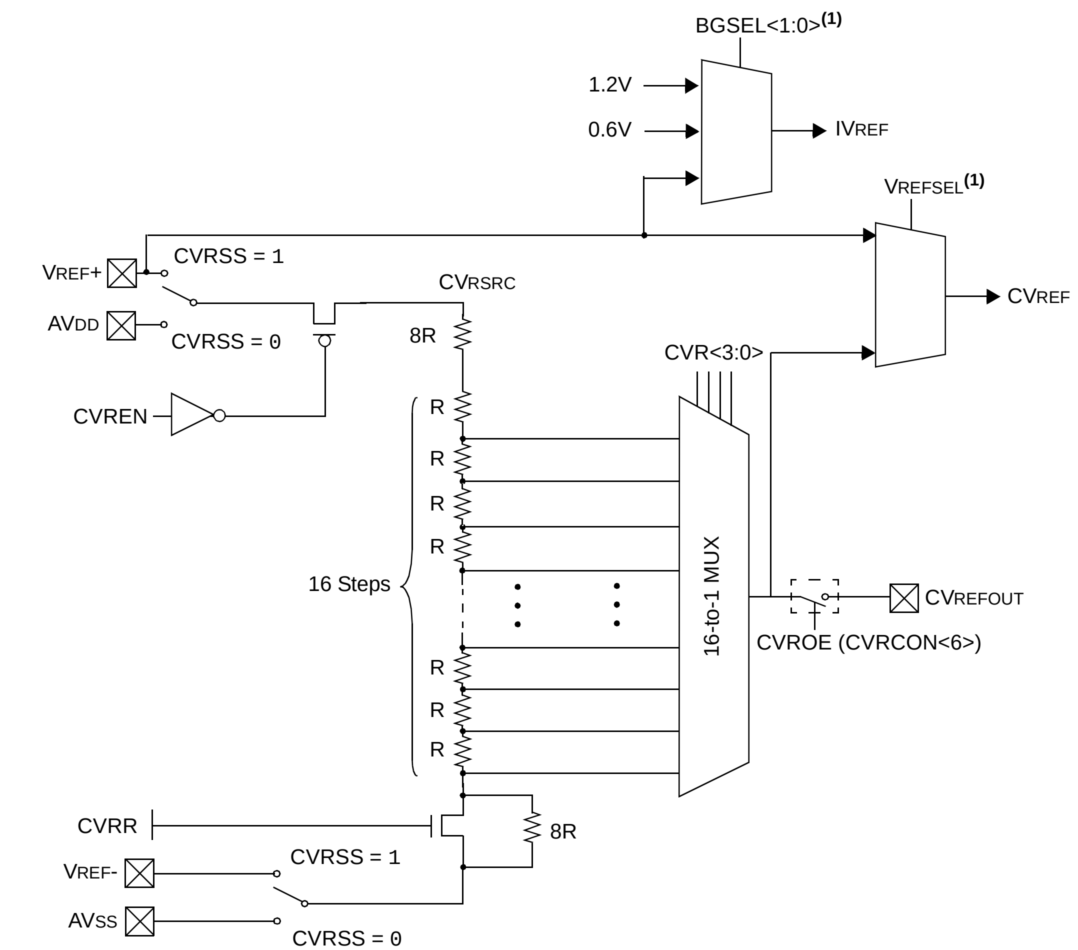
The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is illustrated in Figure 27-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

Key features of the CVREF module include:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

FIGURE 27-1: COMPARATOR VOLTAGE REFERENCE MODULE BLOCK DIAGRAM



Note 1: This bit is not available on PIC32MX575/675/695/775/795 devices. On these devices CVREF is generated by the Register network and IVREF is connected to 0.6V.

28.0 POWER-SAVING FEATURES

> **Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This section describes power-saving features for the PIC32MX5XX/6XX/7XX family of devices. These devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

28.1 Power-Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the Peripheral Bus Clock (PBCLK) and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- SOSC Run mode: the CPU is clocked from the SOSC clock source.

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

28.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- **Posc Idle mode:** the system clock is derived from the POSC. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- **FRC Idle mode:** the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- **Sosc Idle mode:** the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- **LPRC Idle mode:** the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- **Sleep mode:** the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

28.3 Power-Saving Operation

Peripherals and the CPU can be halted or disabled to further reduce power consumption.

28.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See **Section 28.3.3 "Peripheral Bus Scaling Method"** for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit, if enabled, remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)

DC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	**Typical[2]**	**Max.**	**Units**	**Conditions**		
Power-Down Current (IPD)[1] for PIC32MX534/564/664/764 Family Devices						
DC40g	12	40	μA	-40°C	2.3V	Base Power-Down Current **(Note 6)**
DC40h	20	120		+25°C		
DC40i	210	600		+85°C		
DC40o	400	1000		+105°C		
DC40j	20	120		+25°C	3.3V	Base Power-Down Current
DC40k	15	80		-40°C	3.6V	Base Power-Down Current
DC40l	20	120		+25°C		
DC40m	113	350[5]		+70°C		
DC40n	220	650		+85°C		
DC40p	500	1000		+105°C		
Module Differential Current for PIC32MX534/564/664/764 Family Devices						
DC41c	—	10	μA	—	2.5V	Watchdog Timer Current: ΔIWDT **(Notes 3,6)**
DC41d	5	—			3.3V	Watchdog Timer Current: ΔIWDT **(Note 3)**
DC41e	—	20			3.6V	Watchdog Timer Current: ΔIWDT **(Note 3)**
DC42c	—	40	μA	—	2.5V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Notes 3,6)**
DC42d	23	—			3.3V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)**
DC42e	—	50			3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)**
DC43c	—	1300	μA	—	2.5V	ADC: ΔIADC **(Notes 3,4,6)**
DC43d	1100	—			3.3V	ADC: ΔIADC **(Notes 3,4)**
DC43e	—	1300			3.6V	ADC: ΔIADC **(Notes 3,4)**

Note 1: The test conditions for IPD current measurements are as follows:
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- RTCC and JTAG are disabled

2: Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
5: Data is characterized at +70°C and not tested. Parameter is for design guidance only.
6: This parameter is characterized, but not tested in manufacturing.