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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx664f064lt-i-pf">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx664f064lt-i-pf</a>

# PIC32MX5XX/6XX/7XX

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number <sup>(1)</sup>				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
CN0	48	74	B11	B40	I	ST	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
CN1	47	73	C10	A47	I	ST	
CN2	16	25	K2	B14	I	ST	
CN3	15	24	K1	A15	I	ST	
CN4	14	23	J2	B13	I	ST	
CN5	13	22	J1	A13	I	ST	
CN6	12	21	H2	B11	I	ST	
CN7	11	20	H1	A12	I	ST	
CN8	4	10	E3	A7	I	ST	
CN9	5	11	F4	B6	I	ST	
CN10	6	12	F2	A8	I	ST	
CN11	8	14	F3	A9	I	ST	
CN12	30	44	L8	A29	I	ST	
CN13	52	81	C8	B44	I	ST	
CN14	53	82	B8	A55	I	ST	
CN15	54	83	D7	B45	I	ST	
CN16	55	84	C7	A56	I	ST	
CN17	31	49	L10	B27	I	ST	
CN18	32	50	L11	A32	I	ST	
CN19	—	80	D8	A54	I	ST	
CN20	—	47	L9	B26	I	ST	
CN21	—	48	K9	A31	I	ST	
IC1	42	68	E9	B37	I	ST	Capture Inputs 1-5
IC2	43	69	E10	A45	I	ST	
IC3	44	70	D11	B38	I	ST	
IC4	45	71	C11	A46	I	ST	
IC5	52	79	A9	A60	I	ST	
OCFA	17	26	L1	A20	I	ST	Output Compare Fault A Input
OC1	46	72	D9	B39	O	—	Output Compare Output 1
OC2	49	76	A11	A52	O	—	Output Compare Output 2
OC3	50	77	A10	B42	O	—	Output Compare Output 3
OC4	51	78	B9	A53	O	—	Output Compare Output 4
OC5	52	81	C8	B44	O	—	Output Compare Output 5
OCFB	30	44	L8	A29	I	ST	Output Compare Fault B Input
INT0	46	72	D9	B39	I	ST	External Interrupt 0
INT1	42	18	G1	A11	I	ST	External Interrupt 1
INT2	43	19	G2	B10	I	ST	External Interrupt 2
INT3	44	66	E11	B36	I	ST	External Interrupt 3
INT4	45	67	E8	A44	I	ST	External Interrupt 4

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the “**Device Pin Tables**” section for device pin availability.

**2:** See **25.0 “Ethernet Controller”** for more information.

# PIC32MX5XX/6XX/7XX

**REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST <sup>(1)</sup>

<b>Legend:</b>	HC = Cleared by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit<sup>(1)</sup>

1 = Enable software Reset event

0 = No effect

**Note 1:** The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

# PIC32MX5XX/6XX/7XX

## REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IP03<2:0>						IS03<1:0>	
23:16	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IP02<2:0>						IS02<1:0>	
15:8	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IP01<2:0>						IS01<1:0>	
7:0	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IP00<2:0>						IS00<1:0>	

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP03<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•  
•  
•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS03<1:0>:** Interrupt Sub-priority bits

11 = Interrupt sub-priority is 3

10 = Interrupt sub-priority is 2

01 = Interrupt sub-priority is 1

00 = Interrupt sub-priority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP02<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•  
•  
•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS02<1:0>:** Interrupt Sub-priority bits

11 = Interrupt sub-priority is 3

10 = Interrupt sub-priority is 2

01 = Interrupt sub-priority is 1

00 = Interrupt sub-priority is 0

bit 15-13 **Unimplemented:** Read as '0'

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

**TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)**

Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>															0000	
3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>															0000	
31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>															0000	
31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>															0000	
31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>															0000	
31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHPDAT<7:0>									0000
31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>									00FF
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00	
3200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000	
3210	DCH2SSA	31:16	CHSSA<31:0>															0000	
		15:0	CHSSA<31:0>															0000	
3220	DCH2DSA	31:16	CHDSA<31:0>															0000	
		15:0	CHDSA<31:0>															0000	
3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>															0000	
3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>															0000	
3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>															0000	
3260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>															0000	
3270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>															0000	
3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>															0000	

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- 2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

## REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO <sup>(1)</sup>	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP <sup>(1)</sup>	CRCTYP	—	—	CRCCH<2:0>		

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (reverse source byte order)

00 = No swapping (source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit<sup>(1)</sup>

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (reflected)

0 = The LFSR CRC is calculated Most Significant bit first (not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits<sup>(1)</sup>

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

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**REGISTER 10-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 CHBUSY	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 CHCHNS <sup>(1)</sup>
7:0	R/W-0 CHEN <sup>(2)</sup>	R/W-0 CHAED	R/W-0 CHCHN	R/W-0 CHAEN	U-0 —	R-0 CHEDET	R/W-0 CHPRI<1:0>	R/W-0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit

1 = Channel is active or has been enabled

0 = Channel is inactive or has been disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit<sup>(1)</sup>

1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)

0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit<sup>(2)</sup>

1 = Channel is enabled

0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit

1 = Channel start/abort events will be registered, even if the channel is disabled

0 = Channel start/abort events will be ignored if the channel is disabled

bit **CHCHN:** Channel Chain Enable bit

1 = Allow channel to be chained

0 = Do not allow channel to be chained

bit 4 **CHAEN:** Channel Automatic Enable bit

1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete

0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit

1 = An event has been detected

0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits

11 = Channel has priority 3 (highest)

10 = Channel has priority 2

01 = Channel has priority 1

00 = Channel has priority 0

**Note 1:** The chain selection bit takes effect when chaining is enabled (CHCHN = 1).

**2:** When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

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NOTES:



## 18.1 Control Registers

**TABLE 18-1: SPI1 THROUGH SPI4 REGISTER MAP**

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
5E00	SPI1CON <sup>(2)</sup>	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5E10	SPI1STAT <sup>(2)</sup>	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5E20	SPI1BUF <sup>(2)</sup>	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5E30	SPI1BRG <sup>(2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5800	SPI3CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5810	SPI3STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5820	SPI3BUF	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5830	SPI3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5A10	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5A20	SPI2BUF	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									
5C00	SPI4CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSSEN	FRMSYPW	FRMCNT<2:0>			—	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	STXISEL<1:0>		SRXISEL<1:0>		0000
5C10	SPI4STAT	31:16	—	—	—	RXBUFELM<4:0>				—	—	—	TXBUFELM<4:0>					0000	
		15:0	—	—	—	—	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5C20	SPI4BUF	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5C30	SPI4BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register is not available on 64-pin devices.

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## REGISTER 19-2: I2CxSTAT: I<sup>2</sup>C STATUS REGISTER (CONTINUED)

- bit 5     **D\_A**: Data/Address bit (when operating as I<sup>2</sup>C slave)  
This bit is cleared by hardware upon a device address match, and is set by hardware by reception of the slave byte.  
1 = Indicates that the last byte received was data  
0 = Indicates that the last byte received was device address
- bit 4     **P**: Stop bit  
This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected.  
1 = Indicates that a Stop bit has been detected last  
0 = Stop bit was not detected last
- bit 3     **S**: Start bit  
This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected.  
1 = Indicates that a Start (or Repeated Start) bit has been detected last  
0 = Start bit was not detected last
- bit 2     **R\_W**: Read/Write Information bit (when operating as I<sup>2</sup>C slave)  
This bit is set or cleared by hardware after reception of an I<sup>2</sup>C device address byte.  
1 = Read – indicates data transfer is output from slave  
0 = Write – indicates data transfer is input to slave
- bit 1     **RBF**: Receive Buffer Full Status bit  
This bit is set by hardware when the I2CxRCV register is written with a received byte, and is cleared by hardware when software reads I2CxRCV.  
1 = Receive complete, I2CxRCV is full  
0 = Receive not complete, I2CxRCV is empty
- bit 0     **TBF**: Transmit Buffer Full Status bit  
This bit is set by hardware when software writes to the I2CxTRN register, and is cleared by hardware upon completion of data transmission.  
1 = Transmit in progress, I2CxTRN is full  
0 = Transmit complete, I2CxTRN is empty

## REGISTER 22-3: RTCTIME: RTC TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **HR10<3:0>**: Binary-Coded Decimal Value of Hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>**: Binary-Coded Decimal Value of Hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>**: Binary-Coded Decimal Value of Minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>**: Binary-Coded Decimal Value of Minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>**: Binary-Coded Decimal Value of Seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>**: Binary-Coded Decimal Value of Seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented**: Read as '0'

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).

## REGISTER 24-11: CifLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)

bit 15 **FLTEN5**: Filter 17 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 14-13 **MSEL5<1:0>**: Filter 5 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 12-8 **FSEL5<4:0>**: FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

•  
•  
•

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4**: Filter 4 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 6-5 **MSEL4<1:0>**: Filter 4 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 4-0 **FSEL4<4:0>**: FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

•  
•  
•

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

<b>Note:</b> The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.
---

## REGISTER 25-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<7:0>							

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

bit 31-24 **PMM<31:24>**: Pattern Match Mask 3 bits  
bit 23-16 **PMM<23:16>**: Pattern Match Mask 2 bits  
bit 15-8 **PMM<15:8>**: Pattern Match Mask 1 bits  
bit 7-0 **PMM<7:0>**: Pattern Match Mask 0 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

## REGISTER 25-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<39:32>							

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

bit 31-24 **PMM<63:56>**: Pattern Match Mask 7 bits  
bit 23-16 **PMM<55:48>**: Pattern Match Mask 6 bits  
bit 15-8 **PMM<47:40>**: Pattern Match Mask 5 bits  
bit 7-0 **PMM<39:32>**: Pattern Match Mask 4 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

# PIC32MX5XX/6XX/7XX

## REGISTER 25-9: ETHPMCS: ETHERNET CONTROLLER PATTERN MATCH CHECKSUM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<7:0>							

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'  
bit 15-8 **PMCS<15:8>:** Pattern Match Checksum 1 bits  
bit 7-0 **PMCS<7:0>:** Pattern Match Checksum 0 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

## REGISTER 25-10: ETHPMO: ETHERNET CONTROLLER PATTERN MATCH OFFSET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<7:0>							

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'  
bit 15-0 **PMO<15:0>:** Pattern Match Offset 1 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

## REGISTER 25-22: ETHALGNERR: ETHERNET CONTROLLER ALIGNMENT ERRORS STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **ALGNERRCNT<15:0>:** Alignment Error Count bits

Increment count for frames with alignment errors. Note that an alignment error is a frame that has an FCS error and the frame length in bits is not an integral multiple of 8 bits (a.k.a., dribble nibble)

**Note 1:** This register is only used for RX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

## 31.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

## 31.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

## 31.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/librarian features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 31.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility



**TABLE 32-11: DC CHARACTERISTICS: PROGRAM MEMORY<sup>(3)</sup>**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typ. <sup>(1)</sup>	Max.	Units	Conditions
D130	EP	Cell Endurance	1000	—	—	E/W	—
D130a	EP	Cell Endurance	20,000	—	—	E/W	See <b>Note 5</b>
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	3.0	—	3.6	V	—
D132a	VPEW	VDD for Erase or Write	2.3	—	3.6	V	See <b>Note 5</b>
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
D138	TWW	Word Write Cycle Time <sup>(4)</sup>	—	411	—	FRC Cycles	—
D136	TRW	Row Write Cycle Time <sup>(2,4)</sup>	—	26067	—	FRC Cycles	—
D137	TPE	Page Erase Cycle Time <sup>(4)</sup>	—	201060	—	FRC Cycles	—
D139	TCE	Chip Erase Cycle Time <sup>(4)</sup>	—	804652	—	FRC Cycles	—

**Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

- 2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).
- 3:** Refer to “PIC32 Flash Programming Specification” (DS60001145) for operating conditions during programming and erase cycles.
- 4:** This parameter depends on the FRC accuracy (see Table 32-19) and the FRC tuning values (see Register 8-2).
- 5:** This parameter only applies to PIC32MX534/564/664/764 devices.

**TABLE 32-12: PROGRAM FLASH MEMORY WAIT STATE CHARACTERISTICS**

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp	
Required Flash Wait States	SYSCLK	Units	Comments
0 Wait State	0 to 30	MHz	—
1 Wait State	31 to 60		
2 Wait States	61 to 80		

# PIC32MX5XX/6XX/7XX

**TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical <sup>(2)</sup>	Max.	Units	Conditions
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance <sup>(4)</sup>	5	—	25	ns	—
SP52	Tsch2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	Tsck + 20	—	—	ns	—
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	25	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns.

**4:** Assumes 50 pF load on all SPIx pins.

# PIC32MX5XX/6XX/7XX

**TABLE 32-37: 10-BIT ADC CONVERSION RATE PARAMETERS**

<b>Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated)</b> Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp					
ADC Speed <sup>(2)</sup>	T <sub>AD</sub> Minimum	Sampling Time Minimum	R <sub>s</sub> Maximum	V <sub>DD</sub>	ADC Channels Configuration
1 Msps to 400 ksps <sup>(1)</sup>	65 ns	132 ns	500Ω	3.0V to 3.6V	
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	

- Note 1:** External VREF- and VREF+ pins must be used for correct operation.
- 2:** These parameters are characterized, but not tested in manufacturing.
- 3:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

# PIC32MX5XX/6XX/7XX

## Revision E (July 2010)

Minor corrections were incorporated throughout the document.

## Revision F (December 2010)

The revision includes the following global update:

VCAP/VDDCORE has been changed to: VCAP/VCORE

Other major changes are referenced by their respective chapter/section in Table B-4:

**TABLE B-4: SECTION UPDATES**

Section Name	Update Description
<b>High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers</b>	Removed the following Analog Feature: FV tolerant input pins (digital pins only)  Updated the term LIN 1.2 support as LIN support for the peripheral feature: Six UART modules with: RS-232, RS-485, and LIN support
<b>1.0 “Device Overview”</b>	Updated the value of 64-pin QFN/TQFP pin number for the following pin names: PMA0, PMA1 and ECRSDV
<b>4.0 “Memory Organization”</b>	The following register map tables were updated: <ul style="list-style-type: none"><li>• Table 4-2:<ul style="list-style-type: none"><li>- Changed bits 24/8 to I2C5BIF in IFS1</li><li>- Changed bits 24/8-24/10 to SRIPL&lt;2:0&gt; in INTSTAT</li><li>- Changed bits 25/9-24/8 to U5IS&lt;1:0&gt; in IPC12</li><li>- Added note 2</li></ul></li><li>• Table 4-3 through Table 4-7:<ul style="list-style-type: none"><li>- Changed bits 24/8-24/10 to SRIPL&lt;2:0&gt; in INTSTAT</li><li>- Changed bits 25/9-24/8 to U5IS&lt;1:0&gt; in IPC12</li></ul></li><li>• Table 4-3:<ul style="list-style-type: none"><li>- Changed bits 24/8 to I2C5BIF in IFS1</li><li>- Added note 2</li></ul></li><li>• Table 4-4:<ul style="list-style-type: none"><li>- Changed bits 24/8 to I2C5BIF in IFS1</li><li>- Changed bits 24/8 to I2C5BIE in IEC1</li><li>- Added note 2 references</li></ul></li><li>• Table 4-5:<ul style="list-style-type: none"><li>- Changed bits 24/8 to I2C5BIF in IFS1</li><li>- Changed bits 24/8 to I2C5BIE in IEC1</li><li>- Added note 2 references</li></ul></li><li>• Table 4-6:<ul style="list-style-type: none"><li>- Changed bit 24/8 to I2C5BIF in IFS1</li><li>- Updated the bit value of bit 24/8 as I2C5BIE for the IEC1 register.</li><li>- Added note 2</li></ul></li><li>• Table 4-7:<ul style="list-style-type: none"><li>- Changed bit 25/9 to I2C5SIF in IFS1</li><li>- Changed bit 24/8 as I2C5BIF in IFS1</li><li>- Changed bit 25/9 as I2C5SIE in IEC1</li><li>- Changed bit 24/8 as I2C5BIE in IEC1</li><li>- Added note 2 references</li></ul></li><li>• Added note 2 to Table 4-8</li><li>• Updated the All Resets values for the following registers in Table 4-11: I2C3CON, I2C4CON, I2C5CON and I2C1CON.</li><li>• Updated the All Resets values for the I2C2CON register in Table 4-12</li></ul>

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

	PIC32	MX	5XX	F	512	H	T	80	I / PT	XXX
Microchip Brand										
Architecture										
Product Groups										
Flash Memory Family										
Program Memory Size (KB)										
Pin Count										
Tape and Reel Flag (if applicable)										
Speed (see Note 1)										
Temperature Range										
Package										
Pattern										

  

**Example:**  
 PIC32MX575F256H-80I/PT:  
 General purpose PIC32,  
 32-bit RISC MCU,  
 256 KB program memory,  
 64-pin, Industrial temperature,  
 TQFP package.

  

**Flash Memory Family**

Architecture	MX = 32-bit RISC MCU core
Product Groups	5XX = General purpose microcontroller family 6XX = General purpose microcontroller family 7XX = General purpose microcontroller family
Flash Memory Family	F = Flash program memory
Program Memory Size	64 = 64K 128 = 128K 256 = 256K 512 = 512K
Pin Count	H = 64-pin L = 100-pin, 121-pin, 124-pin
Speed (see <b>Note 1</b> )	Blank or 80 = 80 MHz
Temperature Range	I = -40°C to +85°C (Industrial) V = -40°C to +105°C (V-Temp)
Package	PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) PF = 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack) MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat) BG = 121-Lead (10x10x1.1 mm) TFBGA (Plastic Thin Profile Ball Grid Array) TL = 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample

**Note 1:** This option is not available for PIC32MX534/564/664/764 devices.