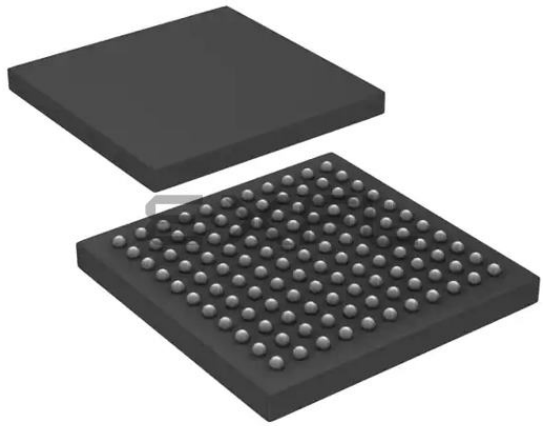
# Microchip Technology - PIC32MX664F064LT-V/BG Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | Ethernet, I²C, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-TFBGA |
| Supplier Device Package | 121-TFBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx664f064lt-v-bg |

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number[1] | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| AC2TX | — | 7 | E4 | B4 | O | — | Alternate CAN2 bus transmit pin |
| ERXD0 | 61 | 41 | J7 | B23 | I | ST | Ethernet Receive Data 0[2] |
| ERXD1 | 60 | 42 | L7 | A28 | I | ST | Ethernet Receive Data 1[2] |
| ERXD2 | 59 | 43 | K7 | B24 | I | ST | Ethernet Receive Data 2[2] |
| ERXD3 | 58 | 44 | L8 | A29 | I | ST | Ethernet Receive Data 3[2] |
| ERXERR | 64 | 35 | J5 | B20 | I | ST | Ethernet receive error input[2] |
| ERXDV | 62 | 12 | F2 | A8 | I | ST | Ethernet receive data valid[2] |
| ECRSDV | 62 | 12 | F2 | A8 | I | ST | Ethernet carrier sense data valid[2] |
| ERXCLK | 63 | 14 | F3 | A9 | I | ST | Ethernet receive clock[2] |
| EREFCLK | 63 | 14 | F3 | A9 | I | ST | Ethernet reference clock[2] |
| ETXD0 | 2 | 88 | A6 | A60 | O | — | Ethernet Transmit Data 0[2] |
| ETXD1 | 3 | 87 | B6 | B49 | O | — | Ethernet Transmit Data 1[2] |
| ETXD2 | 43 | 79 | A9 | B43 | O | — | Ethernet Transmit Data 2[2] |
| ETXD3 | 42 | 80 | D8 | A54 | O | — | Ethernet Transmit Data 3[2] |
| ETXERR | 54 | 89 | E6 | B50 | O | — | Ethernet transmit error[2] |
| ETXEN | 1 | 83 | D7 | B45 | O | — | Ethernet transmit enable[2] |
| ETXCLK | 55 | 84 | C7 | A56 | I | ST | Ethernet transmit clock[2] |
| ECOL | 44 | 10 | E3 | A7 | I | ST | Ethernet collision detect[2] |
| ECRS | 45 | 11 | F4 | B6 | I | ST | Ethernet carrier sense[2] |
| EMDC | 30 | 71 | C11 | A46 | O | — | Ethernet management data clock[2] |
| EMDIO | 49 | 68 | E9 | B37 | I/O | — | Ethernet management data[2] |
| AERXD0 | 43 | 18 | G1 | A11 | I | ST | Alternate Ethernet Receive Data 0[2] |
| AERXD1 | 42 | 19 | G2 | B10 | I | ST | Alternate Ethernet Receive Data 1[2] |
| AERXD2 | — | 28 | L2 | A21 | I | ST | Alternate Ethernet Receive Data 2[2] |
| AERXD3 | — | 29 | K3 | B17 | I | ST | Alternate Ethernet Receive Data 3[2] |
| AERXERR | 55 | 1 | B2 | A2 | I | ST | Alternate Ethernet receive error input[2] |
| AERXDV | — | 12 | F2 | A8 | I | ST | Alternate Ethernet receive data valid[2] |
| AECRSDV | 44 | 12 | F2 | A8 | I | ST | Alternate Ethernet carrier sense data valid[2] |
| AERXCLK | — | 14 | F3 | A9 | I | ST | Alternate Ethernet receive clock[2] |
| AEREFCLK | 45 | 14 | F3 | A9 | I | ST | Alternate Ethernet reference clock[2] |
| AETXD0 | 59 | 47 | L9 | B26 | O | — | Alternate Ethernet Transmit Data 0[2] |
| AETXD1 | 58 | 48 | K9 | A31 | O | — | Alternate Ethernet Transmit Data 1[2] |
| AETXD2 | — | 44 | L8 | A29 | O | — | Alternate Ethernet Transmit Data 2[2] |
| AETXD3 | — | 43 | K7 | B24 | O | — | Alternate Ethernet Transmit Data 3[2] |
| AETXERR | — | 35 | J5 | B20 | O | — | Alternate Ethernet transmit error[2] |
| AETXEN | 54 | 67 | E8 | A44 | O | — | Alternate Ethernet transmit enable[2] |
| AETXCLK | — | 66 | E11 | B36 | I | ST | Alternate Ethernet transmit clock[2] |
| AECOL | — | 42 | L7 | A28 | I | ST | Alternate Ethernet collision detect[2] |

**Legend:** CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = TTL input buffer; Analog = Analog input; O = Output; P = Power; I = Input

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.

**TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)**

| Interrupt Source(1) | IRQ Number | Vector Number | Interrupt Bit Location | | | |
|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Sub-Priority |
| AD1 – ADC1 Convert Done | 33 | 27 | IFS1<1> | IEC1<1> | IPC6<28:26> | IPC6<25:24> |
| PMP – Parallel Master Port | 34 | 28 | IFS1<2> | IEC1<2> | IPC7<4:2> | IPC7<1:0> |
| CMP1 – Comparator Interrupt | 35 | 29 | IFS1<3> | IEC1<3> | IPC7<12:10> | IPC7<9:8> |
| CMP2 – Comparator Interrupt | 36 | 30 | IFS1<4> | IEC1<4> | IPC7<20:18> | IPC7<17:16> |
| U2E – UART2 Error<br>SPI2E – SPI2 Fault<br>I2C4B – I2C4 Bus Collision Event | 37 | 31 | IFS1<5> | IEC1<5> | IPC7<28:26> | IPC7<25:24> |
| U2RX – UART2 Receiver<br>SPI2RX – SPI2 Receive Done<br>I2C4S – I2C4 Slave Event | 38 | 31 | IFS1<6> | IEC1<6> | IPC7<28:26> | IPC7<25:24> |
| U2TX – UART2 Transmitter<br>SPI2TX – SPI2 Transfer Done<br>IC4M – I2C4 Master Event | 39 | 31 | IFS1<7> | IEC1<7> | IPC7<28:26> | IPC7<25:24> |
| U3E – UART3 Error<br>SPI4E – SPI4 Fault<br>I2C5B – I2C5 Bus Collision Event | 40 | 32 | IFS1<8> | IEC1<8> | IPC8<4:2> | IPC8<1:0> |
| U3RX – UART3 Receiver<br>SPI4RX – SPI4 Receive Done<br>I2C5S – I2C5 Slave Event | 41 | 32 | IFS1<9> | IEC1<9> | IPC8<4:2> | IPC8<1:0> |
| U3TX – UART3 Transmitter<br>SPI4TX – SPI4 Transfer Done<br>IC5M – I2C5 Master Event | 42 | 32 | IFS1<10> | IEC1<10> | IPC8<4:2> | IPC8<1:0> |
| I2C2B – I2C2 Bus Collision Event | 43 | 33 | IFS1<11> | IEC1<11> | IPC8<12:10> | IPC8<9:8> |
| I2C2S – I2C2 Slave Event | 44 | 33 | IFS1<12> | IEC1<12> | IPC8<12:10> | IPC8<9:8> |
| I2C2M – I2C2 Master Event | 45 | 33 | IFS1<13> | IEC1<13> | IPC8<12:10> | IPC8<9:8> |
| FSCM – Fail-Safe Clock Monitor | 46 | 34 | IFS1<14> | IEC1<14> | IPC8<20:18> | IPC8<17:16> |
| RTCC – Real-Time Clock and Calendar | 47 | 35 | IFS1<15> | IEC1<15> | IPC8<28:26> | IPC8<25:24> |
| DMA0 – DMA Channel 0 | 48 | 36 | IFS1<16> | IEC1<16> | IPC9<4:2> | IPC9<1:0> |
| DMA1 – DMA Channel 1 | 49 | 37 | IFS1<17> | IEC1<17> | IPC9<12:10> | IPC9<9:8> |
| DMA2 – DMA Channel 2 | 50 | 38 | IFS1<18> | IEC1<18> | IPC9<20:18> | IPC9<17:16> |
| DMA3 – DMA Channel 3 | 51 | 39 | IFS1<19> | IEC1<19> | IPC9<28:26> | IPC9<25:24> |
| DMA4 – DMA Channel 4 | 52 | 40 | IFS1<20> | IEC1<20> | IPC10<4:2> | IPC10<1:0> |
| DMA5 – DMA Channel 5 | 53 | 41 | IFS1<21> | IEC1<21> | IPC10<12:10> | IPC10<9:8> |
| DMA6 – DMA Channel 6 | 54 | 42 | IFS1<22> | IEC1<22> | IPC10<20:18> | IPC10<17:16> |
| DMA7 – DMA Channel 7 | 55 | 43 | IFS1<23> | IEC1<23> | IPC10<28:26> | IPC10<25:24> |
| FCE – Flash Control Event | 56 | 44 | IFS1<24> | IEC1<24> | IPC11<4:2> | IPC11<1:0> |
| USB – USB Interrupt | 57 | 45 | IFS1<25> | IEC1<25> | IPC11<12:10> | IPC11<9:8> |
| CAN1 – Control Area Network 1 | 58 | 46 | IFS1<26> | IEC1<26> | IPC11<20:18> | IPC11<17:16> |
| CAN2 – Control Area Network 2 | 59 | 47 | IFS1<27> | IEC1<27> | IPC11<28:26> | IPC11<25:24> |
| ETH – Ethernet Interrupt | 60 | 48 | IFS1<28> | IEC1<28> | IPC12<4:2> | IPC12<1:0> |
| IC1E – Input Capture 1 Error | 61 | 5 | IFS1<29> | IEC1<29> | IPC1<12:10> | IPC1<9:8> |
| IC2E – Input Capture 2 Error | 62 | 9 | IFS1<30> | IEC1<30> | IPC2<12:10> | IPC2<9:8> |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX5XX USB and CAN Features"**, **TABLE 2: "PIC32MX6XX USB and Ethernet Features"** and **TABLE 3: "PIC32MX7XX USB, Ethernet, and CAN Features"** for the list of available peripherals.

**TABLE 7-4: INTERRUPT REGISTER MAP FOR PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF<br>SPI3TXIF<br>I2C3MIF | U1RXIF<br>SPI3RXIF<br>I2C3SIF | U1EIF<br>SPI3EIF<br>I2C3BIF | — | — | — | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | IC3EIF | IC2EIF | IC1EIF | ETHIF | CAN2IF(2) | CAN1IF | USBIF | FCEIF | DMA7IF(2) | DMA6IF(2) | DMA5IF(2) | DMA4IF(2) | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | — | — | — | U2TXIF<br>SPI4TXIF<br>I2C5MIF | U2RXIF<br>SPI4RXIF<br>I2C5SIF | U2EIF<br>SPI4EIF<br>I2C5BIF | U3TXIF<br>SPI2TXIF<br>I2C4MIF | U3RXIF<br>SPI2RXIF<br>I2C4SIF | U3EIF<br>SPI2EIF<br>I2C4BIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIF | U5RXIF | U5EIF | U6TXIF | U6RXIF | U6EIF | U4TXIF | U4RXIF | U4EIF | PMPEIF | IC5EIF | IC4EIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE<br>SPI3TXIE<br>I2C3MIE | U1RXIE<br>SPI3RXIE<br>I2C3SIE | U1EIE<br>SPI3EIE<br>I2C3BIE | — | — | — | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | IC3EIE | IC2EIE | IC1EIE | ETHIE | CAN2IE(2) | CAN1IE | USBIE | FCEIE | DMA7IE(2) | DMA6IE(2) | DMA5IE(2) | DMA4IE(2) | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | — | — | — | U2TXIE<br>SPI4TXIE<br>I2C5MIE | U2RXIE<br>SPI4RXIE<br>I2C5SIE | U2EIE<br>SPI4EIE<br>I2C5BIE | U3TXIE<br>SPI2TXIE<br>I2C4MIE | U3RXIE<br>SPI2RXIE<br>I2C4SIE | U3EIE<br>SPI2EIE<br>I2C4BIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIE | U5RXIE | U5EIE | U6TXIE | U6RXIE | U6EIE | U4TXIE | U4RXIE | U4EIE | PMPEIE | IC5EIE | IC4EIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This bit is unimplemented on PIC32MX764F128H device.

**3:** This register does not have associated CLR, SET, and INV registers.

**REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | — | — | — | — | — | — | — | SS0 |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MVEC | — | TPC<2:0> | | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-17 **Unimplemented:** Read as '0'

bit 16 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow register set
0 = Single vector is not presented with a shadow register set

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multiple Vector Configuration bit
1 = Interrupt controller configured for Multi-vector mode
0 = Interrupt controller configured for Single-vector mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
001 = Interrupts of group priority 1 start the Interrupt Proximity timer
000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

**REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | RIPL<2:0>(1) | | |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | VEC<5:0>(1) | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **RIPL<2:0>:** Requested Priority Level bits(1)

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits(1)

11111-00000 = The interrupt vector that is presented to the CPU

**Note 1:** This value should only be used when the interrupt controller is configured for Single-vector mode.

**REGISTER 7-3: TPTMR: TEMPORAL PROXIMITY TIMER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **TPTMR<31:0>:** Temporal Proximity Timer Reload bits
Used by the Temporal Proximity Timer as a reload value when the Temporal Proximity timer is triggered by an interrupt event.

**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)**

bit 12-10 **IP01<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 9-8 **IS01<1:0>:** Interrupt Sub-priority bits
11 = Interrupt sub-priority is 3
10 = Interrupt sub-priority is 2
01 = Interrupt sub-priority is 1
00 = Interrupt sub-priority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP00<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS00<1:0>:** Interrupt Sub-priority bits
11 = Interrupt sub-priority is 3
10 = Interrupt sub-priority is 2
01 = Interrupt sub-priority is 1
00 = Interrupt sub-priority is 0

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

**REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDL | TWDIS | TWIP | — | — | — |
| 7:0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
| | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Timer is enabled
- 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation when device is in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
- 1 = Writes to TMR1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:
- 1 = Asynchronous write to TMR1 register in progress
- 0 = Asynchronous write to TMR1 register complete

In Synchronous Timer mode:
This bit is read as '0'.

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## 15.1 Control Registers

**TABLE 15-1: WATCHDOG TIMER REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | WDTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | — | — | — | — | — | SWDTPS<4:0> | | | | | — | WDTCLR | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

## 17.0 OUTPUT COMPARE

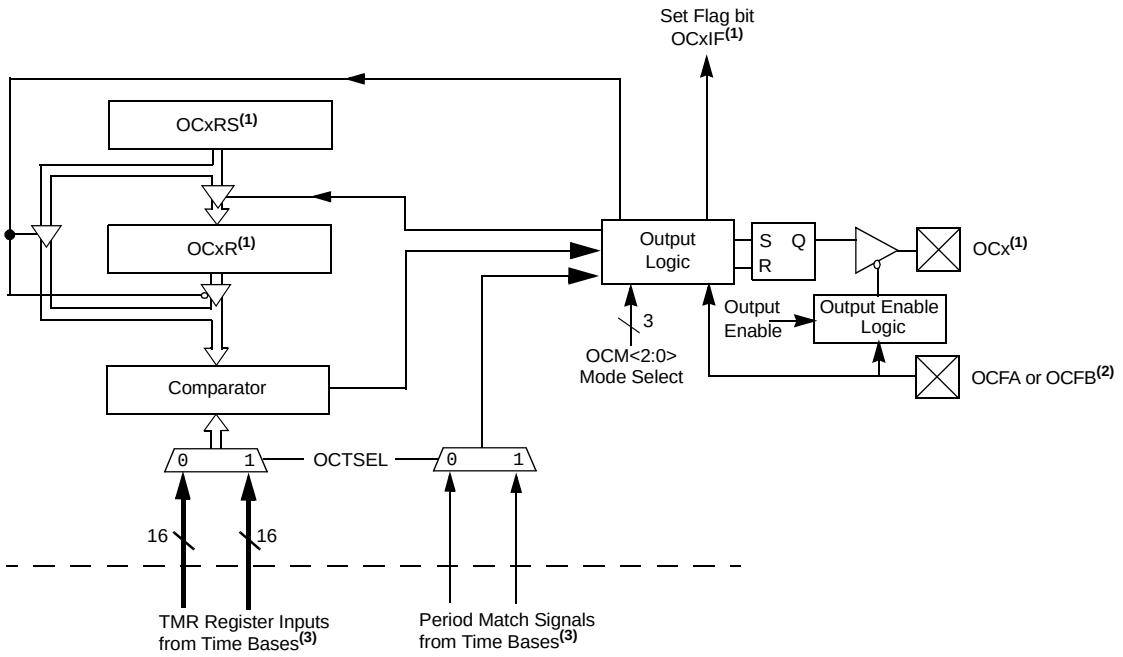
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Output Compare module is used to generate a single pulse or a series of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

**FIGURE 17-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM**




**Note 1:** Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 5.

**2:** The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

**3:** Each output compare channel can use one of two selectable 16-bit time bases or a single 32-bit timer base.

**REGISTER 18-1: SPIxCON: SPI CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | SPIFE | ENHBUF(2) |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE(3) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SSEN | CKP | MSTEN | — | STXISEL<1:0> | | SRXISEL<1:0> | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (only Framed SPI mode)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (only Framed SPI mode)
1 = Frame pulse is active-high
0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The $\overline{SS}$ pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.

bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in Framed Sync mode.
111 = Reserved
110 = Reserved
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character

bit 23-18 **Unimplemented:** Read as '0'

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (only Framed SPI mode)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(2)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit can only be written when the ON bit = 0.

**3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

**REGISTER 19-1: I2CxCON: I$^2$C CONTROL REGISTER (CONTINUED)**

bit 7 **GCEN:** General Call Enable bit (when operating as I$^2$C slave)
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address is disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I$^2$C slave)
Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I$^2$C master, applicable during master receive)
Value that is transmitted when the software initiates an acknowledge sequence.
1 = Send NACK during an acknowledge
0 = Send ACK during an acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (when operating as I$^2$C master, applicable during master receive)
1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence.
0 = Acknowledge sequence not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I$^2$C master)
1 = Enables Receive mode for I$^2$C. Hardware clear at end of eighth bit of master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.
0 = Start condition is not in progress

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 22-6: ALRMDATE: ALARM DATE VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MONTH10<3:0> | | | | MONTH01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | DAY10<1:0> | | | | DAY01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x |
| | — | — | — | — | WDAY01<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1 digit; contains a value from 0 to 6

**REGISTER 25-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMRXOKCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMRXOKCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

**Note 1:** This register is only used for RX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

## 26.0 COMPARATOR

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

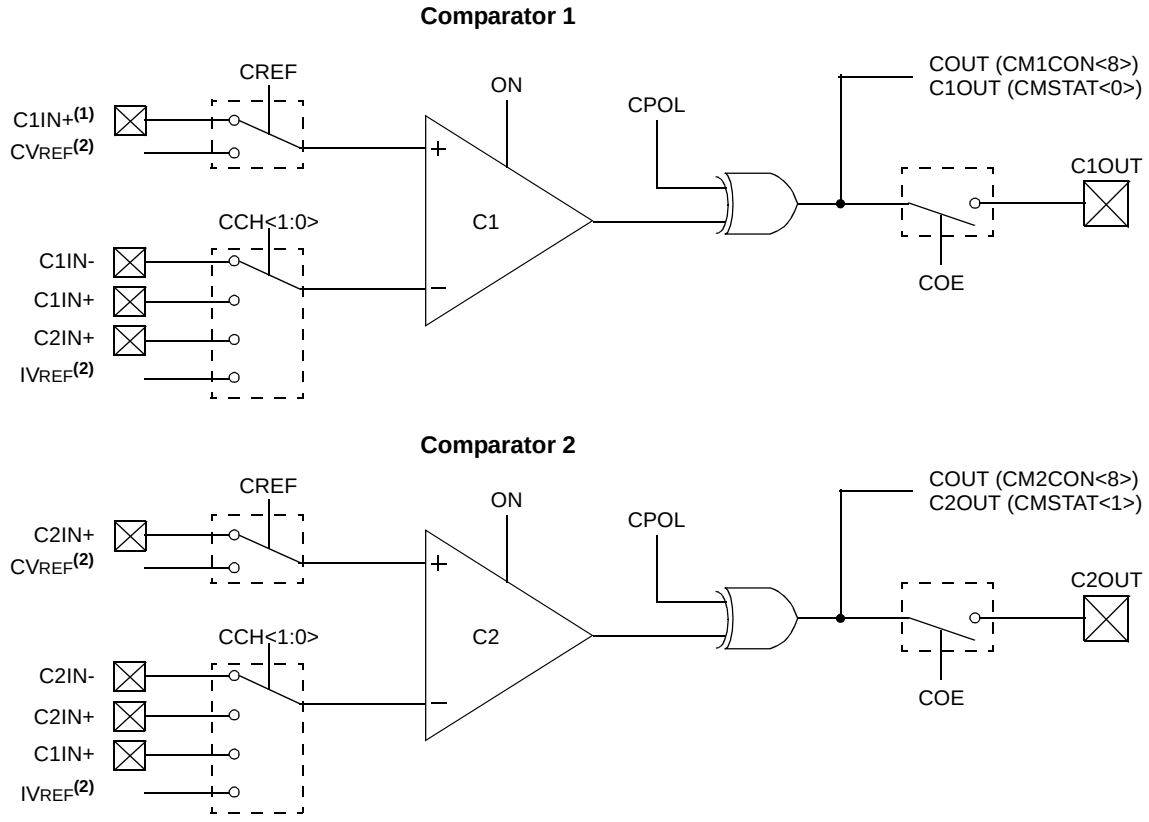
The Comparator module contains two comparators that can be configured in a variety of ways.

Key features of the Comparator module include:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the Comparator module is illustrated in Figure 26-1.

**FIGURE 26-1: COMPARATOR MODULE BLOCK DIAGRAM**




**Note 1:** On devices with a USB module, and when the module is enabled, this pin is controlled by the USB module, and therefore, is not available as a comparator input.

**2:** Internally connected. See **Section 27.0 "Comparator Voltage Reference (CVREF)"**.

**TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD) (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(3)** | **Max.** | **Units** | **Conditions** | | | |
| **Operating Current (IDD)(1,2) for PIC32MX534/564/664/764 Family Devices** | | | | | | | |
| DC20c | 6 | 9 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 4 MHz |
| DC20d | 7 | 10 | | | +105ºC | | |
| DC20e | 2 | — | | Code executing from SRAM | — | | |
| DC21b | 19 | 32 | mA | Code executing from Flash | — | — | 25 MHz **(Note 4)** |
| DC21c | 14 | — | | Code executing from SRAM | | | |
| DC22b | 31 | 50 | mA | Code executing from Flash | — | — | 60 MHz **(Note 4)** |
| DC22c | 29 | — | | Code executing from SRAM | | | |
| DC23c | 39 | 65 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 80 MHz |
| DC23d | 49 | 70 | | | +105ºC | | |
| DC23e | 39 | — | | Code executing from SRAM | — | | |
| DC25b | 100 | 150 | µA | — | +25°C | 3.3V | LPRC (31 kHz) **(Note 4)** |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

**TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT ($I_{PD}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Power-Down Current ($I_{PD}$)(1) for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| DC40 | 10 | 40 | μA | -40°C | 2.3V | Base Power-Down Current **(Note 6)** |
| DC40a | 36 | 100 | | +25°C | | |
| DC40b | 400 | 720 | | +85°C | | |
| DC40h | 900 | 1800 | | +105°C | | |
| DC40c | 41 | 120 | | +25°C | 3.3V | Base Power-Down Current |
| DC40d | 22 | 80 | | -40°C | 3.6V | Base Power-Down Current **(Note 6)** |
| DC40e | 42 | 120 | | +25°C | | |
| DC40g | 315 | 400(5) | | +70°C | | |
| DC40f | 410 | 800 | | +85°C | | |
| DC40i | 1000 | 2000 | | +105°C | | |
| **Module Differential Current for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| DC41 | — | 10 | μA | — | 2.3V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Notes 3,6)** |
| DC41a | 5 | — | | | 3.3V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Note 3)** |
| DC41b | — | 20 | | | 3.6V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Note 3,6)** |
| DC42 | — | 40 | μA | — | 2.3V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Notes 3,6)** |
| DC42a | 23 | — | | | 3.3V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Note 3)** |
| DC42b | — | 50 | | | 3.6V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Note 3,6)** |
| DC43 | — | 1300 | μA | — | 2.5V | ADC: $\Delta I_{ADC}$ **(Notes 3,4,6)** |
| DC43a | 1100 | — | | | 3.3V | ADC: $\Delta I_{ADC}$ **(Notes 3,4)** |
| DC43b | — | 1300 | | | 3.6V | ADC: $\Delta I_{ADC}$ **(Notes 3,4,6)** |

**Note 1:** The test conditions for $I_{PD}$ current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base $I_{PD}$ current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.

**6:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 32-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**

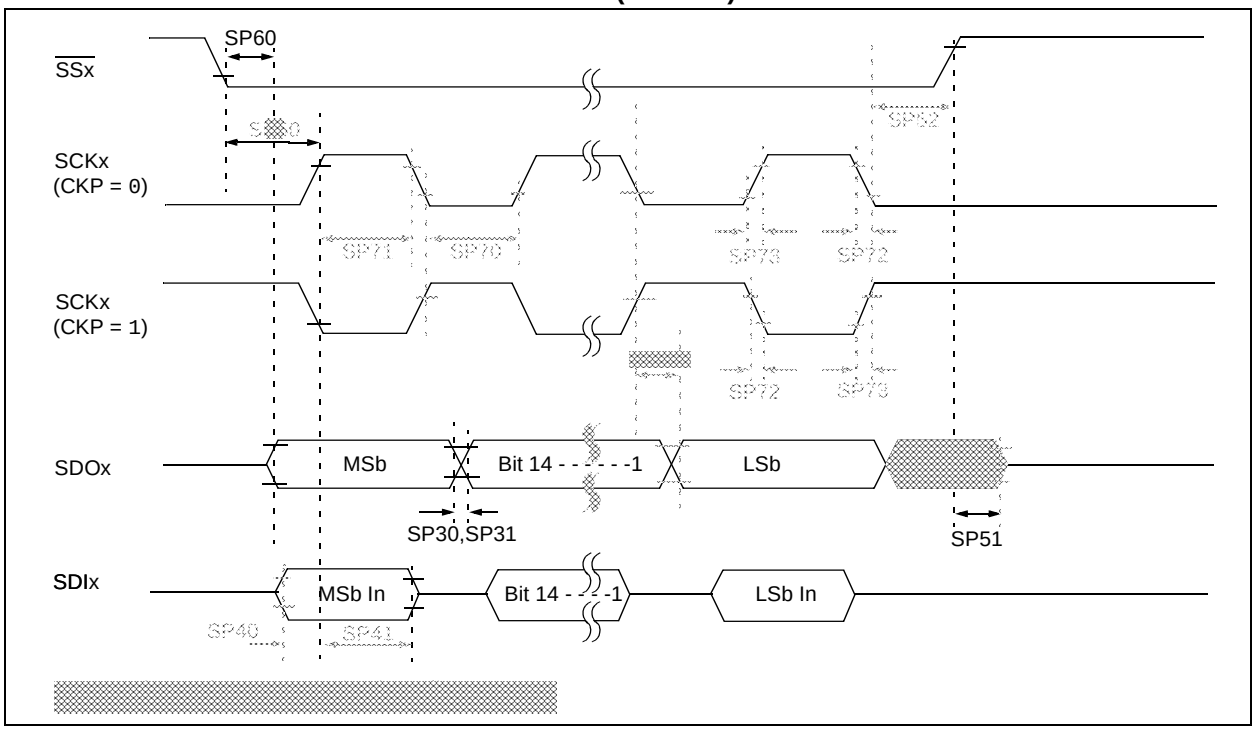



**TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time(3) | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time(3) | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | 5 | 10 | ns | — |
| SP73 | TscR | SCKx Input Rise Time | — | 5 | 10 | ns | — |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 20 | ns | VDD > 2.7V |
| | | | — | — | 30 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input | 175 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns.

**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 32-38: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | Analog-to-Digital Clock Period(2) | 65 | — | — | ns | See Table 32-37 |
| **Conversion Rate** | | | | | | | |
| AD55 | TCONV | Conversion Time | — | 12 TAD | — | — | — |
| AD56 | FCNV | Throughput Rate (Sampling Speed) | — | — | 1000 | ksps | AVDD = 3.0V to 3.6V |
| | | | — | — | 400 | ksps | AVDD = 2.5V to 3.6V |
| AD57 | TSAMP | Sample Time | 1 TAD | — | — | — | TSAMP must be ≥ 132 ns |
| **Timing Parameters** | | | | | | | |
| AD60 | TPCS | Conversion Start from Sample Trigger(3) | — | 1.0 TAD | — | — | Auto-Convert Trigger (SSRC<2:0> = 111) not selected |
| AD61 | TPSS | Sample Start from Setting Sample (SAMP) bit | 0.5 TAD | — | 1.5 TAD | — | — |
| AD62 | TCSS | Conversion Completion to Sample Start (ASAM = 1)(3) | — | 0.5 TAD | — | — | — |
| AD63 | TDPU | Time to Stabilize Analog Stage from Analog-to-Digital Off to Analog-to-Digital On(3) | — | — | 2 | μs | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

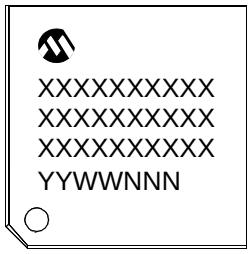
**3:** Characterized by design but not tested.

**4:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

## 34.0 PACKAGING INFORMATION

### 34.1 Package Marking Information

64-Lead TQFP (10x10x1 mm)

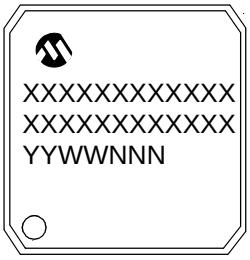



Example


100-Lead TQFP (14x14x1 mm)


Example


100-Lead TQFP (12x12x1 mm)




Example


| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

**TABLE B-4: SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **4.0 "Memory Organization"** (Continued) | • Table 4-13:<br>- Changed register U4RG to U1BRG<br>- Changed register U5RG to U3BRG<br>- Changed register U6RG to U2BRG<br>• Table 4-14:<br>- Updated the All Resets values for the following registers: SPI3STAT, SPI2STAT and SPI4STAT<br>• Table 4-15: Updated the All Resets values for the SPI1STAT register<br>• Table 4-17: Added note 2<br>• Table 4-19: Added note 2<br>• Table 4-20: Updated the All Resets values for the CM1CON and CM2CON registers<br>• Table 4-21:<br>- Updated the All Resets values as 0000 for the CVRCON register<br>- Updated note 2<br>• Table 4-38: Updated the All Resets values for the PMSTAT register<br>• Table 4-40: Updated the All Resets values for the CHECON and CHETAG registers<br>• Table 4-42: Updated the bit value of bit 29/13 as '—' for the DEVCFG3 register<br>• Table 4-44:<br>- Updated the note references in the entire table<br>- Changed existing note 1 to note 4<br>- Added notes 1, 2 and 3<br>- Changed bits 23/7 in U1PWRC to UACTPND<br>- Changed register U1DDR to U1ADDR<br>- Changed register U4DTP1 to U1BDTP1<br>- Changed register U4DTP2 to U1BDTP2<br>- Changed register U4DTP3 to U1BDTP3<br>• Table 4-45:<br>- Updated the All Resets values for the C1CON and C1VEC registers<br>- Changed bits 30/14 in C1CON to FRZ<br>- Changed bits 27/11 in C1CON to CANBUSY<br>- Changed bits 22/6-16/0 in C1VEC to ICODE<6:0><br>- Changed bits 22/6-16/0 in C1TREC to RERRCNT<7:0><br>- Changed bits 31/15-24/8 in C1TREC to TERRCNT<7:0><br>• Table 4-46:<br>- Updated the All Resets values for the C2CON and C2VEC registers<br>- Changed bits 30/14 in C1CON to FRZ<br>- Changed bits 27/11 in C1CON to CANBUSY<br>- Changed bits 22/6-16/0 in C1VEC register to ICODE<6:0><br>- Changed bits 22/6-16/0 in C1TREC register to RERRCNT<7:0><br>- Changed bits 31/15-24/8 in C1TREC to TERRCNT<7:0> |