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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx664f128l-i-bg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIN NAMES FOR 100-PIN USB, ETHERNET, AND CAN DEVICES TABLE 9:

100-PIN TQFP (TOP VIEW)

PIC32MX764F128L PIC32MX775F256L PIC32MX775F512L PIC32MX795F512L

100

Pin #	Full Pin Name
1	AERXERR/RG15
2	VDD
3	PMD5/RE5
4	PMD6/RE6
5	PMD7/RE7
6	T2CK/RC1
7	T3CK/AC2TX ⁽¹⁾ /RC2
8	T4CK/AC2RX ⁽¹⁾ /RC3
9	T5CK/SDI1/RC4
10	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6
11	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7
12	ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8
13	MCLR
14	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9
15	Vss
16	VDD
17	TMS/RA0
18	AERXD0/INT1/RE8
19	AERXD1/INT2/RE9
20	AN5/C1IN+/VBUSON/CN7/RB5
21	AN4/C1IN-/CN6/RB4
22	AN3/C2IN+/CN5/RB3
23	AN2/C2IN-/CN4/RB2
24	PGEC1/AN1/CN3/RB1
25	PGED1/AN0/CN2/RB0
26	PGEC2/AN6/OCFA/RB6
27	PGED2/AN7/RB7
28	Vref-/CVref-/AERXD2/PMA7/RA9
29	VREF+/CVREF+/AERXD3/PMA6/RA10
30	AVdd
31	AVss
32	AN8/C1OUT/RB8
33	AN9/C2OUT/RB9
34	AN10/CVREFOUT/PMA13/RB10
35	AN11/ERXERR/AETXERR/PMA12/RB11
Note	1. This pin is not available on PIC32MX764E128L devices

Pin #	Full Pin Name
36	Vss
37	VDD
38	TCK/RA1
39	AC1TX/SCK4/U5TX/U2RTS/RF13
40	AC1RX/SS4/U5RX/U2CTS/RF12
41	AN12/ERXD0/AECRS/PMA11/RB12
42	AN13/ERXD1/AECOL/PMA10/RB13
43	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14
44	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
45	Vss
46	Vdd
47	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
48	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
51	USBID/RF3
52	SDA3/SDI3/U1RX/RF2
53	SCL3/SDO3/U1TX/RF8
54	VBUS
55	VUSB3V3
56	D-/RG3
57	D+/RG2
58	SCL2/RA2
59	SDA2/RA3
60	TDI/RA4
61	TDO/RA5
62	Vdd
63	OSC1/CLKI/RC12
64	OSC2/CLKO/RC15
65	Vss
66	AETXCLK/SCL1/INT3/RA14
67	AETXEN/SDA1/INT4/RA15
68	RTCC/EMDIO/AEMDIO/IC1/RD8
69	SS1/IC2/RD9
70	SCK1/IC3/PMCS2/PMA15/RD10

1

This pin is not available on PIC32MX764F128L devices. 1:

2: Shaded pins are 5V tolerant. NOTES:

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32). The Oscillator module has the following features:

- A total of four external and internal oscillator options as clock sources
- On-chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

Figure 8-1shows the Oscillator module block diagram.



TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)

ess										Bi	its								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000		31:16	_		_	_	_	_		_		_	—	_	_	_	_		0000
3290	DCH2DAI	15:0	_	_		_	_	_	_	_				CHPDA	AT<7:0>				0000
3240		31:16	—	_	—	_	_	_	_	—	_	—	_	_	_	_	_	_	0000
02A0	DOI 100011	15:0	CHBUSY	_	—	_	_	_	_	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPR	l<1:0>	0000
32B0	DCH3ECON	31:16	—			—	—	—	—	—				CHAIR	Q<7:0>				OOFF
		15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	-			FF00
32C0	DCH3INT	31:16			_	_	_	_	_	_	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHIAIE	CHERIE	0000
		31.16	_	—	_	—	_	—	_	—	CHODIE	Спапіг	CHUDIF	CHDHIF		CHCCIF	CHIAIF	CHERIF	0000
32D0	DCH3SSA	CHSSA<31:0>														0000			
	DOLIODOA	31:16 0000																	
32E0	DCH3DSA	15:0								CHDSA	<31:0>								0000
2250		31:16	_	_		—	—	—	_	_	_		—	_	—	—	_	_	0000
32FU	DCH353IZ	15:0 CHSSIZ<15:0> 0000																	
3300	DCH3DSIZ	31:16	—	_	—	—	—	—	—	—	_	—	—	—	—	—	—	_	0000
	501105012	15:0								CHDSIZ	Z<15:0>								0000
3310	DCH3SPTR	31:16	—	_	—				_	-	—	—		—			_	_	0000
		15:0	15:0 CHSPTR<15:0> 000														0000		
3320	DCH3DPTR	31.10	—	—	—	—	_	—	—		— P~15:0>	_	_	—	_	—	—	_	0000
		31.16	_	_	_	_	_	_	_		_	_	_	_	_	_	_	_	0000
3330	DCH3CSIZ	15:0								CHCSIZ	Z<15:0>								0000
		31:16	_	_	—	_	_	_	—	_	_	_	_	_	_	_	_	_	0000
3340	DCH3CPTR	15:0								CHCPT	R<15:0>								0000
3350		31:16	—	—	_	-	-			_		_	-	_	-	-			0000
3350	DCH3DAI	15:0	—	_	—	-	—	-	-	—				CHPDA	AT<7:0>				0000
3360	DCH4CON	31:16	—	_	—	—	—	—	_	—	—	—	—	—	—	—	_	—	0000
	20110011	15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	_	CHEDET	CHPR	l<1:0>	0000
3370	DCH4ECON	31:16	—	_	—	-			_	—	050005	ALDODT	DATEN	CHAIR	Q<7:0>				00FF
		15:0				CHSIR	Q<7:0>				CFORCE	CABORT		SIRQEN					FF00
3380	DCH4INT	31:10			_					_	CHSDIE	CHSHIE							0000
		31.16			_					_	CHODIF	CHOHIF		CHDHIF		CHOOF		UNERIF	0000
3390	DCH4SSA	15:0								CHSSA	<31:0>								0000
		31:16																	0000
33A0	DCH4DSA	15:0								CHDSA	<31:0>								0000
Logon	d																		

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more Note 1: information.

2: DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		—	—	_	_		_	_
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8		—	—	_	_		_	_
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-24 Unimplemented: Read as '0'

bit 23	CHSDIE: Channel Source Done Interrupt Enable bit
	1 = Interrupt is enabled0 = Interrupt is disabled
bit 22	CHSHIE: Channel Source Half Empty Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 21	CHDDIE: Channel Destination Done Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 20	CHDHIE: Channel Destination Half Full Interrupt Enable bit
	1 = Interrupt is enabled
hit 10	CHRCIE: Channel Black Transfer Complete Interrupt Enchle hit
DIL 19	
	0 = Interrupt is disabled
bit 18	CHCCIE: Channel Cell Transfer Complete Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 17	CHTAIE: Channel Transfer Abort Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 16	CHERIE: Channel Address Error Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 15-8	Unimplemented: Read as '0'
bit 7	CHSDIF: Channel Source Done Interrupt Flag bit
	 1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ) 0 = No interrupt is pending
bit 6	CHSHIF: Channel Source Half Empty Interrupt Flag bit
	1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
	0 = No interrupt is pending

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0						
01.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
31:24	CHSSA<31:24>													
00:40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
23:16	CHSSA<23:16>													
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
15:8	CHSSA<15:8>													
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
7:0				CHSSA	<7:0>									

REGISTER 10-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER

Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-0 CHSSA<31:0> Channel Source Start Address bits Channel source start address. Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0						
04.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
31:24	CHDSA<31:24>													
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
23:16				CHDSA<	:23:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
15:8				CHDSA	<15:8>									
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
7:0				CHDSA	<7:0>									

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 CHDSA<31:0>: Channel Destination Start Address bits Channel destination start address.

Note: This must be the physical address of the destination.



NOTES:

TABLE 12-5: PORTD REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

ess	Register Name ⁽¹⁾	Bit Range		Bits															9
Virtual Addr (BF88_#)			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
0000	TDICD	31:16	_	_	_	_	-	—	_	_	_	_	_	_	_	_	_	_	0000
6000	IRISD	15:0		_		_	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	OFFF
6000		31:16	_	—	_	—		—	-		_	_	_	_	_	_	_	_	0000
0000	FORTD	15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0		31:16		—	_	—		_			_	_	_	_	_	-		_	0000
00E0	LAID	15:0	-	_	_	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	0000	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
	ODCD	15:0	_	_	_	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 12-6: PORTD REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F512L, AND PIC32MX795F512L DEVICES

ess		Ó								В	ts								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6000	TRICD	31:16	-	_	_	-	—	—	—	—	-	—	_	_	—	—	_	_	0000
6000	TRISD	15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
6000		31:16	_	_	_	_	_	—	_	_		_	_	_	—	—	_	_	0000
00D0	FORTD	15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
6050		31:16	—	—	—	—		_	—	_	_	—	—	—	—	—	—	—	0000
OUEU	LAID	15:0	LAT15	LAT14	LAT13	LAT12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
6050	0000	31:16	_	_	_	_		_	_	_	_	_	_	_	_	_	_	_	0000
00F0	UDUD	15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Ļ

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24		—	—	—	_		—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

REGISTER 23-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

1 = Select ANx for input scan

0 =Skip ANx for input scan

Note 1: CSSL = ANx, where 'x' = 0-15.

bit 15-0 CSSL<15:0>: ADC Input Pin Scan Selection bits⁽¹⁾

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24	FLTEN3 MSEL3<1:0>			FSEL3<4:0>					
22.46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	FLTEN2 MSEL2<1:0>			FSEL2<4:0>					
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
10.0	FLTEN1	MSEL	1<1:0>		F	SEL1<4:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0	FLTEN0	MSEL0<1:0>		FSEL0<4:0>					

REGISTER 24-10: CIFLTCON0: CAN FILTER CONTROL REGISTER 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN3: Filter 3 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL3<1:0>: Filter 3 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 28-24	FSEL3<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN2: Filter 2 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 22-21	MSEL2<1:0>: Filter 2 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 20-16	FSEL2<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 24-10: CIFLTCONO: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 15	FLTEN1: Filter 1 Enable bit 1 = Filter is enabled
	0 = Filter is disabled
bit 14-13	MSEL1<1:0>: Filter 1 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	00 = Acceptance Mask 0 selected
bit 12-8	FSEL1<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 7	FLTEN0: Filter 0 Enable bit
	1 = Filter is enabled 0 = Filter is disabled
bit 6-5	MSEL0<1:0>: Filter 0 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
hit 1 0	$\mathbf{SEEI} = \mathbf{Acceptance mask 0 selected}$
DIL 4-0	11111 - Message matching filter is stored in EIEO buffer 31
	11110 - Message matching filter is stored in FIFO buffer 30
	•
	•
	• 00001 – Message matching filter is stored in EIEO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24	FLTEN11 MSEL11<1:0>			FSEL11<4:0>					
22:46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	FLTEN10 MSEL1		0<1:0>	FSEL10<4:0>					
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15.6	FLTEN9 MSEL9<		9<1:0>		FSEL9<4:0>				
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	FLTEN8 MSEL8<1:0>		8<1:0>	FSEL8<4:0>					

REGISTER 24-12: CIFLTCON2: CAN FILTER CONTROL REGISTER 2

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN11: Filter 11 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL11<1:0>: Filter 11 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 28-24	FSEL11<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN10: Filter 10 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 22-21	MSEL10<1:0>: Filter 10 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
bit 20-16	FSEL10<4:0>: FIFO Selection bits
	11111 = Message matching filter is stored in FIFO buffer 31
	11110 = Message matching filter is stored in FIFO buffer 30
	•
	•
	00001 = Message matching filter is stored in FIFO buffer 1
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

28.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 10. "Power-Saving Features" (DS60001130) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

This section describes power-saving features for the PIC32MX5XX/6XX/7XX family of devices. These devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

28.1 Power-Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the Peripheral Bus Clock (PBCLK) and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- Sosc Run mode: the CPU is clocked from the Sosc clock source.

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

28.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- **Posc Idle mode:** the system clock is derived from the Posc. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.

- **Sosc Idle mode:** the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.
- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

28.3 Power-Saving Operation

Peripherals and the CPU can be halted or disabled to further reduce power consumption.

28.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See Section 28.3.3 "Peripheral Bus Scaling Method" for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit, if enabled, remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

REGISTER 29-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

- bit 3 ICESEL: In-Circuit Emulator/Debugger Communication Channel Select bit
 - 1 = PGEC2/PGED2 pair is used
 - 0 = PGEC1/PGED1 pair is used
- bit 2 Reserved: Write '1'
- bit 1-0 DEBUG<1:0>: Background Debugger Enable bits (forced to '11' if code-protect is enabled)
 - 11 = Debugger is disabled
 - 10 = Debugger is enabled
 - 01 = Reserved (same as '11' setting)
 - 00 = Reserved (same as '11' setting)

REGISTER 29-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
31:24	—	—	—	—	—	-	—	—
00.40	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
23:16	—	—	—	—	—	FF	PLLODIV<2:0)>
45.0	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
15:8	UPLLEN	—	—	—	—	UPLLIDIV<2:0>		
7:0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
		F	PLLMUL<2:0	>	_	FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-19 Reserved: Write '1'

bit 18-16 **FPLLODIV<2:0>:** PLL Output Divider bits 111 = PLL output divided by 256

- 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2
- 000 = PLL output divided by 1
- bit 15 UPLLEN: USB PLL Enable bit 1 = Disable and bypass USB PLL 0 = Enable USB PLL
- bit 14-11 Reserved: Write '1'
- bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits
 - 111 = 12x divider
 - 110 = 10x divider
 - 101 = 6x divider
 - 100 = 5x divider
 - 011 = 4x divider
 - 010 = 3x divider
 - 001 = 2x divider 000 = 1x divider
- bit 7 **Reserved:** Write '1'
- bit 6-4 FPLLMUL<2:0>: PLL Multiplier bits
 - 111 = 24x multiplier
 - 110 = 21x multiplier
 - 101 = 20x multiplier
 - 100 = 19x multiplier
 - 011 = 18x multiplier
 - 010 = 17x multiplier 001 = 16x multiplier
 - 001 = 10x multiplier
- bit 3 **Reserved:** Write '1'

TABLE 32-13: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D300	VIOFF	Input Offset Voltage	_	±7.5	±25	mV	Avdd = Vdd, Avss = Vss
D301	VICM	Input Common Mode Voltage	0	—	Vdd	V	Avdd = Vdd, Avss = Vss (Note 2)
D302	CMRR	Common Mode Rejection Ratio	55	—	_	dB	Max VICM = (VDD - 1)V (Note 2)
D303	TRESP	Response Time	-	150	400	ns	AVDD = VDD, AVss = Vss (Notes 1, 2)
D304	ON2ov	Comparator Enabled to Output Valid	—	—	10	μs	Comparator module is configured before setting the comparator ON bit (Note 2)
D305	IVREF	Internal Voltage Reference	0.57	0.6	0.63	V	For devices without BGSEL<1:0>
			1.14	1.2	1.26	V	BGSEL<1:0> = 00
			0.57	0.6	0.63	V	BGSEL<1:0> = 01

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from Vss to VDD.

2: These parameters are characterized but not tested.

3: The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

34.2 Package Details

The following sections give the technical details of the packages.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

Revision E (July 2010)

Minor corrections were incorporated throughout the document.

Revision F (December 2010)

The revision includes the following global update:

VCAP/VDDCORE has been changed to: VCAP/VCORE

Other major changes are referenced by their respective chapter/section in Table B-4:

TABLE B-4: SECTION UPDATES

Section Name	Update Description
High-Performance, USB, CAN and	Removed the following Analog Feature: FV tolerant input pins
Ethernet 32-bit Flash Microcontrollers	(digital pins only)
	Updated the term LIN 1.2 support as LIN support for the peripheral feature: Six UART modules with: RS-232, RS-485, and LIN support
1.0 "Device Overview"	Updated the value of 64-pin QFN/TQFP pin number for the following pin names: PMA0, PMA1 and ECRSDV
4.0 "Memory Organization"	The following register map tables were updated:
	• Table 4-2:
	 Changed bits 24/8 to I2C5BIF in IFS1
	 Changed bits 24/8-24/10 to SRIPL<2:0> in INTSTAT
	 Changed bits 25/9/-24/8 to U5IS<1:0> in IPC12
	- Added note 2
	Table 4-3 through Table 4-7:
	 Changed bits 24/8-24/10 to SRIPL<2:0> in INTSTAT
	 Changed bits 25/9-24/8 to U5IS<1:0> in IPC12
	• Table 4-3:
	 Changed bits 24/8 to I2C5BIF in IFS1
	- Added note 2
	• Table 4-4:
	 Changed bits 24/8 to I2C5BIF in IFS1
	 Changed bits 24/8 to I2C5BIE in IEC1
	 Added note 2 references
	• Table 4-5:
	 Changed bits 24/8 to I2C5BIF in IFS1
	 Changed bits 24/8 to I2C5BIE in IEC1
	- Added note 2 references
	• Table 4-6:
	 Changed bit 24/8 to I2C5BIF in IFS1
	 Updated the bit value of bit 24/8 as I2C5BIE for the IEC1 register.
	- Added note 2
	• Table 4-7:
	 Changed bit 25/9 to I2C5SIF in IFS1
	- Changed bit 24/8 as I2C5BIF in IFS1
	- Changed bit 25/9 as I2C5SIE in IEC1
	- Changed bit 24/8 as I2C5BIE in IEC1
	- Added note 2 references
	Added note 2 to Table 4-8
	 Updated the All Resets values for the following registers in Table 4-11: I2C3CON, I2C4CON, I2C5CON and I2C1CON.
	 Updated the All Resets values for the I2C2CON register in Table 4-12