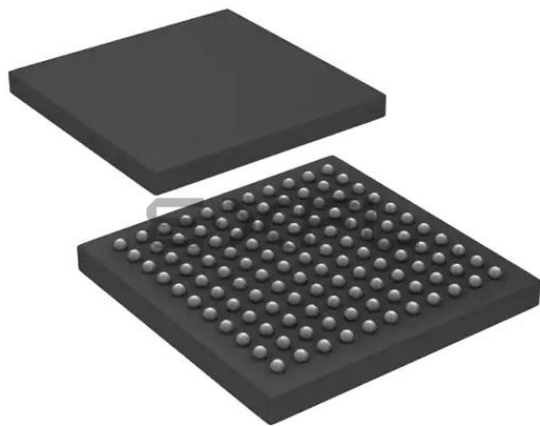




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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx664f128lt-v-bg

PIC32MX5XX/6XX/7XX

TABLE 10: PIN NAMES FOR USB AND CAN DEVICES

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX575F256L PIC32MX575F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1	
Pin #	Full Pin Name	Pin #	Full Pin Name
A1	PMD4/RE4	E2	T4CK/RC3
A2	PMD3/RE3	E3	SCK2/U6TXU6TX/U3RTS/PMA5/CN8/RG6
A3	TRD0/RG13	E4	T3CK/RC2
A4	PMD0/RE0	E5	VDD
A5	PMD8/RG0	E6	PMD9/RG1
A6	C1TX/PMD10/RF1	E7	VSS
A7	VDD	E8	SDA1/INT4/RA15
A8	VSS	E9	RTCC/IC1/RD8
A9	IC5/PMD12/RD12	E10	SS1/IC2/RD9
A10	OC3/RD2	E11	SCL1/INT3/RA14
A11	OC2/RD1	F1	MCLR
B1	No Connect (NC)	F2	SCL4/SDO2/U3TX/PMA3/CN10/RG8
B2	RG15	F3	SS2/U6RX/U3CTS/PMA2/CN11/RG9
B3	PMD2/RE2	F4	SDA4/SDI2/U3RX/PMA4/CN9/RG7
B4	PMD1/RE1	F5	VSS
B5	TRD3/RA7	F6	No Connect (NC)
B6	C1RX/PMD11/RF0	F7	No Connect (NC)
B7	VCAP	F8	VDD
B8	PMRD/CN14/RD5	F9	OSC1/CLKI/RC12
B9	OC4/RD3	F10	VSS
B10	VSS	F11	OSC2/CLKO/RC15
B11	SOSCO/T1CK/CN0/RC14	G1	INT1/RE8
C1	PMD6/RE6	G2	INT2/RE9
C2	VDD	G3	TMS/RA0
C3	TRD1/RG12	G4	No Connect (NC)
C4	TRD2/RG14	G5	VDD
C5	TRCLK/RA6	G6	VSS
C6	No Connect (NC)	G7	VSS
C7	PMD15/CN16/RD7	G8	No Connect (NC)
C8	OC5/PMWR/CN13/RD4	G9	TDO/RA5
C9	VDD	G10	SDA2/RA3
C10	SOSCI/CN1/RC13	G11	TDI/RA4
C11	IC4/PMCS1/PMA14/RD11	H1	AN5/C1IN+/VBUSON/CN7/RB5
D1	T2CK/RC1	H2	AN4/C1IN-/CN6/RB4
D2	PMD7/RE7	H3	VSS
D3	PMD5/RE5	H4	VDD
D4	VSS	H5	No Connect (NC)
D5	VSS	H6	VDD
D6	No Connect (NC)	H7	No Connect (NC)
D7	PMD14/CN15/RD6	H8	VBUS
D8	PMD13/CN19/RD13	H9	VUSB3V3
D9	SDO1/OC1/INT0/RD0	H10	D+/RG2
D10	No Connect (NC)	H11	SCL2/RA2
D11	SCK1/IC3/PMCS2/PMA15/RD10	J1	AN3/C2IN+/CN5/RB3
E1	T5CK/SDI1/RC4	J2	AN2/C2IN-/CN4/RB2

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1	
Pin #	Full Pin Name	Pin #	Full Pin Name
A1	PMD4/RE4	E2	T4CK/RC3
A2	PMD3/RE3	E3	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6
A3	TRD0/RG13	E4	T3CK/RC2
A4	PMD0/RE0	E5	VDD
A5	PMD8/RG0	E6	ETXERR/PMD9/RG1
A6	ETXD0/PMD10/RF1	E7	VSS
A7	VDD	E8	AETXEN/SDA1/INT4/RA15
A8	VSS	E9	RTCC/EMDIO/AEMDIO/IC1/RD8
A9	ETXD2/IC5/PMD12/RD12	E10	SS1/IC2/RD9
A10	OC3/RD2	E11	AETXCLK/SCL1/INT3/RA14
A11	OC2/RD1	F1	MCLR
B1	No Connect (NC)	F2	ERXDVI/AERXDVI/ECRSDVI/AECRSDVI/SCL4/SDO2/U3TX/PMA3/CN10/RG8
B2	AERXERR/RG15	F3	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9
B3	PMD2/RE2	F4	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7
B4	PMD1/RE1	F5	VSS
B5	TRD3/RA7	F6	No Connect (NC)
B6	ETXD1/PMD11/RF0	F7	No Connect (NC)
B7	VCAP	F8	VDD
B8	PMRD/CN14/RD5	F9	OSC1/CLKI/RC12
B9	OC4/RD3	F10	VSS
B10	VSS	F11	OSC2/CLKO/RC15
B11	SOSCO/T1CK/CN0/RC14	G1	AERXD0/INT1/RE8
C1	PMD6/RE6	G2	AERXD1/INT2/RE9
C2	VDD	G3	TMS/RA0
C3	TRD1/RG12	G4	No Connect (NC)
C4	TRD2/RG14	G5	VDD
C5	TRCLK/RA6	G6	VSS
C6	No Connect (NC)	G7	VSS
C7	ETXCLK/PMD15/CN16/RD7	G8	No Connect (NC)
C8	OC5/PMWR/CN13/RD4	G9	TDO/RA5
C9	VDD	G10	SDA2/RA3
C10	SOSCI/CN1/RC13	G11	TDI/RA4
C11	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	H1	AN5/C1IN+/VBUSON/CN7/RB5
D1	T2CK/RC1	H2	AN4/C1IN-/CN6/RB4
D2	PMD7/RE7	H3	VSS
D3	PMD5/RE5	H4	VDD
D4	VSS	H5	No Connect (NC)
D5	VSS	H6	VDD
D6	No Connect (NC)	H7	No Connect (NC)
D7	ETXEN/PMD14/CN15/RD6	H8	VBUS
D8	ETXD3/PMD13/CN19/RD13	H9	VUSB3V3
D9	SDO1/OC1/INT0/RD0	H10	D+/RG2
D10	No Connect (NC)	H11	SCL2/RA2
D11	SCK1/IC3/PMCS2/PMA15/RD10	J1	AN3/C2IN+/CN5/RB3
E1	T5CK/SDI1/RC4	J2	AN2/C2IN-/CN4/RB2

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST ⁽¹⁾

Legend:	HC = Cleared by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit⁽¹⁾
 1 = Enable software Reset event
 0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

TABLE 7-7: INTERRUPT REGISTER MAP FOR PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	SPI1TXIF	SPI1RXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	CAN2IF ⁽²⁾	CAN1IF	USBIF	FCEIF	DMA7IF ⁽²⁾	DMA6IF ⁽²⁾	DMA5IF ⁽²⁾	DMA4IF ⁽²⁾	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIF	U5RXIF	U5EIF	U6TXIF	U6RXIF	U6EIF	U4TXIF	U4RXIF	U4EIF	PMPEIF	IC5EIF	IC4EIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	SPI1TXIE	SPI1RXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	CAN2IE ⁽²⁾	CAN1IE	USBIE	FCEIE	DMA7IE ⁽²⁾	DMA6IE ⁽²⁾	DMA5IE ⁽²⁾	DMA4IE ⁽²⁾	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>			—	—	—	CS1IP<2:0>			CS1IS<1:0>	0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>			—	—	—	CTIP<2:0>			CTIS<1:0>	0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>			—	—	—	OC1IP<2:0>			OC1IS<1:0>	0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>			—	—	—	T1IP<2:0>			T1IS<1:0>	0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>			—	—	—	OC2IP<2:0>			OC2IS<1:0>	0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>			—	—	—	T2IP<2:0>			T2IS<1:0>	0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>			—	—	—	OC3IP<2:0>			OC3IS<1:0>	0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>			—	—	—	T3IP<2:0>			T3IS<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2: This bit is unimplemented on PIC32MX764F128L device.
- 3: This register does not have associated CLR, SET, and INV registers.

TABLE 7-7: INTERRUPT REGISTER MAP FOR PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>			—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000	
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>			—	—	—	T4IP<2:0>			T4IS<1:0>		0000	
10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>			—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000	
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>			—	—	—	T5IP<2:0>			T5IS<1:0>		0000	
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>			—	—	—	CNIP<2:0>			CNIS<1:0>		0000	
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>			—	—	—	U1IP<2:0>			U1IS<1:0>		0000	
															SPI3IP<2:0>			SPI3IS<1:0>			
															I2C3IP<2:0>			I2C3IS<1:0>			
1100	IPC7	31:16	—	—	—	U3IP<2:0>			U3IS<1:0>			—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000	
						SPI2IP<2:0>			SPI2IS<1:0>												
						I2C4IP<2:0>			I2C4IS<1:0>												
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>			—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000	
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>			—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000	
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>			—	—	—	U2IP<2:0>			U2IS<1:0>		0000	
															SPI4IP<2:0>			SPI4IS<1:0>			
															I2C5IP<2:0>			I2C5IS<1:0>			
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>			—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000	
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>			—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000	
1130	IPC10	31:16	—	—	—	DMA7IP<2:0> ⁽²⁾			DMA7IS<1:0> ⁽²⁾			—	—	—	DMA6IP<2:0> ⁽²⁾			DMA6IS<1:0> ⁽²⁾		0000	
		15:0	—	—	—	DMA5IP<2:0> ⁽²⁾			DMA5IS<1:0> ⁽²⁾			—	—	—	DMA4IP<2:0> ⁽²⁾			DMA4IS<1:0> ⁽²⁾		0000	
1140	IPC11	31:16	—	—	—	CAN2IP<2:0> ⁽²⁾			CAN2IS<1:0> ⁽²⁾			—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		0000	
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>			—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000	
1150	IPC12	31:16	—	—	—	U5IP<2:0>			U5IS<1:0>			—	—	—	U6IP<2:0>			U6IS<1:0>		0000	
		15:0	—	—	—	U4IP<2:0>			U4IS<1:0>			—	—	—	ETHIP<2:0>			ETHIS<1:0>		0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This bit is unimplemented on PIC32MX764F128L device.

3: This register does not have associated CLR, SET, and INV registers.

PIC32MX5XX/6XX/7XX

REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RIPL<2:0> ⁽¹⁾		
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	VEC<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **RIPL<2:0>:** Requested Priority Level bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits⁽¹⁾

11111-00000 = The interrupt vector that is presented to the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single-vector mode.

REGISTER 7-3: TPTMR: TEMPORAL PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TPTMR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **TPTMR<31:0>:** Temporal Proximity Timer Reload bits

Used by the Temporal Proximity Timer as a reload value when the Temporal Proximity timer is triggered by an interrupt event.

TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0	CHSSA<31:0>																0000
30A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0	CHDSA<31:0>																0000
30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0	CHSSA<31:0>																0000
3160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0	CHDSA<31:0>																0000
3170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- Note 2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

PIC32MX5XX/6XX/7XX

REGISTER 11-3: U1OTGSTAT: USB OTG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit

1 = No cable is attached or a "type B" cable has been inserted into the USB receptacle

0 = A "type A" OTG cable has been inserted into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit

1 = USB line state (SE0 (U1CON<6> and JSTATE (U1CON<7>) has been stable for the previous 1 ms

0 = USB line state (SE0 (U1CON<6> and JSTATE (U1CON<7>) has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit

1 = VBUS voltage is above Session Valid on the A or B device

0 = VBUS voltage is below Session Valid on the A or B device

bit 2 **SESEND:** B-Device Session End Indicator bit

1 = VBUS voltage is below Session Valid on the B device

0 = VBUS voltage is above Session Valid on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit

1 = VBUS voltage is above Session Valid on the A device

0 = VBUS voltage is below Session Valid on the A device

PIC32MX5XX/6XX/7XX

REGISTER 11-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/WC-0, HS BTSEF	R/WC-0, HS BMXEF	R/WC-0, HS DMAEF ⁽¹⁾	R/WC-0, HS BTOEF ⁽²⁾	R/WC-0, HS DFN8EF	R/WC-0, HS CRC16EF	R/WC-0, HS CRC5EF ⁽⁴⁾ EOFEF ^(3,5)	R/WC-0, HS PIDEF

Legend:

R = Readable bit

-n = Value at POR

WC = Write '1' to clear

W = Writable bit

'1' = Bit is set

HS = Hardware Settable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit

1 = Packet is rejected due to bit stuff error

0 = Packet is accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit

1 = Invalid base address of the BDT, or the address of an individual buffer pointed to by a BDT entry

0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit⁽¹⁾

1 = USB DMA error condition detected

0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit⁽²⁾

1 = Bus turnaround time-out has occurred

0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit

1 = Data field received is not an integral number of bytes

0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit

1 = Data packet is rejected due to CRC16 error

0 = Data packet is accepted

bit 1 **CRC5EF:** CRC5 Host Error Flag bit⁽⁴⁾

1 = Token packet is rejected due to CRC5 error

0 = Token packet is accepted

EOFEF: EOF Error Flag bit^(3,5)

1 = EOF error condition is detected

0 = No EOF error condition

bit 0 **PIDEF:** PID Check Failure Flag bit

1 = PID check is failed

0 = PID check is passed

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

PIC32MX5XX/6XX/7XX

REGISTER 11-9: U1IE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE ⁽¹⁾ EOFEE ⁽²⁾	PIDEE

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit

1 = BTSEF interrupt is enabled
0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit

1 = BMXEF interrupt is enabled
0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit

1 = DMAEF interrupt is enabled
0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit

1 = BTOEF interrupt is enabled
0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit

1 = DFN8EF interrupt is enabled
0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit

1 = CRC16EF interrupt is enabled
0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit⁽¹⁾

1 = CRC5EF interrupt is enabled
0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit⁽²⁾

1 = EOF interrupt is enabled
0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit

1 = PIDEF interrupt is enabled
0 = PIDEF interrupt is disabled

Note 1: Device mode.

2: Host mode.

Note: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

PIC32MX5XX/6XX/7XX

NOTES:

16.1 Control Registers

TABLE 16-1: INPUT CAPTURE 1-INPUT CAPTURE 5 REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	IC1CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																XXXX
		15:0	IC1BUF<31:0>																XXXX
2200	IC2CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																XXXX
		15:0	IC2BUF<31:0>																XXXX
2400	IC3CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																XXXX
		15:0	IC3BUF<31:0>																XXXX
2600	IC4CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																XXXX
		15:0	IC4BUF<31:0>																XXXX
2800	IC5CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																XXXX
		15:0	IC5BUF<31:0>																XXXX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

PIC32MX5XX/6XX/7XX

Figure 20-2 and Figure 20-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 20-2: UART RECEPTION

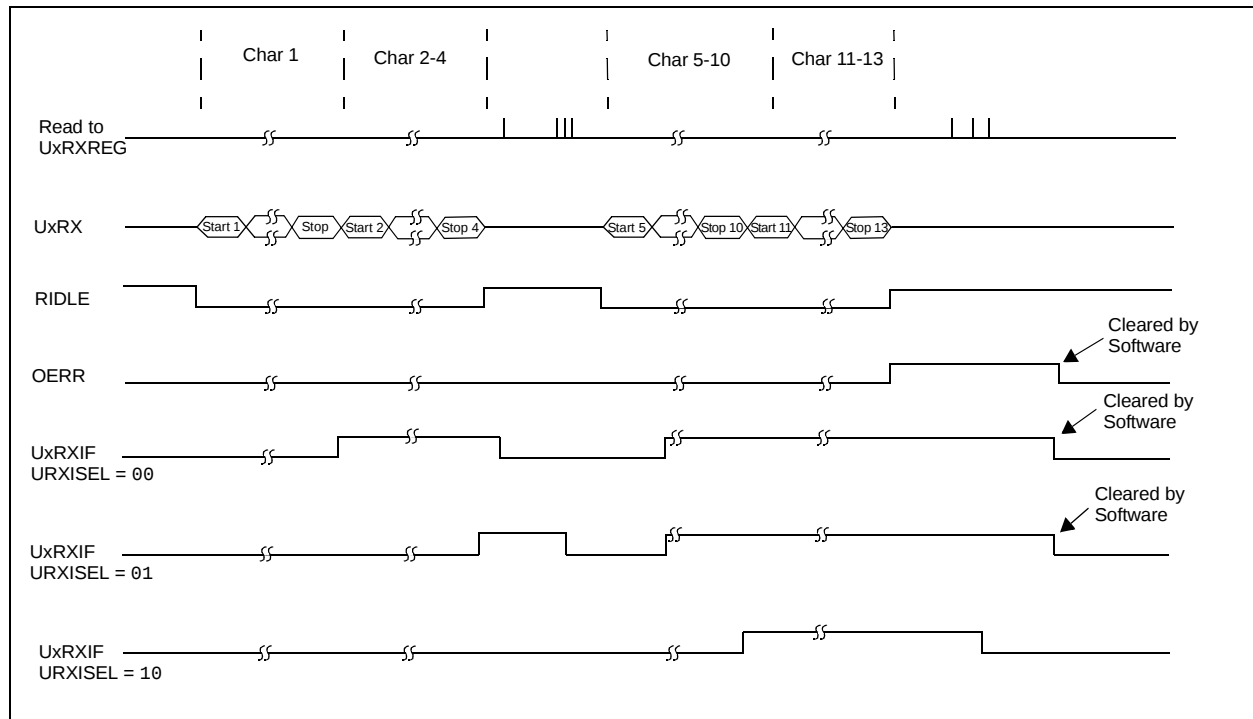
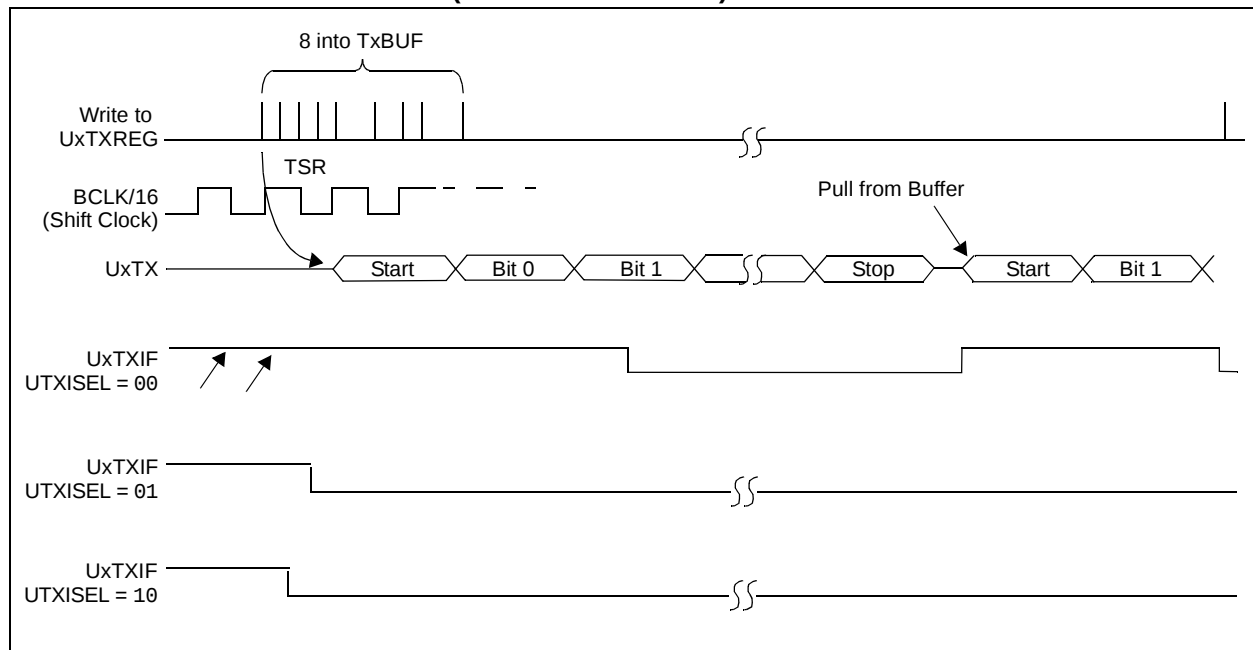


FIGURE 20-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



PIC32MX5XX/6XX/7XX

REGISTER 21-5: PMSTAT: PARALLEL PORT STATUS REGISTER (ONLY SLAVE MODES)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:

R = Readable bit

-n = Value at POR

HS = Set by Hardware

W = Writable bit

'1' = Bit is set

SC = Cleared by software

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit

1 = All writable input buffer registers are full

0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit

1 = A write attempt to a full input byte buffer occurred (must be cleared in software)

0 = An overflow has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits

1 = Input buffer contains data that has not been read (reading buffer will clear this bit)

0 = Input buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit

1 = All readable output buffer registers are empty

0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit

1 = A read occurred from an empty output byte buffer (must be cleared in software)

0 = An underflow has not occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits

1 = Output buffer is empty (writing data to the buffer will clear this bit)

0 = Output buffer contains data that has not been transmitted

24.0 CONTROLLER AREA NETWORK (CAN)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. “Controller Area Network (CAN)”** (DS60001154) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

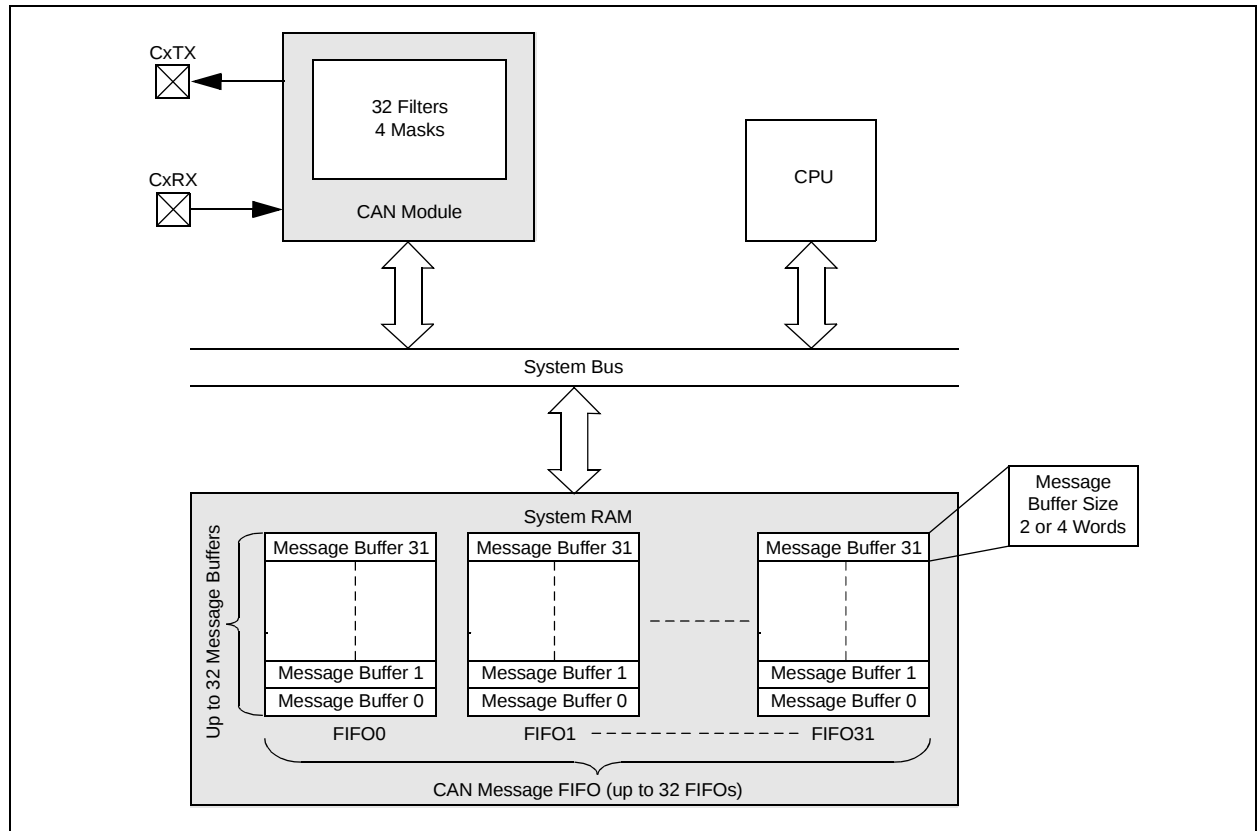
The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
 - Full CAN 2.0B compliance
 - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
 - 32 message FIFOs
 - Each FIFO can have up to 32 messages for a total of 1024 messages

- FIFO can be a transmit message FIFO or a receive message FIFO
- User-defined priority levels for message FIFOs used for transmission
- 32 acceptance filters for message filtering
- Four acceptance filter mask registers for message filtering
- Automatic response to remote transmit request
- DeviceNet™ addressing support
- Additional Features:
 - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
 - Low-power operating modes
 - CAN module is a bus master on the PIC32 system bus
 - Use of DMA is not required
 - Dedicated time-stamp timer
 - Dedicated DMA channels
 - Data-only Message Reception mode

Figure 24-1 illustrates the general structure of the CAN module.

FIGURE 24-1: PIC32 CAN MODULE BLOCK DIAGRAM



PIC32MX5XX/6XX/7XX

REGISTER 25-2: ETHCON2: ETHERNET CONTROLLER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RXBUFSZ<6:4>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RXBUFSZ<3:0>				—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-4 **RXBUFSZ<6:0>:** RX Data Buffer Size for All RX Descriptors (in 16-byte increments) bits

1111111 = RX data Buffer size for descriptors is 2032 bytes

.

.

1100000 = RX data Buffer size for descriptors is 1536 bytes

.

.

0000011 = RX data Buffer size for descriptors is 48 bytes

0000010 = RX data Buffer size for descriptors is 32 bytes

0000001 = RX data Buffer size for descriptors is 16 bytes

0000000 = Reserved

bit 3-0 **Unimplemented:** Read as '0'

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

PIC32MX5XX/6XX/7XX

NOTES:

TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions		
Idle Current (IDLE) ⁽¹⁾ for PIC32MX534/564/664/764 Family Devices						
DC30a	1.5	5	mA	-40°C, +25°C, +85°C	—	4 MHz
DC30c	3.5	6		+105°C		
DC31a	7	11		-40°C, +25°C, +85°C		
DC32a	13	20	mA	-40°C, +25°C, +85°C	—	25 MHz (Note 3)
DC33a	17	25	mA	-40°C, +25°C, +85°C	—	80 MHz
DC33c	20	27		+105°C		
DC34c	—	40	μA	-40°C	2.3V	LPRC (31 kHz) (Note 3)
DC34d		75		+25°C		
DC34e		800		+85°C		
DC34f		1000		+105°C		
DC35c	30	—	μA	-40°C	3.3V	
DC35d	55			+25°C		
DC35e	230			+85°C		
DC35f	800			+105°C		
DC36c	—	43	μA	-40°C	3.6V	
DC36d		106		+25°C		
DC36e		800		+85°C		
DC36f		1000		+105°C		

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0)
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to V_{SS}
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
- 2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** This parameter is characterized, but not tested in manufacturing.
- 4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

FIGURE 32-18: CAN MODULE I/O TIMING CHARACTERISTICS

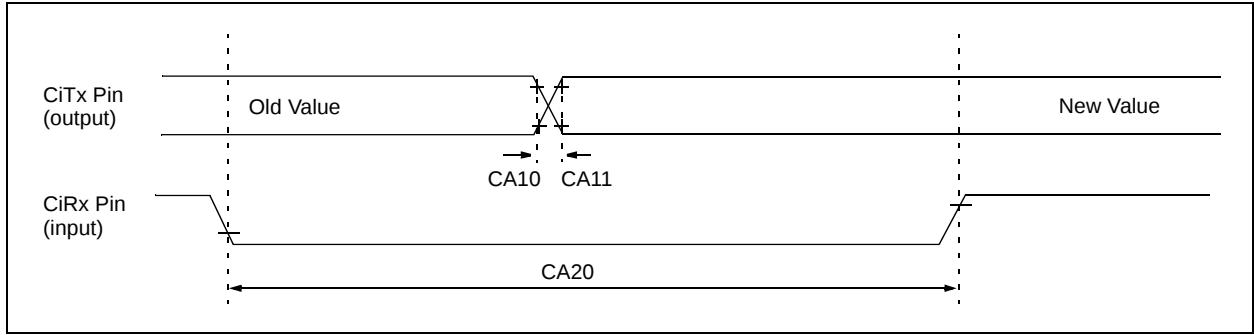


TABLE 32-34: CAN MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter DO31
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	700	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

PIC32MX5XX/6XX/7XX

Revision C (February 2010)

The revision includes the following updates, as described in Table B-2:

TABLE B-2: MAJOR SECTION UPDATES

Section Name	Update Description																								
“High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers”	Added the following devices: • PIC32MX675F256H • PIC32MX775F256H • PIC32MX775F512H • PIC32MX675F256L • PIC32MX775F256L • PIC32MX775F512L Added the following pins: • EREFCLK • ECRSDV • AEREFCLK • AECRSDV Added the EREFCLK and ECRSDV pins to Table 5 and Table 6.																								
1.0 “Device Overview”	Updated the pin number pinout I/O descriptions for the following pin names in Table 1-1: <table><tr><td>• SCL3</td><td>• SCL5</td><td>• RTCC</td><td>• C1OUT</td></tr><tr><td>• SDA3</td><td>• SDA5</td><td>• CVREF-</td><td>• C2IN-</td></tr><tr><td>• SCL2</td><td>• TMS</td><td>• CVREF+</td><td>• C2IN+</td></tr><tr><td>• SDA2</td><td>• TCK</td><td>• CVREFOUT</td><td>• C2OUT</td></tr><tr><td>• SCL4</td><td>• TDI</td><td>• C1IN-</td><td>• PMA0</td></tr><tr><td>• SDA4</td><td>• TDO</td><td>• C1IN+</td><td>• PMA1</td></tr></table> Added the following pins to the Pinout I/O Descriptions table (Table 1-1): • EREFCLK • ECRSDV • AEREFCLK • AECRSDV	• SCL3	• SCL5	• RTCC	• C1OUT	• SDA3	• SDA5	• CVREF-	• C2IN-	• SCL2	• TMS	• CVREF+	• C2IN+	• SDA2	• TCK	• CVREFOUT	• C2OUT	• SCL4	• TDI	• C1IN-	• PMA0	• SDA4	• TDO	• C1IN+	• PMA1
• SCL3	• SCL5	• RTCC	• C1OUT																						
• SDA3	• SDA5	• CVREF-	• C2IN-																						
• SCL2	• TMS	• CVREF+	• C2IN+																						
• SDA2	• TCK	• CVREFOUT	• C2OUT																						
• SCL4	• TDI	• C1IN-	• PMA0																						
• SDA4	• TDO	• C1IN+	• PMA1																						
4.0 “Memory Organization”	Added new devices and updated the virtual and physical memory map values in Figure 4-4. Added new devices to Figure 4-5. Added new devices to the following register maps: • Table 4-3, Table 4-4, Table 4-6 and Table 4-7 (Interrupt Register Maps) • Table 4-12 (I2C2 Register Map) • Table 4-15 (SPI1 Register Map) • Table 4-24 through Table 4-35 (PORTA-PORTG Register Maps) • Table 4-36 and Table 4-37 (Change Notice and Pull-up Register Maps) • Table 4-45 (CAN1 Register Map) • Table 4-46 (CAN2 Register Map) • Table 4-47 (Ethernet Controller Register Map) Changed the bits named POSCMD to POSCMOD in Table 4-42 (Device Configuration Word Summary).																								
1.0 “Special Features”	Changed all references of POSCMD to POSCMOD in the Device Configuration Word 1 register (see Register 1-2).																								
Appendix A: “Migrating from PIC32MX3XX/4XX to PIC32MX5XX/6XX/7XX Devices”	Added the new section Appendix .																								