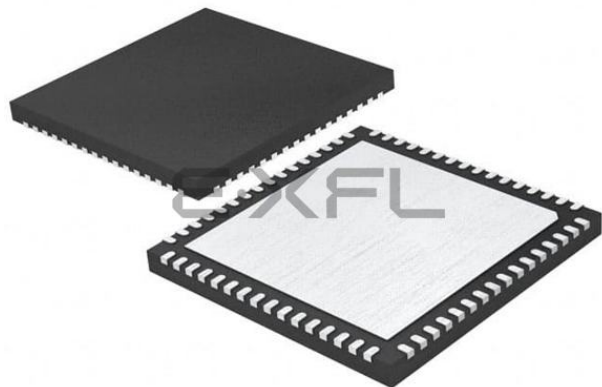




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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f256h-80i-mr

PIC32MX5XX/6XX/7XX

TABLE 7: PIN NAMES FOR 100-PIN USB AND CAN DEVICES

100-PIN TQFP (TOP VIEW)			
PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX575F512L PIC32MX575F256L		100 1	
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RG15	36	VSS
2	VDD	37	VDD
3	PMD5/RE5	38	TCK/RA1
4	PMD6/RE6	39	AC1TX/SCK4/U5TX/U2RTS/RF13
5	PMD7/RE7	40	AC1RX/SS4/U5RX/U2CTS/RF12
6	T2CK/RC1	41	AN12/PMA11/RB12
7	T3CK/RC2	42	AN13/PMA10/RB13
8	T4CK/RC3	43	AN14/PMALH/PMA1/RB14
9	T5CK/SDI1/RC4	44	AN15/OCFB/PMALL/PMA0/CN12/RB15
10	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	45	VSS
11	SDA4/SDI2/U3RX/PMA4/CN9/RG7	46	VDD
12	SCL4/SDO2/U3TX/PMA3/CN10/RG8	47	SS3/U4RX/U1CTS/CN20/RD14
13	MCLR	48	SCK3/U4TX/U1RTS/CN21/RD15
14	SS2/U6RX/U3CTS/PMA2/CN11/RG9	49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
15	VSS	50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
16	VDD	51	USBID/RF3
17	TMS/RA0	52	SDA3/SDI3/U1RX/RF2
18	INT1/RE8	53	SCL3/SDO3/U1TX/RF8
19	INT2/RE9	54	VBUS
20	AN5/C1IN+/VBUSON/CN7/RB5	55	VUSB3V3
21	AN4/C1IN-/CN6/RB4	56	D-/RG3
22	AN3/C2IN+/CN5/RB3	57	D+/RG2
23	AN2/C2IN-/CN4/RB2	58	SCL2/RA2
24	PGEC1/AN1/CN3/RB1	59	SDA2/RA3
25	PGED1/AN0/CN2/RB0	60	TDI/RA4
26	PGEC2/AN6/OCFA/RB6	61	TDO/RA5
27	PGED2/AN7/RB7	62	VDD
28	VREF-/CVREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	SCL1/INT3/RA14
32	AN8/C1OUT/RB8	67	SDA1/INT4/RA15
33	AN9/C2OUT/RB9	68	RTCC/IC1/RD8
34	AN10/CVREFOUT/PMA13/RB10	69	SS1/IC2/RD9
35	AN11/PMA12/RB11	70	SCK1/IC3/PMCS2/PMA15/RD10

Note 1: Shaded pins are 5V tolerant.

TABLE 7: PIN NAMES FOR 100-PIN USB AND CAN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MX534F064L
 PIC32MX564F064L
 PIC32MX564F128L
 PIC32MX575F512L
 PIC32MX575F256L

100

1

Pin #	Full Pin Name
71	IC4/PMCS1/PMA14/RD11
72	SDO1/OC1/INT0/RD0
73	SOSCI/CN1/RC13
74	SOSCO/T1CK/CN0/RC14
75	Vss
76	OC2/RD1
77	OC3/RD2
78	OC4/RD3
79	IC5/PMD12/RD12
80	PMD13/CN19/RD13
81	OC5/PMWR/CN13/RD4
82	PMRD/CN14/RD5
83	PMD14/CN15/RD6
84	PMD15/CN16/RD7
85	VCAP

Pin #	Full Pin Name
86	VDD
87	C1RX/PMD11/RF0
88	C1TX/PMD10/RF1
89	PMD9/RG1
90	PMD8/RG0
91	TRCLK/RA6
92	TRD3/RA7
93	PMD0/RE0
94	PMD1/RE1
95	TRD2/RG14
96	TRD1/RG12
97	TRD0/RG13
98	PMD2/RE2
99	PMD3/RE3
100	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 9: PIN NAMES FOR 100-PIN USB, ETHERNET, AND CAN DEVICES

100-PIN TQFP (TOP VIEW)			
PIC32MX764F128L PIC32MX775F256L PIC32MX775F512L PIC32MX795F512L		100	
		1	
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AERXERR/RG15	36	Vss
2	VDD	37	VDD
3	PMD5/RE5	38	TCK/RA1
4	PMD6/RE6	39	AC1TX/SCK4/U5TX/U2RTS/RF13
5	PMD7/RE7	40	AC1RX/SS4/U5RX/U2CTS/RF12
6	T2CK/RC1	41	AN12/ERXD0/AECRS/PMA11/RB12
7	T3CK/AC2TX ⁽¹⁾ /RC2	42	AN13/ERXD1/AECOL/PMA10/RB13
8	T4CK/AC2RX ⁽¹⁾ /RC3	43	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14
9	T5CK/SD11/RC4	44	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
10	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6	45	Vss
11	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7	46	VDD
12	ERXDVI/AERXDV/ECRS/SDV/AECRS/SDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8	47	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
13	MCLR	48	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
14	ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9	49	SDA5/SDI4/U2RX/PMA9/CN17/RF4
15	Vss	50	SCL5/SDO4/U2TX/PMA8/CN18/RF5
16	VDD	51	USBID/RF3
17	TMS/RA0	52	SDA3/SDI3/U1RX/RF2
18	AERXD0/INT1/RE8	53	SCL3/SDO3/U1TX/RF8
19	AERXD1/INT2/RE9	54	VBUS
20	AN5/C1IN+/VBUSON/CN7/RB5	55	VUSB3V3
21	AN4/C1IN-/CN6/RB4	56	D-/RG3
22	AN3/C2IN+/CN5/RB3	57	D+/RG2
23	AN2/C2IN-/CN4/RB2	58	SCL2/RA2
24	PGEC1/AN1/CN3/RB1	59	SDA2/RA3
25	PGED1/AN0/CN2/RB0	60	TDI/RA4
26	PGEC2/AN6/OCFA/RB6	61	TDO/RA5
27	PGED2/AN7/RB7	62	VDD
28	VREF-/CVREF-/AERXD2/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/AERXD3/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	Vss
31	AVss	66	AETXCLK/SCL1/INT3/RA14
32	AN8/C1OUT/RB8	67	AETXEN/SDA1/INT4/RA15
33	AN9/C2OUT/RB9	68	RTCC/EMDIO/AEMDIO/IC1/RD8
34	AN10/CVREFOUT/PMA13/RB10	69	SS1/IC2/RD9
35	AN11/ERXERR/AETXERR/PMA12/RB11	70	SCK1/IC3/PMCS2/PMA15/RD10

Note 1: This pin is not available on PIC32MX764F128L devices.
2: Shaded pins are 5V tolerant.

PIC32MX5XX/6XX/7XX

TABLE 13: PIN NAMES FOR 124-PIN USB, ETHERNET, AND CAN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)^(2,3)		A17	B13	B29	A34	Conductive Thermal Pad
PIC32MX675F512L PIC32MX695F512L PIC32MX795F512L		A1	B1	B56	B41	A51
		A1	Polarity Indicator		A68	
Package Bump #	Full Pin Name	Package Bump #	Full Pin Name	Package Bump #	Full Pin Name	Package Bump #
B8	VSS	B33	TDO/RA5	B33	TDO/RA5	
B9	TMS/RA0	B34	OSC1/CLKI/RC12	B34	OSC1/CLKI/RC12	
B10	AERXD1/INT2/RE9	B35	No Connect (NC)	B35	No Connect (NC)	
B11	AN4/C1IN-/CN6/RB4	B36	AETXCLK/SCL1/INT3/RA14	B36	AETXCLK/SCL1/INT3/RA14	
B12	VSS	B37	RTCC/EMDIO/AEMDIO/IC1/RD8	B37	RTCC/EMDIO/AEMDIO/IC1/RD8	
B13	AN2/C2IN-/CN4/RB2	B38	SCK1/IC3/PMCS2/PMA15/RD10	B38	SCK1/IC3/PMCS2/PMA15/RD10	
B14	PGED1/AN0/CN2/RB0	B39	SDO1/OC1/INT0/RD0	B39	SDO1/OC1/INT0/RD0	
B15	No Connect (NC)	B40	SOSCO/T1CK/CN0/RC14	B40	SOSCO/T1CK/CN0/RC14	
B16	PGED2/AN7/RB7	B41	VSS	B41	VSS	
B17	VREF+/CVREF+/AERXD3/PMA6/RA10	B42	OC3/RD2	B42	OC3/RD2	
B18	AVSS	B43	ETXD2/IC5/PMD12/RD12	B43	ETXD2/IC5/PMD12/RD12	
B19	AN9/C2OUT/RB9	B44	OC5/PMWR/CN13/RD4	B44	OC5/PMWR/CN13/RD4	
B20	AN11/ERXERR/AETXERR/PMA12/RB11	B45	ETXEN/PMD14/CN15/RD6	B45	ETXEN/PMD14/CN15/RD6	
B21	VDD	B46	VSS	B46	VSS	
B22	AC1TX/SCK4/U5TX/U2RTS/RF13	B47	No Connect (NC)	B47	No Connect (NC)	
B23	AN12/ERXD0/AECRS/PMA11/RB12	B48	VCAP	B48	VCAP	
B24	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14	B49	C1RX ⁽¹⁾ /ETXD1/PMD11/RF0	B49	C1RX ⁽¹⁾ /ETXD1/PMD11/RF0	
B25	VSS	B50	C2TX ⁽¹⁾ /ETXERR/PMD9/RG1	B50	C2TX ⁽¹⁾ /ETXERR/PMD9/RG1	
B26	AETXD0/SS3/U4RX/U1CTS/CN20/RD14	B51	TRCLK/RA6	B51	TRCLK/RA6	
B27	SDA5/SDI4/U2RX/PMA9/CN17/RF4	B52	PMD0/RE0	B52	PMD0/RE0	
B28	No Connect (NC)	B53	VDD	B53	VDD	
B29	SCL3/SDO3/U1TX/RF8	B54	TRD2/RG14	B54	TRD2/RG14	
B30	VUSB3V3	B55	TRD0/RG13	B55	TRD0/RG13	
B31	D+/RG2	B56	PMD3/RE3	B56	PMD3/RE3	

- Note**
- 1: This pin is only available on PIC32MX795F512L devices.
 - 2: Shaded package bumps are 5V tolerant.
 - 3: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

6.1 Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets ⁽²⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F600	RCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	0000
F610	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.

PIC32MX5XX/6XX/7XX

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

Interrupt Source ⁽¹⁾	IRQ Number	Vector Number	Interrupt Bit Location			
			Flag	Enable	Priority	Sub-Priority
Highest Natural Order Priority						
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>
INT0 – External Interrupt 0	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>
IC1 – Input Capture 1	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>
OC1 – Output Compare 1	6	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>
INT1 – External Interrupt 1	7	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>
T2 – Timer2	8	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>
IC2 – Input Capture 2	9	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>
OC2 – Output Compare 2	10	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>
INT2 – External Interrupt 2	11	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>
T3 – Timer3	12	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>
IC3 – Input Capture 3	13	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>
OC3 – Output Compare 3	14	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>
INT3 – External Interrupt 3	15	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>
T4 – Timer4	16	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>
IC4 – Input Capture 4	17	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>
OC4 – Output Compare 4	18	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>
INT4 – External Interrupt 4	19	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>
T5 – Timer5	20	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>
IC5 – Input Capture 5	21	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>
OC5 – Output Compare 5	22	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>
SPI1E – SPI1 Fault	23	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>
SPI1RX – SPI1 Receive Done	24	23	IFS0<24>	IEC0<24>	IPC5<28:26>	IPC5<25:24>
SPI1TX – SPI1 Transfer Done	25	23	IFS0<25>	IEC0<25>	IPC5<28:26>	IPC5<25:24>
U1E – UART1 Error	26	24	IFS0<26>	IEC0<26>	IPC6<4:2>	IPC6<1:0>
SPI3E – SPI3 Fault						
I2C3B – I2C3 Bus Collision Event						
U1RX – UART1 Receiver	27	24	IFS0<27>	IEC0<27>	IPC6<4:2>	IPC6<1:0>
SPI3RX – SPI3 Receive Done						
I2C3S – I2C3 Slave Event						
U1TX – UART1 Transmitter	28	24	IFS0<28>	IEC0<28>	IPC6<4:2>	IPC6<1:0>
SPI3TX – SPI3 Transfer Done						
I2C3M – I2C3 Master Event						
I2C1B – I2C1 Bus Collision Event	29	25	IFS0<29>	IEC0<29>	IPC6<12:10>	IPC6<9:8>
I2C1S – I2C1 Slave Event	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>
I2C1M – I2C1 Master Event	31	25	IFS0<31>	IEC0<31>	IPC6<12:10>	IPC6<9:8>
CN – Input Change Interrupt	32	26	IFS1<0>	IEC1<0>	IPC6<20:18>	IPC6<17:16>

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX5XX USB and CAN Features”**, **TABLE 2: “PIC32MX6XX USB and Ethernet Features”** and **TABLE 3: “PIC32MX7XX USB, Ethernet, and CAN Features”** for the list of available peripherals.

TABLE 7-3: INTERRUPT REGISTER MAP FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H AND PIC32MX695F512H DEVICES

Virtual Address (BF88..#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>				—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
1010	INTSTAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>				—	—	VEC<5:0>					0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
		31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	—	—	USBIF	FCEIF	DMA7IF ⁽²⁾	DMA6IF ⁽²⁾	DMA5IF ⁽²⁾	DMA4IF ⁽²⁾	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
1040	IFS1	15:0	RTCCIF	FSCMIF	—	—	—	U2TXIF SPI4TXIF I2C5MIF	U2RXIF SPI4RXIF I2C5SIF	U2EIF SPI4EIF I2C5BIF	U3TXIF SPI2TXIF I2C4MIF	U3RXIF SPI2RXIF I2C4SIF	U3EIF SPI2EIF I2C4BIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
		31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	—	—	USBIE	FCEIE	DMA7IE ⁽²⁾	DMA6IE ⁽²⁾	DMA5IE ⁽²⁾	DMA4IE ⁽²⁾	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
1070	IEC1	15:0	RTCCIE	FSCMIE	—	—	—	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE
1090	IPC0	31:16	—	—	—	—	—	INT0IP<2:0>	—	—	—	—	—	—	—	CS1IP<2:0>	—	CS1IS<1:0>	0000
		15:0	—	—	—	—	—	CS0IP<2:0>	—	—	—	—	—	—	—	CTIP<2:0>	—	CTIS<1:0>	0000
10A0	IPC1	31:16	—	—	—	—	—	INT1IP<2:0>	—	—	—	—	—	—	—	OC1IP<2:0>	—	OC1IS<1:0>	0000
		15:0	—	—	—	—	—	IC1IP<2:0>	—	—	—	—	—	—	—	T1IP<2:0>	—	T1IS<1:0>	0000
10B0	IPC2	31:16	—	—	—	—	—	INT2IP<2:0>	—	—	—	—	—	—	—	OC2IP<2:0>	—	OC2IS<1:0>	0000
		15:0	—	—	—	—	—	IC2IP<2:0>	—	—	—	—	—	—	—	T2IP<2:0>	—	T2IS<1:0>	0000
10C0	IPC3	31:16	—	—	—	—	—	INT3IP<2:0>	—	—	—	—	—	—	—	OC3IP<2:0>	—	OC3IS<1:0>	0000
		15:0	—	—	—	—	—	IC3IP<2:0>	—	—	—	—	—	—	—	T3IP<2:0>	—	T3IS<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- 2: These bits are not available on PIC32MX664 devices.
- 3: This register does not have associated CLR, SET, and INV registers.

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REGISTER 11-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 11-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

16.1 Control Registers

TABLE 16-1: INPUT CAPTURE 1-INPUT CAPTURE 5 REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	IC1CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																xxxx
		15:0	IC1BUF<31:0>																xxxx
2200	IC2CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																xxxx
		15:0	IC2BUF<31:0>																xxxx
2400	IC3CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																xxxx
		15:0	IC3BUF<31:0>																xxxx
2600	IC4CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																xxxx
		15:0	IC4BUF<31:0>																xxxx
2800	IC5CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																xxxx
		15:0	IC5BUF<31:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

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REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

- bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)
1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
0 = Normal operation, buffer contents will be overwritten by the next conversion sequence
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
0 = Sampling begins when SAMP bit is set
- bit 1 **SAMP:** ADC Sample Enable bit⁽²⁾
1 = The ADC S&H circuit is sampling
0 = The ADC S&H circuit is holding
When ASAM = 0, writing '1' to this bit starts sampling.
When SSRC<2:0> = 000, writing '0' to this bit will end sampling and start conversion.
- bit 0 **DONE:** Analog-to-Digital Conversion Status bit⁽³⁾
Clearing this bit will not affect any operation in progress.
1 = Analog-to-digital conversion is done
0 = Analog-to-digital conversion is not done or has not started

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write a '0' to end sampling and start conversion. If SSRC<2:0> ≠ '000', this bit is automatically cleared by hardware to end sampling and start conversion.
- 3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)

- bit 13 **SIDLE:** CAN Stop in Idle bit
 1 = CAN Stops operation when system enters Idle mode
 0 = CAN continues operation when system enters Idle mode
- bit 12 **Unimplemented:** Read as '0'
- bit 11 **CANBUSY:** CAN Module is Busy bit
 1 = The CAN module is active
 0 = The CAN module is completely disabled
- bit 10-5 **Unimplemented:** Read as '0'
- bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
 10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
 10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
 •
 •
 •
 00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
 00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 24-10: C_iFLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 15	FLTEN1: Filter 1 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 14-13	MSEL1<1:0>: Filter 1 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 12-8	FSEL1<4:0>: FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 . . . 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0
bit 7	FLTEN0: Filter 0 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 6-5	MSEL0<1:0>: Filter 0 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 4-0	FSEL0<4:0>: FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 . . . 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTEN _n) bit is '0'.
--

REGISTER 24-15: CifLTCON5: CAN FILTER CONTROL REGISTER 5 (CONTINUED)

- bit 15 **FLTEN21**: Filter 21 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 14-13 **MSEL21<1:0>**: Filter 21 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL21<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 .
 .
 .
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN20**: Filter 20 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 6-5 **MSEL20<1:0>**: Filter 20 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL20<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 .
 .
 .
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

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REGISTER 24-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	FSIZE<4:0> ⁽¹⁾				
15:8	U-0	S/HC-0	S/HC-0	R/W-0	U-0	U-0	U-0	U-0
	—	FRESET	UINC	DONLY ⁽¹⁾	—	—	—	—
7:0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXEN	TXABAT ⁽²⁾	TXLARB ⁽³⁾	TXERR ⁽³⁾	TXREQ	RTREN	TXPR<1:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **FSIZE<4:0>:** FIFO Size bits⁽¹⁾

11111 = FIFO is 32 messages deep

•
•
•

00010 = FIFO is 3 messages deep

00001 = FIFO is 2 messages deep

00000 = FIFO is 1 message deep

bit 15 **Unimplemented:** Read as '0'

bit 14 **FRESET:** FIFO Reset bits

1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset. After setting, the user should poll whether this bit is clear before taking any action.

0 = No effect

bit 13 **UINC:** Increment Head/Tail bit

TXEN = 1: (FIFO configured as a Transmit FIFO)

When this bit is set the FIFO head will increment by a single message

TXEN = 0: (FIFO configured as a Receive FIFO)

When this bit is set the FIFO tail will increment by a single message

bit 12 **DONLY:** Store Message Data Only bit⁽¹⁾

TXEN = 1: (FIFO configured as a Transmit FIFO)

This bit is not used and has no effect.

TXEN = 0: (FIFO configured as a Receive FIFO)

1 = Only data bytes will be stored in the FIFO

0 = Full message is stored, including identifier

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **TXEN:** TX/RX Buffer Selection bit

1 = FIFO is a Transmit FIFO

0 = FIFO is a Receive FIFO

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).

2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

3: This bit is reset on any read of this register or when the FIFO is reset.

27.1 Control Register

TABLE 27-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9800	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	VREFSEL ⁽²⁾	BGSEL<1:0> ⁽²⁾	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0100

- Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** These bits are not available on PIC32MX575/675/695/775/795 devices. On these devices, reset value for CVRCON is '0000'.

REGISTER 27-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON ⁽¹⁾	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 VREFSEL ⁽²⁾	R/W-0 BGSEL<1:0> ⁽²⁾	R/W-1
7:0	U-0 —	R/W-0 CVROE	R/W-0 CVRR	R/W-0 CVRSS	R/W-0	R/W-0	R/W-0	R/W-0
CVR<3:0>								

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit⁽¹⁾

Setting or clearing this bit does not affect the other bits in this register.

1 = Module is enabled

0 = Module is disabled and does not consume current

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Voltage Reference Select bit⁽²⁾

1 = CVREF = VREF+

0 = CVREF is generated by the resistor network

bit 9-8 **BGSEL<1:0>:** Band Gap Reference Source bits⁽²⁾

11 = IVREF = VREF+

10 = Reserved

01 = IVREF = 0.6V (nominal, default)

00 = IVREF = 1.2V (nominal)

bit 7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** CVREFOUT Enable bit

1 = Voltage level is output on CVREFOUT pin

0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit

1 = 0 to 0.625 CVRSRC, with CVRSRC/24 step size

0 = 0.25 CVRSRC to 0.719 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit

1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)

0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \leq \text{CVR}<3:0> \leq 15$ bits

When CVRR = 1:

$\text{CVREF} = (\text{CVR}<3:0>/24) \cdot (\text{CVRSRC})$

When CVRR = 0:

$\text{CVREF} = 1/4 \cdot (\text{CVRSRC}) + (\text{CVR}<3:0>/32) \cdot (\text{CVRSRC})$

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: These bits are not available on PIC32MX575/675/775/795 devices. On these devices, the reset value for CVRON is '0000'.

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NOTES:

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TABLE 32-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	Output Low Voltage I/O Pins: 4x Sink Driver Pins - All I/O output pins not defined as 8x Sink Driver pins	—	—	0.4	V	IOL ≤ 10 mA, VDD = 3.3V
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RC15	—	—	0.4	V	IOL ≤ 15 mA, VDD = 3.3V
DO20	VOH	Output High Voltage I/O Pins: 4x Source Driver Pins - All I/O output pins not defined as 8x Source Driver pins	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - RC15	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	Output High Voltage I/O Pins: 4x Source Driver Pins - All I/O output pins not defined as 8x Sink Driver pins	1.5 ⁽¹⁾	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0 ⁽¹⁾	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0 ⁽¹⁾	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - RC15	1.5 ⁽¹⁾	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0 ⁽¹⁾	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0 ⁽¹⁾	—	—		IOH ≥ -10 mA, VDD = 3.3V

- Note 1:** Parameters are characterized, but not tested.
2: This driver pin only applies to devices with less than 64 pins.
3: This driver pin only applies to devices with 64 pins.

TABLE 32-10: ELECTRICAL CHARACTERISTICS: BOR

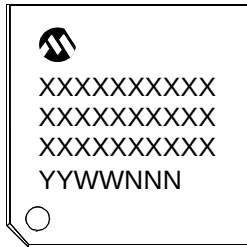
DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min. ⁽¹⁾	Typical	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD transition high-to-low (Note 2)	2.0	—	2.3	V	—

- Note 1:** Parameters are for design guidance only and are not tested in manufacturing.
2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

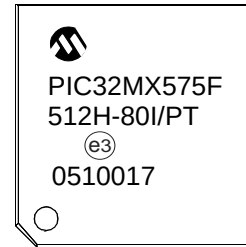
34.0 PACKAGING INFORMATION

34.1 Package Marking Information

64-Lead TQFP (10x10x1 mm)



Example



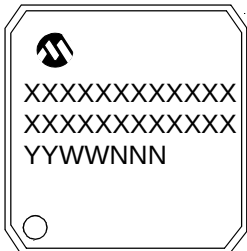
100-Lead TQFP (14x14x1 mm)



Example



100-Lead TQFP (12x12x1 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	*	Pb-free JEDEC designator for Matte Tin (Sn)
		This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.