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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f256h-80i-pt

Referenced Sources

This device data sheet is based on the following individual chapters of the “PIC32 Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the PIC32MX795F512L product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. “Introduction”** (DS60001127)
- **Section 2. “CPU”** (DS60001113)
- **Section 4. “Prefetch Cache”** (DS60001119)
- **Section 3. “Memory Organization”** (DS60001115)
- **Section 5. “Flash Program Memory”** (DS60001121)
- **Section 6. “Oscillator Configuration”** (DS60001112)
- **Section 7. “Resets”** (DS60001118)
- **Section 8. “Interrupt Controller”** (DS60001108)
- **Section 9. “Watchdog Timer and Power-up Timer** (DS60001114)
- **Section 10. “Power-Saving Features”** (DS60001130)
- **Section 12. “I/O Ports”** (DS60001120)
- **Section 13. “Parallel Master Port (PMP)”** (DS60001128)
- **Section 14. “Timers”** (DS60001105)
- **Section 15. “Input Capture”** (DS60001122)
- **Section 16. “Output Capture”** (DS60001111)
- **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104)
- **Section 19. “Comparator”** (DS60001110)
- **Section 20. “Comparator Voltage Reference (CVREF)”** (DS60001109)
- **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107)
- **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106)
- **Section 24. “Inter-Integrated Circuit (I2C)”** (DS60001116)
- **Section 27. “USB On-The-Go (OTG)”** (DS60001126)
- **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125)
- **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117)
- **Section 32. “Configuration”** (DS60001124)
- **Section 33. “Programming and Diagnostics”** (DS60001129)
- **Section 34. “Controller Area Network (CAN)”** (DS60001154)
- **Section 35. “Ethernet Controller”** (DS60001155)

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TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number ⁽¹⁾				Pin Type	Buffer Type	Description
	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA			
AN0	16	25	K2	B14	I	Analog	Analog input channels
AN1	15	24	K1	A15	I	Analog	
AN2	14	23	J2	B13	I	Analog	
AN3	13	22	J1	A13	I	Analog	
AN4	12	21	H2	B11	I	Analog	
AN5	11	20	H1	A12	I	Analog	
AN6	17	26	L1	A20	I	Analog	
AN7	18	27	J3	B16	I	Analog	
AN8	21	32	K4	A23	I	Analog	
AN9	22	33	L4	B19	I	Analog	
AN10	23	34	L5	A24	I	Analog	
AN11	24	35	J5	B20	I	Analog	
AN12	27	41	J7	B23	I	Analog	
AN13	28	42	L7	A28	I	Analog	
AN14	29	43	K7	B24	I	Analog	
AN15	30	44	L8	A29	I	Analog	
CLKI	39	63	F9	B34	I	ST/ CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	40	64	F11	A42	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	39	63	F9	B34	I	ST/ CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	40	64	F11	A42	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	73	C10	A47	I	ST/ CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise
SOSCO	48	74	B11	B40	O	—	32.768 kHz low-power oscillator crystal output

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input P = Power
O = Output I = Input

Note 1: Pin numbers are only provided for reference. See the “**Device Pin Tables**” section for device pin availability.

2: See **25.0 “Ethernet Controller”** for more information.

9.2 Control Registers

TABLE 9-1: PREFETCH REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
4000	CHECON ^(1,2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHECOH	0000		
		15:0	—	—	—	—	—	DCSZ<1:0>			—	—	PREFEN<1:0>		—	PFMWS<2:0>			0007		
4010	CHEACC ⁽¹⁾	31:16	CHEWEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CHEIDX<3:0>					0000	
4020	CHETAG ⁽¹⁾	31:16	LTAGBOOT	—	—	—	—	—	—	—	LTAG<23:16>										00xx
		15:0	LTAG<15:4>												LVALID	LLOCK	LTYPE	—	xxx2		
4030	CHEMSK ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	LMASK<15:5>												—	—	—	—	—	0000	
4040	CHEW0	31:16	CHEW0<31:0>																xxxx		
		15:0	CHEW0<31:0>																xxxx		
4050	CHEW1	31:16	CHEW1<31:0>																xxxx		
		15:0	CHEW1<31:0>																xxxx		
4060	CHEW2	31:16	CHEW2<31:0>																xxxx		
		15:0	CHEW2<31:0>																xxxx		
4070	CHEW3	31:16	CHEW3<31:0>																xxxx		
		15:0	CHEW3<31:0>																xxxx		
4080	CHELRU	31:16	—	—	—	—	—	—	—	CHELRU<24:16>										0000	
		15:0	CHELRU<15:0>																0000		
4090	CHEHIT	31:16	CHEHIT<31:0>																xxxx		
		15:0	CHEHIT<31:0>																xxxx		
40A0	CHEMIS	31:16	CHEMIS<31:0>																xxxx		
		15:0	CHEMIS<31:0>																xxxx		
40C0	CHEPFABT	31:16	CHEPFABT<31:0>																xxxx		
		15:0	CHEPFABT<31:0>																xxxx		

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
 2: Reset value is dependent on DEVCFGx configuration.

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
 0 = No interrupt is pending
- bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
 0 = No interrupt is pending
- bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a
 pattern match event occurs
 0 = No interrupt is pending
- bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
 0 = No interrupt is pending
- bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
 0 = No interrupt is pending
- bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
 1 = A channel address error has been detected (either the source or the destination address is invalid)
 0 = No interrupt is pending

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REGISTER 11-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit

1 = Next token command to be executed at low-speed

0 = Next token command to be executed at full-speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 11-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

12.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. “I/O Ports”** (DS60001120) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

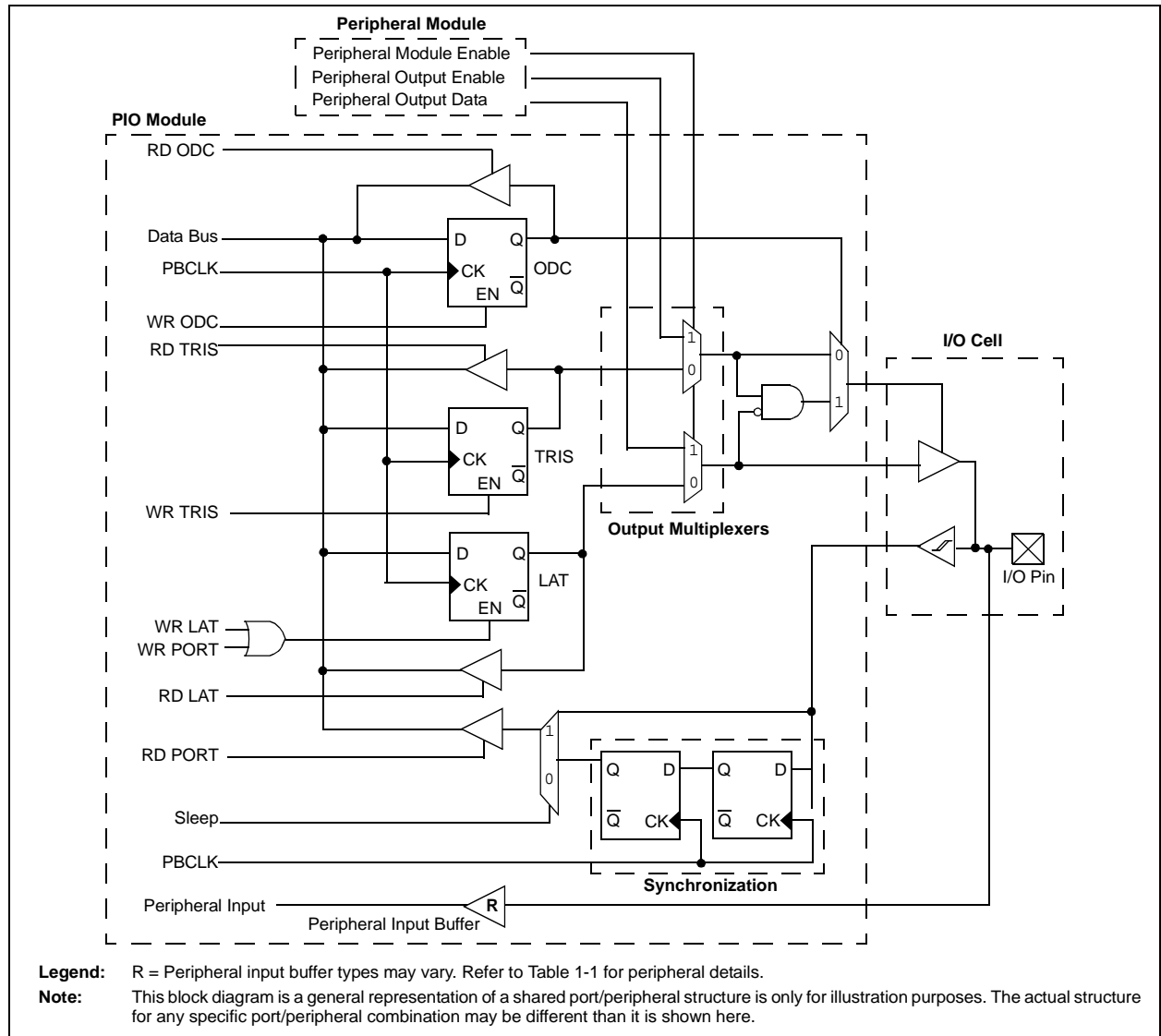
Following are some of the key features of this module:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up enable/disable
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

General purpose I/O pins are the simplest of peripherals. They allow the PIC32 MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



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12.1 Parallel I/O (PIO) Ports

All port pins have three registers (TRIS, LAT and PORT) that are directly associated with their operation.

TRIS is a Data Direction or Tri-State Control register that determines whether a digital pin is an input or an output. Setting a TRISx register bit = 1, configures the corresponding I/O pin as an input; setting a TRISx register bit = 0, configures the corresponding I/O pin as an output. All port I/O pins are defined as inputs after a device Reset. Certain I/O pins are shared with analog peripherals and default to analog inputs after a device Reset.

PORT is a register used to read the current state of the signal applied to the port I/O pins. Writing to a PORTx register performs a write to the port's latch, LATx register, latching the data to the port's I/O pins.

LAT is a register used to write data to the port I/O pins. The LATx Latch register holds the data written to either the LATx or PORTx registers. Reading the LATx Latch register reads the last value written to the corresponding PORT or Latch register.

Not all port I/O pins are implemented on some devices, therefore, the corresponding PORTx, LATx and TRISx register bits will read as zeros.

12.1.1 CLR, SET AND INV REGISTERS

Every I/O module register has a corresponding Clear (CLR), Set (SET) and Invert (INV) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

Note: Using a PORTxINV register to toggle a bit is recommended because the operation is performed in hardware atomically, using fewer instructions, as compared to the traditional read-modify-write method, as follows:

```
PORTC ^ = 0x0001;
```

12.1.2 DIGITAL INPUTS

Pins are configured as digital inputs by setting the corresponding TRIS register bits = 1. When configured as inputs, they are either TTL buffers or Schmitt Triggers. Several digital pins share functionality with analog inputs and default to the analog inputs at POR. Setting the corresponding bit in the AD1PCFG register = 1 enables the pin as a digital pin.

The maximum input voltage allowed on the input pins is the same as the maximum V_{IH} specification. Refer to **Section 32.0 "Electrical Characteristics"** for V_{IH} specification details.

Note: Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

12.1.3 ANALOG INPUTS

Certain pins can be configured as analog inputs used by the ADC and comparator modules. Setting the corresponding bits in the AD1PCFG register = 0 enables the pin as an analog input pin and must have the corresponding TRIS bit set = 1 (input). If the TRIS bit is cleared = 0 (output), the digital output level (V_{OH} or V_{OL}) will be converted. Any time a port I/O pin is configured as analog, its digital input is disabled and the corresponding PORTx register bit will read '0'. The AD1PCFG register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

12.1.4 DIGITAL OUTPUTS

Pins are configured as digital outputs by setting the corresponding TRIS register bits = 0. When configured as digital outputs, these pins are CMOS drivers or can be configured as open-drain outputs by setting the corresponding bits in the Open-Drain Configuration (ODCx) register.

The open-drain feature allows generation of outputs higher than V_{DD} (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

See the **"Device Pin Tables"** section for the available pins and their functionality.

12.1.5 ANALOG OUTPUTS

Certain pins can be configured as analog outputs, such as the CVREF output voltage used by the comparator module. Configuring the comparator reference module to provide this output will present the analog output voltage on the pin, independent of the TRIS register setting for the corresponding pin.

12.1.6 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports (CNx) allows devices to generate interrupt requests in response to change-of-state on selected pin.

Each CNx pin also has a weak pull-up, which acts as a current source connected to the pin. The pull-ups are enabled by setting the corresponding bit in the CNPUE register.

REGISTER 14-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

bit 3	T32: 32-Bit Timer Mode Select bit ⁽²⁾ 1 = Odd numbered and even numbered timers form a 32-bit timer 0 = Odd numbered and even numbered timers form a separate 16-bit timer
bit 2	Unimplemented: Read as '0'
bit 1	TCS: Timer Clock Source Select bit ⁽³⁾ 1 = External clock from TxCK pin 0 = Internal peripheral clock
bit 0	Unimplemented: Read as '0'

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit is only available on even numbered timers (Timer2 and Timer4).
- 3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, and Timer5). All timer functions are set through the even numbered timers.
- 4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON ^(1,2)	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	—	SWDTPS<4:0>					WDTWINEN	WDTCLR

Legend:

y = Values set from Configuration bits on POR
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit^(1,2)

1 = Enables the WDT if it is not enabled by the device configuration
0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit

1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit

1 = Writing a '1' will clear the WDT
0 = Software cannot force this bit to a '0'

- Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
2: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

17.0 OUTPUT COMPARE

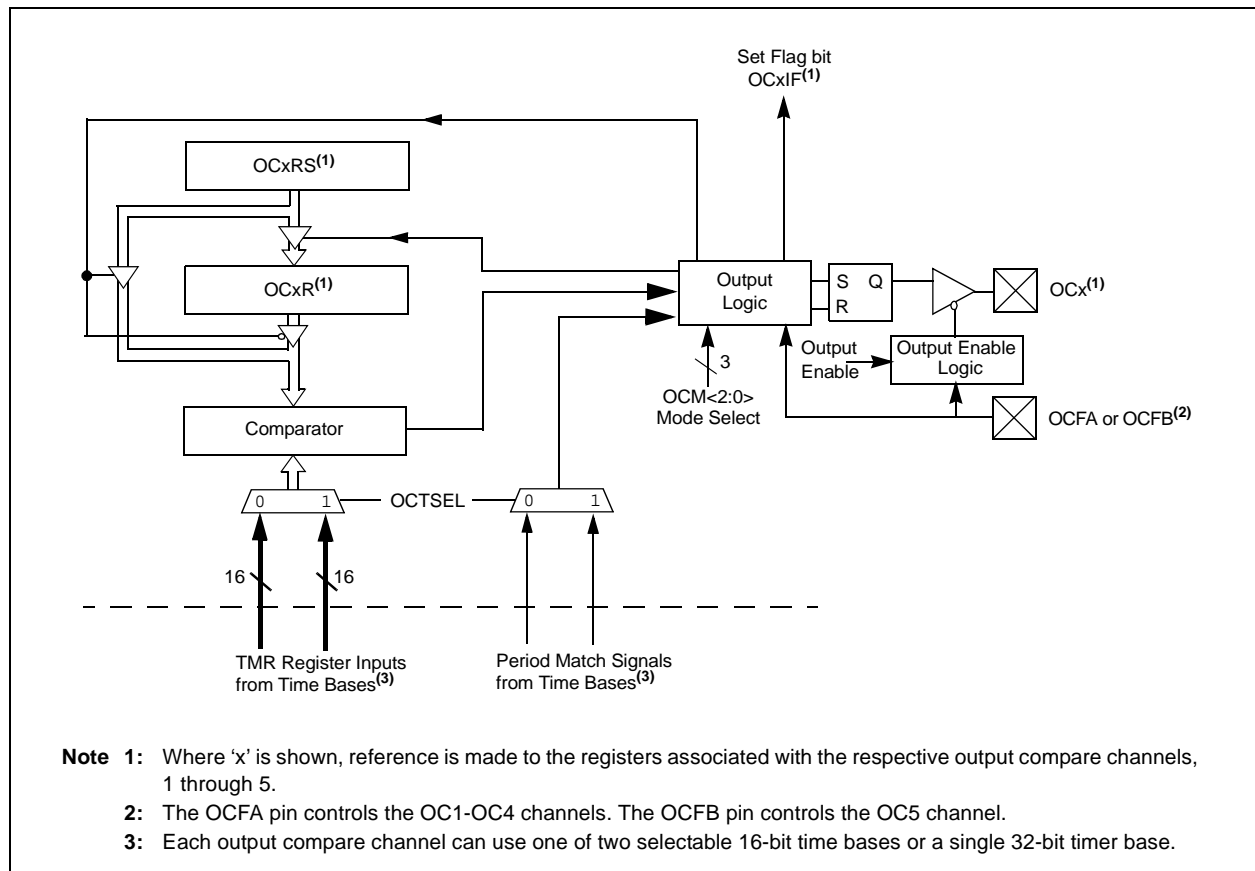
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. “Output Compare”** (DS60001111) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Output Compare module is used to generate a single pulse or a series of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

FIGURE 17-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



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REGISTER 19-2: I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
This bit is cleared by hardware upon a device address match, and is set by hardware by reception of the slave byte.
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
- bit 4 **P:** Stop bit
This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected.
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
- bit 3 **S:** Start bit
This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected.
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
- bit 2 **R_W:** Read/Write Information bit (when operating as I²C slave)
This bit is set or cleared by hardware after reception of an I²C device address byte.
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
- bit 1 **RBF:** Receive Buffer Full Status bit
This bit is set by hardware when the I2CxRCV register is written with a received byte, and is cleared by hardware when software reads I2CxRCV.
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
- bit 0 **TBF:** Transmit Buffer Full Status bit
This bit is set by hardware when software writes to the I2CxTRN register, and is cleared by hardware upon completion of data transmission.
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty

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REGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ADRC	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
ADCS<7:0> ⁽²⁾								

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit

1 = Clock derived from FRC

0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits⁽¹⁾

11111 = 31 TAD

•
•
•

00001 = 1 TAD

00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits⁽²⁾

11111111 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 512 \cdot TPB = TAD$

•
•
•

00000001 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 4 \cdot TPB = TAD$

00000000 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 2 \cdot TPB = TAD$

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.

Note 2: This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

REGISTER 24-9: CiRXMn: CAN ACCEPTANCE FILTER MASK 'n' REGISTER (n = 0, 1, 2 OR 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SID<10:3>							
23:16	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SID<2:0>			—	MIDE	—	EID<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-21 **SID<10:0>**: Standard Identifier bits

- 1 = Include the SIDx bit in filter comparison
- 0 = The SIDx bit is a 'don't care' in filter operation

bit 20 **Unimplemented**: Read as '0'

bit 19 **MIDE**: Identifier Receive Mode bit

- 1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
- 0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented**: Read as '0'

bit 17-0 **EID<17:0>**: Extended Identifier bits

- 1 = Include the EIDx bit in filter comparison
- 0 = The EIDx bit is a 'don't care' in filter operation

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

REGISTER 25-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<7:0>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-24 **PMM<31:24>**: Pattern Match Mask 3 bits
bit 23-16 **PMM<23:16>**: Pattern Match Mask 2 bits
bit 15-8 **PMM<15:8>**: Pattern Match Mask 1 bits
bit 7-0 **PMM<7:0>**: Pattern Match Mask 0 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 25-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<39:32>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-24 **PMM<63:56>**: Pattern Match Mask 7 bits
bit 23-16 **PMM<55:48>**: Pattern Match Mask 6 bits
bit 15-8 **PMM<47:40>**: Pattern Match Mask 5 bits
bit 7-0 **PMM<39:32>**: Pattern Match Mask 4 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

29.2 On-Chip Voltage Regulator

All PIC32MX5XX/6XX/7XX devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX-5XX/6XX/7XX family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 29-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 32.1 "DC Characteristics"**.

Note: It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

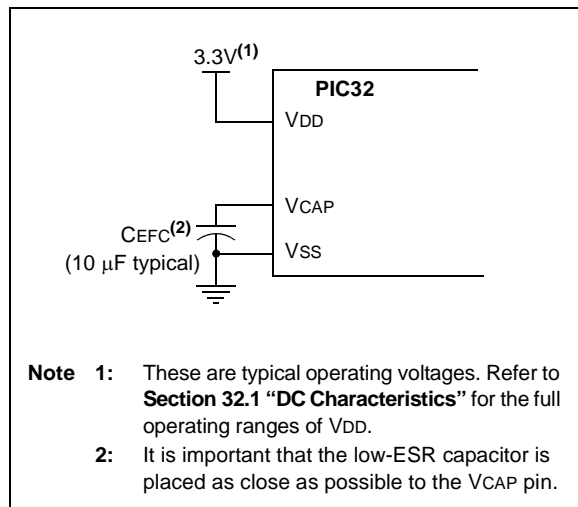
29.2.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

29.2.2 ON-CHIP REGULATOR AND BOR

PIC32MX5XX/6XX/7XX devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset (BOR). This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specified in **Section 32.1 "DC Characteristics"**.

FIGURE 29-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



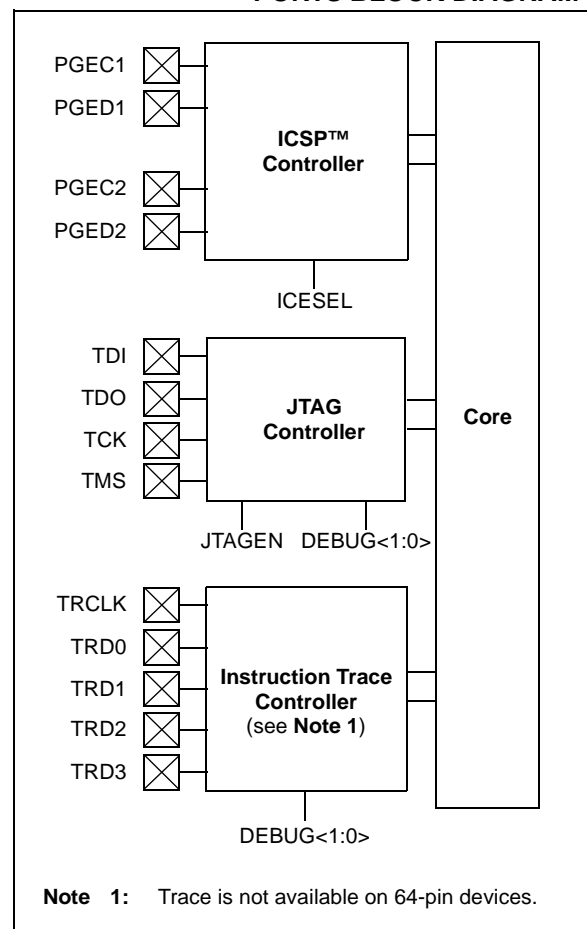
29.3 Programming and Diagnostics

PIC32MX5XX/6XX/7XX devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 29-2: PROGRAMMING, DEBUGGING, AND TRACE PORTS BLOCK DIAGRAM



32.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX5XX/6XX/7XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX5XX/6XX/7XX devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias.....	-40°C to +105°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3).....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V (Note 3).....	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V (Note 3).....	-0.3V to +3.6V
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin(s)	300 mA
Maximum current into VDD pin(s) (Note 2).....	300 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2).....	200 mA

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

3: See the “**Device Pin Tables**” section for the 5V tolerant pins.

TABLE 32-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
DI50	IIL	Input Leakage Current ⁽³⁾ I/O Ports	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		MCLR ⁽²⁾	—	—	±1	μA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, XT and HS modes
DI60a	IICL	Input Low Injection Current	0	—	-5 ^(7,10)	mA	This parameter applies to all pins, with the exception of RB10. Maximum IICL current for this exception is 0 mA.
DI60b	IICH	Input High Injection Current	0	—	+5 ^(8,9,10)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, SOSC1, and RB10. Maximum IICH current for these exceptions is 0 mA.
DI60c	ΣIIC	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽¹¹⁾	—	+20 ⁽¹¹⁾	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (IICL + IICH) ≤ ΣIIC

- Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** This parameter is characterized, but not tested in manufacturing.
- 5:** See the “**Device Pin Tables**” section for the 5V-tolerant pins.
- 6:** The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic “high” internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.
- 7:** VIL source < (VSS - 0.3). Characterized but not tested.
- 8:** VIH source > (VDD + 0.3) for non-5V tolerant pins only.
- 9:** Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any “positive” input injection current.
- 10:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).
- 11:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**, IICL = (((VSS - 0.3) - VIL source) / RS). If **Note 8**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

PIC32MX5XX/6XX/7XX

FIGURE 32-28: EJTAG TIMING CHARACTERISTICS

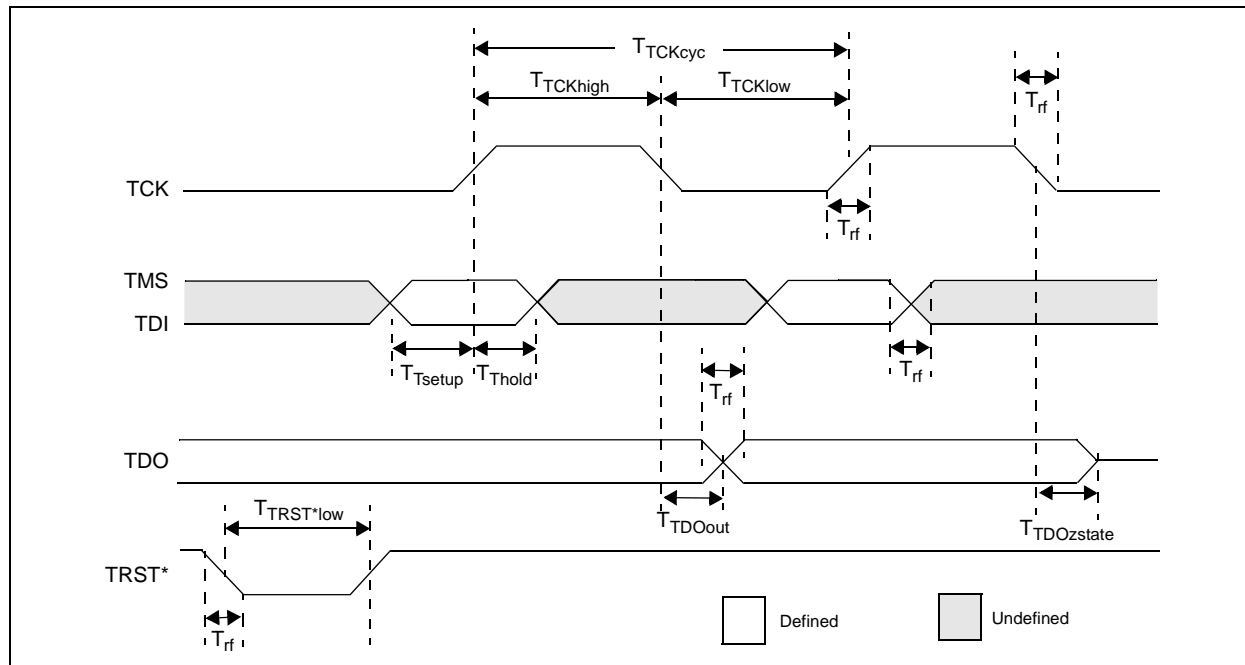


TABLE 32-43: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)		
				Operating temperature -40°C ≤ Ta ≤ +85°C for Industrial -40°C ≤ Ta ≤ +105°C for V-Temp		
Param. No.	Symbol	Description ⁽¹⁾	Min.	Max.	Units	Conditions
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

Revision D (May 2010)

The revision includes the following updates, as described in Table B-3:

TABLE B-3: MAJOR SECTION UPDATES

Section Name	Update Description
“High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers”	<p>Updated the initial Flash memory range to 64K.</p> <p>Updated the initial SRAM memory range to 16K.</p> <p>Added the following devices (see Table 1, Table 2, Table 3 and the Pin Diagrams):</p> <ul style="list-style-type: none">• PIC32MX534F064H• PIC32MX564F064H• PIC32MX664F064H• PIC32MX564F128H• PIC32MX664F128H• PIC32MX764F128H• PIC32MX534F064L• PIC32MX564F064L• PIC32MX664F064L• PIC32MX564F128L• PIC32MX664F128L• PIC32MX764F128L
4.0 “Memory Organization”	<p>Added new Memory Maps (Figure 4-1, Figure 4-2 and Figure 4-3).</p> <p>The bit named I2CSIF was changed to I2C1SIF and the bit named I2CBIF was changed to I2C1BIF in the Interrupt Register Map tables (Table 4-2, Table 4-3, Table 4-4, Table 4-5, Table 4-6 and Table 4-7)</p> <p>Added the following devices to the Interrupt Register Map (Table 4-2):</p> <ul style="list-style-type: none">• PIC32MX534F064H• PIC32MX564F064H• PIC32MX564F128H <p>Added the following devices to the Interrupt Register Map (Table 4-3):</p> <ul style="list-style-type: none">• PIC32MX664F064H• PIC32MX664F128H <p>Added the following device to the Interrupt Register Map (Table 4-4):</p> <ul style="list-style-type: none">• PIC32MX764F128H <p>Added the following devices to the Interrupt Register Map (Table 4-5):</p> <ul style="list-style-type: none">• PIC32MX534F064L• PIC32MX564F064L• PIC32MX564F128L <p>Added the following devices to the Interrupt Register Map (Table 4-6):</p> <ul style="list-style-type: none">• PIC32MX664F064L• PIC32MX664F128L <p>Added the following device to the Interrupt Register Map (Table 4-7):</p> <ul style="list-style-type: none">• PIC32MX764F128L

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