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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

# Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	•
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f256h-80v-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# **Referenced Sources**

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

- Note 1: To access the documents listed below, browse to the documentation section of the PIC32MX795F512L product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list. In addition to parameters, features, and other documentation, the resulting page provides links to the related family
- Section 1. "Introduction" (DS60001127)
- Section 2. "CPU" (DS60001113)
- Section 4. "Prefetch Cache" (DS60001119)
- Section 3. "Memory Organization" (DS60001115)

reference manual sections.

- Section 5. "Flash Program Memory" (DS60001121)
- Section 6. "Oscillator Configuration" (DS60001112)
- Section 7. "Resets" (DS60001118)
- Section 8. "Interrupt Controller" (DS60001108)
- Section 9. "Watchdog Timer and Power-up Timer (DS60001114)
- Section 10. "Power-Saving Features" (DS60001130)
- Section 12. "I/O Ports" (DS60001120)
- Section 13. "Parallel Master Port (PMP)" (DS60001128)
- Section 14. "Timers" (DS60001105)
- Section 15. "Input Capture" (DS60001122)
- Section 16. "Output Capture" (DS60001111)
- Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104)
- Section 19. "Comparator" (DS60001110)
- Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109)
- Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107)
- Section 23. "Serial Peripheral Interface (SPI)" (DS60001106)
- Section 24. "Inter-Integrated Circuit (I2C)" (DS60001116)
- Section 27. "USB On-The-Go (OTG)" (DS60001126)
- Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125)
- Section 31. "Direct Memory Access (DMA) Controller" (DS60001117)
- Section 32. "Configuration" (DS60001124)
- Section 33. "Programming and Diagnostics" (DS60001129)
- Section 34. "Controller Area Network (CAN)" (DS60001154)
- Section 35. "Ethernet Controller" (DS60001155)

# FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX564F128H, PIC32MX564F128L, PIC32MX664F128H, PIC32MX664F128L, PIC32MX764F128H AND PIC32MX764F128L DEVICES



(DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—		—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—		—	—	
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	
15:8	BMXDKPBA<15:8>								
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
7:0				BMXDK	PBA<7:0>				

# REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

# Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** DRM Kernel Program Base Address Read-Only bits Value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

		<u>г</u>		V092L2															-
ess										В	its								s
Virtual Addr (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
1000	INTCON	31:16	—	—	—	—	—	—	—		—	—	—	_	_	—	—	SS0	0000
		15:0	_	_	_	MVEC	_		TPC<2:0>		_	_	_	INT4EP	INT3EP	INT2EP	INT1EP	INTOEP	0000
1010	INTSTAT <sup>(3)</sup>	15.0	_	_		_	_	_			_		_	—		<5:0>	_	_	0000
1020	IPTMR	31:16 15:0							01111 2 12:05	IPTMR	<31:0>					10.07			0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF SPI3TXIF I2C3MIF	U1RXIF SPI3RXIF I2C3SIF	U1EIF SPI3EIF I2C3BIF	SPI1TXIF	SPI1RXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
		31:16	IC3EIF	IC2EIF	IC1EIF	ETHIF	—	—	USBIF	FCEIF	DMA7IF <sup>(2)</sup>	DMA6IF <sup>(2)</sup>	DMA5IF <sup>(2)</sup>	DMA4IF <sup>(2)</sup>	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
1040	IFS1	15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF SPI4TXIF	U2RXIF SPI4RXIF	U2EIF SPI4EIF	U3TXIF SPI2TXIF	U3RXIF SPI2RXIF	U3EIF SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
		04.40						I2C5MIF	12C5SIF	I2C5BIF	I2C4MIF	I2C4SIF	I2C4BIF						
1050	IFS2	31:16			_														0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE SPI3TXIE I2C3MIE	U1RXIE SPI3RXIE I2C3SIE	U1EIE SPI3EIE I2C3BIE	SPI1TXIE	SPI1RXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
		31:16	IC3EIE	IC2EIE	IC1EIE	ETHIE	—	—	USBIE	FCEIE	DMA7IE <sup>(2)</sup>	DMA6IE <sup>(2)</sup>	DMA5IE <sup>(2)</sup>	DMA4IE <sup>(2)</sup>	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
1070	IEC1	15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE SPI4TXIE I2C5MIE	U2RXIE SPI4RXIE I2C5SIE	U2EIE SPI4EIE I2C5BIE	U3TXIE SPI2TXIE I2C4MIE	U3RXIE SPI2RXIE I2C4SIE	U3EIE SPI2EIE I2C4BIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
4000	15.00	31:16	—	_	_	_	—	—	—	_	_	_	_	_		_	_	_	0000
1080	IEC2	15:0	—	_	_	—	U5TXIE	U5RXIE	U5EIE	U6TXIE	U6RXIE	U6EIE	U4TXIE	U4RXIE	U4EIE	PMPEIE	IC5EIE	IC4EIE	0000
1090	IPC0	31:16	—	—	—		INT0IP<2:0>	•	INTOIS	S<1:0>	—	—	—		CS1IP<2:0>	•	CS1IS	S<1:0>	0000
		15:0		_	_		CS0IP<2:0>		CSOIS	S<1:0>	_				CTIP<2:0>		CTIS	<1:0>	0000
10A0	IPC1	31:16 15:0					IC1IP<2:0>	•	INT 11: IC1IS	5<1:0> i<1:0>					T1IP<2:0>	>	T1IS	<1:0> <1:0>	0000
	10.00	31:16	_	_	_		INT2IP<2:0>	•	INT2IS	S<1:0>	_	_	_		OC2IP<2:0>	•	OC2IS	6<1:0>	0000
1080	IPC2	15:0	—	_	_		IC2IP<2:0>		IC2IS	<1:0>	_	_	_		T2IP<2:0>		T2IS	<1:0>	0000
1000	IPC3	31:16	—	—	—		INT3IP<2:0>	•	INT3IS	S<1:0>	—	-	—		OC3IP<2:0>	<b>`</b>	OC3I	S<1:0>	0000
1000	15.03	15:0	_	_	_		IC3IP<2:0>		IC3IS	<1:0>	—	—	—		T3IP<2:0>		T3IS	<1:0>	0000
Legend	end: y = unknown value on Reset: — = unimplemented read as '0'. Reset values are shown in hexadecimal																		

### **TABLE 7-6:** INTERRUPT REGISTER MAP FOR PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L AND

0'. Reset values are shown in hexadecimal

Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Note 1: Registers" for more information.

These bits are not available on PIC32MX664 devices. 2:

This register does note have associated CLR, SET, and INV registers. 3:

# REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 18-16 PLLMULT<2:0>: Phase-Locked Loop (PLL) Multiplier bits

- 111 = Clock is multiplied by 24
- 110 = Clock is multiplied by 21
- 101 = Clock is multiplied by 20
- 100 = Clock is multiplied by 19
- 011 = Clock is multiplied by 18
- 010 =Clock is multiplied by 17
- 001 =Clock is multiplied by 16
- 000 =Clock is multiplied by 15
- bit 15 Unimplemented: Read as '0'
- bit 14-12 COSC<2:0>: Current Oscillator Selection bits
  - 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
  - 110 = Internal Fast RC (FRC) Oscillator divided by 16
  - 101 = Internal Low-Power RC (LPRC) Oscillator
  - 100 = Secondary Oscillator (Sosc)
  - 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
  - 010 = Primary Oscillator (Posc) (XT, HS or EC)
  - 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
  - 000 = Internal Fast RC (FRC) Oscillator
- bit 11 Unimplemented: Read as '0'
- bit 10-8 NOSC<2:0>: New Oscillator Selection bits
  - 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
  - 110 = Internal Fast RC Oscillator (FRC) divided by 16
  - 101 = Internal Low-Power RC (LPRC) Oscillator
  - 100 = Secondary Oscillator (Sosc)
  - 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
  - 010 = Primary Oscillator (XT, HS or EC)
  - 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
  - 000 = Internal Fast Internal RC Oscillator (FRC)
  - On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).
- bit 7 CLKLOCK: Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):

- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):

Clock and PLL selections are never locked and may be modified.

- bit 6 ULOCK: USB PLL Lock Status bit
  - 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
  - 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled
- bit 5 SLOCK: PLL Lock Status bit
  - 1 = PLL module is in lock or PLL module start-up timer is satisfied
  - 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

### bit 4 SLPEN: Sleep Mode Enable bit

- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed
- bit 3 **CF:** Clock Fail Detect bit
  - 1 = FSCM has detected a clock failure
  - 0 = No clock failure has been detected

Note: Writes to this register require an unlock sequence. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
23:16	—	—	—	—	—	-	—	CHECOH
15.0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
10.0	—	—	—	—	—		DCSZ	<b>ː&lt;</b> 1:0>
7.0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
7:0	—	—	PREFE	N<1:0>	—	PFMWS<2:0>		

# REGISTER 9-1: CHECON: CACHE CONTROL REGISTER

## Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-17 Unimplemented: Write '0'; ignore read

- bit 16 CHECOH: Cache Coherency Setting on a PFM Program Cycle bit
  - 1 = Invalidate all data and instruction lines
  - 0 = Invalidate all data lnes and instruction lines that are not locked
- bit 15-10 Unimplemented: Write '0'; ignore read
- bit 9-8 DCSZ<1:0>: Data Cache Size in Lines bits
  - Changing these bits causes all lines to be reinitialized to the "invalid" state.
    - 11 = Enable data caching with a size of 4 lines
    - 10 = Enable data caching with a size of 2 lines
    - 01 = Enable data caching with a size of 1 line
    - 00 = Disable data caching
- bit 7-6 Unimplemented: Write '0'; ignore read
- bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits
  - 11 = Enable predictive prefetch for both cacheable and non-cacheable regions
  - 10 = Enable predictive prefetch only for non-cacheable regions
  - 01 = Enable predictive prefetch only for cacheable regions
  - 00 = Disable predictive prefetch
- bit 3 Unimplemented: Write '0'; ignore read

### bit 2-0 PFMWS<2:0>: PFM Access Time Defined in Terms of SYSLK Wait States bits

- 111 = Seven Wait states
- 110 = Six Wait states
- 101 = Five Wait states
- 100 = Four Wait states
- 011 = Three Wait states
- 010 = Two Wait states
- 001 = One Wait state
- 000 = Zero Wait state

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	LTAGBOOT	—	—	—	—	-	—	—	
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23.10	LTAG<19:12>								
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15.0	LTAG<11:4>								
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-0	R/W-0	R/W-1	U-0	
		LTAG-	<3:0>		LVALID	LLOCK	LTYPE	—	

# REGISTER 9-3: CHETAG: CACHE TAG REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## bit 31 LTAGBOOT: Line Tag Address Boot bit

- 1 = The line is in the 0x1D000000 (physical) area of memory
- 0 = The line is in the 0x1FC00000 (physical) area of memory

## bit 30-24 Unimplemented: Write '0'; ignore read

## bit 23-4 LTAG<19:0>: Line Tag Address bits

LTAG<19:0> bits are compared against physical address to determine a hit. Because its address range and position of PFM in kernel space and user space, the LTAG PFM address is identical for virtual addresses, (system) physical addresses, and PFM physical addresses.

### bit 3 LVALID: Line Valid bit

- 1 = The line is valid and is compared to the physical address for hit detection
- 0 = The line is not valid and is not compared to the physical address for hit detection

# bit 2 LLOCK: Line Lock bit

- 1 = The line is locked and will not be replaced
- 0 = The line is not locked and can be replaced

# bit 1 LTYPE: Line Type bit

- 1 = The line caches instruction words
- 0 = The line caches data words
- bit 0 Unimplemented: Write '0'; ignore read

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	-	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10		—	—	—	—	—	—	—	
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
10.0	LMASK<10:3>								
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
		LMASK<2:0>		—		—			

# REGISTER 9-4: CHEMSK: CACHE TAG MASK REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Write '0'; ignore read

## bit 15-5 LMASK<10:0>: Line Mask bits

- 1 = Enables mask logic to force a match on the corresponding bit position in LTAG<19:0> bits (CHETAG<23:4>) and the physical address
- 0 = Only writeable for values of CHEIDX<3:0> bits (CHEACC<3:0>) equal to 0x0A and 0x0B (disables mask logic)
- bit 4-0 **Unimplemented:** Write '0'; ignore read

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31.24	CHEW0<31:24>								
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23.10	CHEW0<23:16>								
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15.6	CHEW0<15:8>								
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
7.0				CHEWO	<7:0>				

# REGISTER 9-5: CHEW0: CACHE WORD 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW0<31:0>:** Word 0 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0						
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0						
23.10	—	—	—	—	_	_	—	
15.0	U-0	U-0						
15.6	_	_	_					
	R/W-0	R/W-0						
7:0	BTSEE	BMXEE		BTOFF		CRC16EE	CRC5EE <sup>(1)</sup>	PIDEE
	DIGLE	DIVIALL		DIOLL	DINOLL	GROTOLL	EOFEE <sup>(2)</sup>	TIDEE

# REGISTER 11-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8	Unimplemented: Read as '0'
bit 7	BTSEE: Bit Stuff Error Interrupt Enable bit
	<ul><li>1 = BTSEF interrupt is enabled</li><li>0 = BTSEF interrupt is disabled</li></ul>
bit 6	BMXEE: Bus Matrix Error Interrupt Enable bit
	<ul><li>1 = BMXEF interrupt is enabled</li><li>0 = BMXEF interrupt is disabled</li></ul>
bit 5	DMAEE: DMA Error Interrupt Enable bit
	<ul><li>1 = DMAEF interrupt is enabled</li><li>0 = DMAEF interrupt is disabled</li></ul>
bit 4	BTOEE: Bus Turnaround Time-out Error Interrupt Enable bit
	1 = BTOEF interrupt is enabled

- 0 = BTOEF interrupt is disabled
- bit 3 DFN8EE: Data Field Size Error Interrupt Enable bit
  - 1 = DFN8EF interrupt is enabled
  - 0 = DFN8EF interrupt is disabled
- bit 2 CRC16EE: CRC16 Failure Interrupt Enable bit
  - 1 = CRC16EF interrupt is enabled
  - 0 = CRC16EF interrupt is disabled
- CRC5EE: CRC5 Host Error Interrupt Enable bit<sup>(1)</sup> bit 1
  - 1 = CRC5EF interrupt is enabled
  - 0 = CRC5EF interrupt is disabled
  - EOFEE: EOF Error Interrupt Enable bit<sup>(2)</sup>
  - 1 = EOF interrupt is enabled
  - 0 = EOF interrupt is disabled
- bit 0 PIDEE: PID Check Failure Interrupt Enable bit
  - 1 = PIDEF interrupt is enabled
  - 0 = PIDEF interrupt is disabled
- Note 1: Device mode.
  - 2: Host mode.

Note: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

# 14.0 TIMER2/3, TIMER4/5

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a freerunning interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-bit Timer
- Synchronous Internal 16-bit Gated Timer
- Synchronous External 16-bit Timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

- Synchronous Internal 32-bit Timer
- · Synchronous Internal 32-bit Gated Timer
- Synchronous External 32-bit Timer
- Note: In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through Timer5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or Timer4; 'y' represents Timer3 or Timer5.

# 14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (only Timer2 and Timer3)
- ADC event trigger (only Timer3)
- Fast bit manipulation using CLR, SET and INV registers

# FIGURE 14-1: TIMER2/3 AND TIMER4/5 BLOCK DIAGRAM (16-BIT)



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0			
31:24	—	—	—		RXBUFELM<4:0>						
00.40	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0			
23:16	—	—	—	TXBUFELM<4:0>							
45.0	U-0	U-0	U-0	U-0	R-0	U-0	U-0	R-0			
15:8	—	—	—	—	SPIBUSY	—	—	SPITUR			
7.0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0			
7:0	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF			

# **REGISTER 18-2: SPIxSTAT: SPI STATUS REGISTER**

Legend:	C = Clearable bit	HS = Set in hardware			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

- bit 31-29 Unimplemented: Read as '0'
- bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (only valid when ENHBUF = 1)
- bit 23-21 Unimplemented: Read as '0'
- bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (only valid when ENHBUF = 1)
- bit 15-12 Unimplemented: Read as '0'
- bit 11 SPIBUSY: SPI Activity Status bit 1 = SPI peripheral is currently busy with some transactions 0 = SPI peripheral is currently idle
  - Unimplemented: Read as '0'
- bit 10-9
- bit 8 SPITUR: Transmit Under Run bit
  - 1 = Transmit buffer has encountered an underrun condition
  - 0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

- bit 7 **SRMT:** Shift Register Empty bit (only valid when ENHBUF = 1)
  - 1 = When SPI module shift register is empty
  - 0 = When SPI module shift register is not empty
- bit 6 SPIROV: Receive Overflow Flag bit
  - 1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
  - 0 = No overflow has occurred
  - This bit is set in hardware; can only be cleared (= 0) in software.
- bit 5 **SPIRBE:** RX FIFO Empty bit (only valid when ENHBUF = 1) 1 = RX FIFO is empty (CRPTR = SWPTR) 0 = RX FIFO is not empty (CRPTR  $\neq$  SWPTR)
- bit 4 Unimplemented: Read as '0'
- bit 3 SPITBE: SPI Transmit Buffer Empty Status bit
  - 1 = Transmit buffer, SPIxTXB is empty
  - 0 = Transmit buffer, SPIxTXB is not empty
  - Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
  - Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.
- bit 2 Unimplemented: Read as '0'

### I2CxSTAT: I<sup>2</sup>C STATUS REGISTER (CONTINUED) REGISTER 19-2: **D\_A:** Data/Address bit (when operating as I<sup>2</sup>C slave) bit 5 This bit is cleared by hardware upon a device address match, and is set by hardware by reception of the slave byte. 1 = Indicates that the last byte received was data 0 = Indicates that the last byte received was device address bit 4 P: Stop bit This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected. 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last bit 3 S: Start bit This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected. 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last **R\_W:** Read/Write Information bit (when operating as I<sup>2</sup>C slave) bit 2 This bit is set or cleared by hardware after reception of an I<sup>2</sup>C device address byte. 1 = Read – indicates data transfer is output from slave 0 = Write - indicates data transfer is input to slave **RBF:** Receive Buffer Full Status bit bit 1 This bit is set by hardware when the I2CxRCV register is written with a received byte, and is cleared by hardware when software reads I2CxRCV. 1 = Receive complete, I2CxRCV is full 0 = Receive not complete, I2CxRCV is empty bit 0 TBF: Transmit Buffer Full Status bit This bit is set by hardware when software writes to the I2CxTRN register, and is cleared by hardware upon completion of data transmission.

1 = Transmit in progress, I2CxTRN is full

0 = Transmit complete, I2CxTRN is empty

# 21.1 Control Registers

# TABLE 21-1: PARALLEL MASTER PORT REGISTER MAP

ess										Bi	ts								
Virtual Addr (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
7000	PMCON	31:16	—	—	—	1	1	—	—	-		—	—	1	1	—	—	-	0000
7000	TIMOON	15:0	ON	—	SIDL	ADRMU	JX<1:0>	PMPTTL	PTWREN	PTRDEN	CSF	<1:0>	ALP	CS2P	CS1P	—	WRSP	RDSP	0000
7010		31:16	—	—	—	_	_	—	—	_	_	—	—	_	_	—	—	—	0000
7010	FININODE	15:0	BUSY	IRQM	<1:0>	INCM	<1:0>	MODE16	MODE	<1:0>	WAITE	3<1:0>		WAITN	//<3:0>		WAITI	E<1:0>	0000
7020		31:16	—	—	—	_	_	—	—	_	_	—	—	_	_	—	—	—	0000
1020		15:0	CS2EN/A15	CS1EN/A14							ADDR	<13:0>							0000
7020		31:16									IT -21.05								0000
7030	FINDOUT	15:0								DATAOL	1<31.0>								0000
7040		31:16								ΠΑΤΑΙΝ	1-31.05								0000
7040	FINDIN	15:0								DATAIN	1<31.0>								0000
7050		31:16	—	—	—	_	_	—	—	-	_	—	—	_	_	—	_	—	0000
7050	FINALIN	15:0								PTEN	<15:0>								0000
7060	DMOTAT	31:16	_	_	_	_	_		_	_	_	_	_	_	_	_	_	_	0000
1060	FIVISTAT	15:0	IBF	IBOV	_	-	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	_	-	OB3E	OB2E	OB1E	OB0E	008F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

NOTES:

REGISTER 23-2:	AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—			—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	_	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
15:8	VCFG<2:0>			OFFCAL	—	CSCNA	—	—
7:0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFS	—		SMP	l<3:0>		BUFM	ALTS

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

# bit 31-16 Unimplemented: Read as '0'

bit 15-13 VCFG<2:0>: Voltage Reference Configuration bits

Bit Value	VREFH	VREFL		
1xx	AVdd	AVss		
011	External VREF+ pin	External VREF- pin		
010	AVdd	External VREF- pin		
001	External VREF+ pin	AVss		
000	AVdd	AVss		

## bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the S&H circuit are connected to VREFL.

0 = Disable Offset Calibration mode

The inputs to the S&H circuit are controlled by AD1CHS or AD1CSSL.

# bit 11 Unimplemented: Read as '0'

- bit 10 **CSCNA:** Input Scan Select bit
  - 1 = Scan inputs

0 = Do not scan inputs

- bit 9-8 Unimplemented: Read as '0'
- bit 7 BUFS: Buffer Fill Status bit
  - Only valid when BUFM = 1.
    - 1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
    - 0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

# bit 6 Unimplemented: Read as '0'

# bit 5-2 SMPI<3:0>: Sample/Convert Sequences Per Interrupt Selection bits

- 1111 = Interrupts at the completion of conversion for each 16<sup>th</sup> sample/convert sequence 1110 = Interrupts at the completion of conversion for each 15<sup>th</sup> sample/convert sequence
- 1110 = Interrupts at the completion of conversion for each 15" sample/convert sequence
- •

0001 = Interrupts at the completion of conversion for each 2<sup>nd</sup> sample/convert sequence 0000 = Interrupts at the completion of conversion for each sample/convert sequence

- bit 1 BUFM: ADC Result Buffer Mode Select bit
  - 1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
  - 0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0
- bit 0 ALTS: Alternate Input Sample Mode Select bit
  - 1 = Uses Sample A input multiplexer settings for first sample, and then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
  - 0 = Always use Sample A input multiplexer settings

# **REGISTER 25-13: ETHIEN: ETHERNET CONTROLLER INTERRUPT ENABLE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	_		—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	_		—	—	—	—
15.0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	—	TXBUSEIE <sup>(1)</sup>	RXBUSEIE <sup>(2)</sup>	_	—	—	EWMARKIE <sup>(2)</sup>	FWMARKIE <sup>(2)</sup>
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	RXDONEIE <sup>(2)</sup>	PKTPENDIE <sup>(2)</sup>	RXACTIE <sup>(2)</sup>		TXDONEIE <sup>(1)</sup>	TXABORTIE <sup>(1)</sup>	RXBUFNAIE <sup>(2)</sup>	RXOVFLWIE <sup>(2)</sup>

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-15 Unimplemented: Read as '0'

- bit 14 **TXBUSEIE:** Transmit BVCI Bus Error Interrupt Enable bit<sup>(1)</sup>
  - 1 = Enable TXBUS Error Interrupt
  - 0 = Disable TXBUS Error Interrupt
- bit 13 **RXBUSEIE:** Receive BVCI Bus Error Interrupt Enable bit<sup>(2)</sup>
  - 1 = Enable RXBUS Error Interrupt 0 = Disable RXBUS Error Interrupt
  - 0 = Disable RABUS Erfor Interrup
- bit 12-10 Unimplemented: Read as '0'

bit 9	<b>EWMARKIE:</b> Empty Watermark Interrupt Enable bit <sup>(2)</sup> 1 = Enable EWMARK Interrupt
	0 = Disable EWMARK Interrupt
bit 8	FWMARKIE: Full Watermark Interrupt Enable bit <sup>(2)</sup>
	1 = Enable FWMARK Interrupt
	0 = Disable FWMARK Interrupt
bit 7	<b>RXDONEIE:</b> Receiver Done Interrupt Enable bit <sup>(2)</sup>
	1 = Enable RXDONE Interrupt
	0 = Disable RXDONE Interrupt
bit 6	PKTPENDIE: Packet Pending Interrupt Enable bit <sup>(2)</sup>
	1 = Enable PKTPEND Interrupt
	0 = Disable PKTPEND Interrupt
bit 5	<b>RXACTIE:</b> RX Activity Interrupt Enable bit
	1 = Enable RXACT Interrupt
	0 = Disable RXACT Interrupt
bit 4	Unimplemented: Read as '0'
bit 3	TXDONEIE: Transmitter Done Interrupt Enable bit <sup>(1)</sup>
	1 = Enable TXDONE Interrupt
	0 = Disable TXDONE Interrupt
bit 2	TXABORTIE: Transmitter Abort Interrupt Enable bit <sup>(1)</sup>
	1 = Enable TXABORT Interrupt
	0 = Disable TXABORT Interrupt
bit 1	<b>RXBUFNAIE:</b> Receive Buffer Not Available Interrupt Enable bit <sup>(2)</sup>
	1 = Enable RXBUFNA Interrupt
	0 = Disable RXBUFNA Interrupt
bit 0	<b>RXOVFLWIE:</b> Receive FIFO Overflow Interrupt Enable bit <sup>(2)</sup>
	1 = Enable RXOVFLW Interrupt
	0 = Disable RXOVELW Interrupt

- **Note 1:** This bit is only used for TX operations.
  - **2:** This bit is only used for RX operations.

# REGISTER 25-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 25/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	-	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	-	—	—	—	—
15:8	U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	EXCESS DFR	BPNOBK OFF	NOBK OFF	—	—	LONGPRE	PUREPRE
7:0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	AUTO PAD <sup>(1,2)</sup>	VLAN PAD <sup>(1,2)</sup>	PAD ENABLE <sup>(1,3)</sup>	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 Unimplemented: Read as '0'

bit 14 **EXCESSDER:** Excess Defer bit

1 = The MAC will defer to carrier indefinitely as per the Standard

0 = The MAC will abort when the excessive deferral limit is reached

### bit 13 **BPNOBKOFF:** Backpressure/No Backoff bit

- 1 = The MAC after incidentally causing a collision during backpressure will immediately retransmit without backoff reducing the chance of further collisions and ensuring transmit packets get sent
- 0 = The MAC will not remove the backoff

### bit 12 NOBKOFF: No Backoff bit

- 1 = Following a collision, the MAC will immediately retransmit rather than using the Binary Exponential Backoff algorithm as specified in the Standard
- 0 = Following a collision, the MAC will use the Binary Exponential Backoff algorithm

### bit 11-10 Unimplemented: Read as '0'

- bit 9 LONGPRE: Long Preamble Enforcement bit
  - 1 = The MAC only allows receive packets which contain preamble fields less than 12 bytes in length
  - 0 = The MAC allows any length preamble as per the Standard

### bit 8 **PUREPRE:** Pure Preamble Enforcement bit

- 1 = The MAC will verify the content of the preamble to ensure it contains 0x55 and is error-free. A packet with errors in its preamble is discarded
- 0 = The MAC does not perform any preamble checking
- bit 7 AUTOPAD: Automatic Detect Pad Enable bit<sup>(1,2)</sup>
  - 1 = The MAC will automatically detect the type of frame, either tagged or untagged, by comparing the two octets following the source address with 0x8100 (VLAN Protocol ID) and pad accordingly
  - 0 = The MAC does not perform automatic detection

### Note 1: Table 25-6 provides a description of the pad function based on the configuration of this register.

- 2: This bit is ignored if the PADENABLE bit is cleared.
- 3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

# TABLE 32-31: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-Temp} \end{array}$					
Param. No.	Symbol	Characteristics <sup>(1)</sup>	eristics <sup>(1)</sup> Min. Typical <sup>(2)</sup> Max.				Conditions	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance <sup>(4)</sup>	5	—	25	ns	_	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	Тѕск + 20	_		ns	_	
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	_	_	25	ns		

**Note 1:** These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

# TABLE 32-37: 10-BIT ADC CONVERSION RATE PARAMETERS

Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-Temp								
ADC Speed <sup>(2)</sup>	TAD Minimum	Sampling Time Minimum	Rs Maximum	Vdd	ADC Channels Configuration			
1 Msps to 400 ksps <sup>(1)</sup>	65 ns	132 ns	500Ω	3.0V to 3.6V	ANX CHX ADC			
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	ANX CHX ANX OF VREF- ANX OF VREF-			

Note 1: External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.

**3:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	0.50 BSC			
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A