



Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f256h-80v-pt

Device Pin Tables

TABLE 4: PIN NAMES FOR 64-PIN USB AND CAN DEVICES

64-PIN QFN ⁽²⁾ AND TQFP (TOP VIEW)			
PIC32MX534F064H PIC32MX564F064H PIC32MX564F128H PIC32MX575F256H PIC32MX575F512H		64	1
		QFN ⁽²⁾	TQFP ¹
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PMD5/RE5	33	USBID/RF3
2	PMD6/RE6	34	V _{BUS}
3	PMD7/RE7	35	V _{USB3V3}
4	SCK2/U6TX/U3RTS/PMA5/CN8/RG6	36	D-/RG3
5	SDA4/SDI2/U3RX/PMA4/CN9/RG7	37	D+/RG2
6	SCL4/SDO2/U3TX/PMA3/CN10/RG8	38	V _{DD}
7	MCLR	39	OSC1/CLKI/RC12
8	SS2/U6RX/U3CTS/PMA2/CN11/RG9	40	OSC2/CLKO/RC15
9	V _{SS}	41	V _{SS}
10	V _{DD}	42	RTCC/IC1/INT1/RD8
11	AN5/C1IN+/V _{BUSON} /CN7/RB5	43	SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9
12	AN4/C1IN-/CN6/RB4	44	SCL1/IC3/PMCS2/PMA15/INT3/RD10
13	AN3/C2IN+/CN5/RB3	45	IC4/PMCS1/PMA14/INT4/RD11
14	AN2/C2IN-/CN4/RB2	46	OC1/INT0/RD0
15	PGEC1/AN1/VREF-/CVREF-/CN3/RB1	47	SOSCI/CN1/RC13
16	PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0	48	SOSCO/T1CK/CN0/RC14
17	PGEC2/AN6/OCFA/RB6	49	SCK3/U4TX/U1RTS/OC2/RD1
18	PGED2/AN7/RB7	50	SDA3/SDI3/U1RX/OC3/RD2
19	AV _{DD}	51	SCL3/SDO3/U1TX/OC4/RD3
20	AV _{SS}	52	OC5/IC5/PMWR/CN13/RD4
21	AN8/SS4/U5RX/U2CTS/C1OUT/RB8	53	PMRD/CN14/RD5
22	AN9/C2OUT/PMA7/RB9	54	CN15/RD6
23	TMS/AN10/CVREFOUT/PMA13/RB10	55	CN16/RD7
24	TDO/AN11/PMA12/RB11	56	V _{CAP}
25	V _{SS}	57	V _{DD}
26	V _{DD}	58	C1RX/RF0
27	TCK/AN12/PMA11/RB12	59	C1TX/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14	61	PMD1/RE1
30	AN15/OCFB/PMALL/PMA0/CN12/RB15	62	PMD2/RE2
31	AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4	63	PMD3/RE3
32	AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5	64	PMD4/RE4

Note 1: Shaded pins are 5V tolerant.

Note 2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to V_{SS} externally.

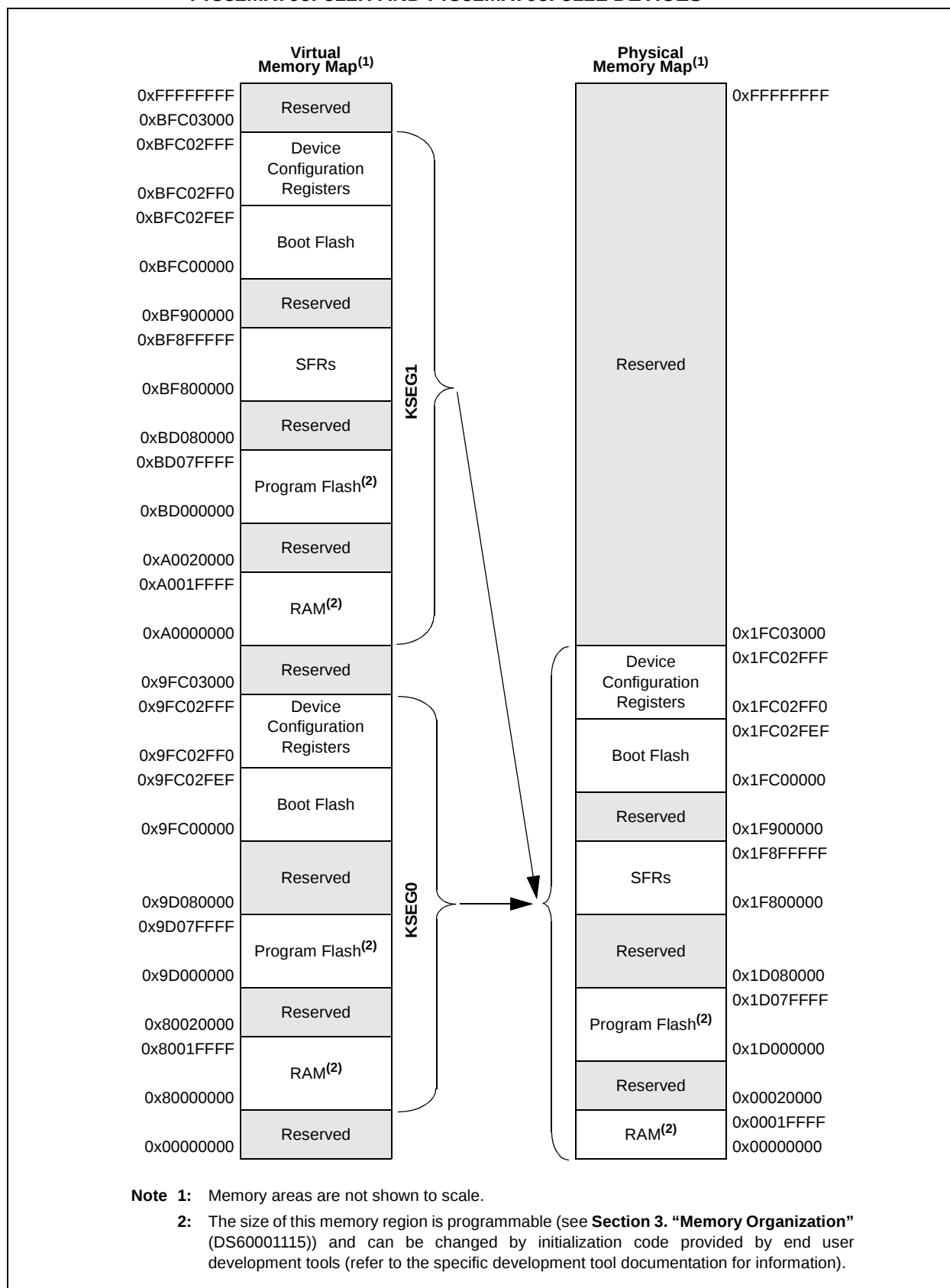
PIC32MX5XX/6XX/7XX

TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)

121-PIN TFBGA (BOTTOM VIEW)		L11	
PIC32MX664F064L PIC32MX664F128L PIC32MX675F256L PIC32MX675F512L PIC32MX695F512L		L1	A11
Note: The TFBGA package skips from row “H” to row “J” and has no “I” row.		A1	
Pin #	Full Pin Name	Pin #	Full Pin Name
J3	PGED2/AN7/RB7	K8	VDD
J4	AVDD	K9	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15
J5	AN11/ERXERR/AETXERR/PMA12/RB11	K10	USBID/RF3
J6	TCK/RA1	K11	SDA3/SDI3/U1RX/RF2
J7	AN12/ERXD0/AECRS/PMA11/RB12	L1	PGEC2/AN6/OCFA/RB6
J8	No Connect (NC)	L2	VREF-/CVREF-/AERXD2/PMA7/RA9
J9	No Connect (NC)	L3	AVss
J10	SCL3/SDO3/U1TX/RF8	L4	AN9/C2OUT/RB9
J11	D-/RG3	L5	AN10/CVREFOUT/PMA13/RB10
K1	PGEC1/AN1/CN3/RB1	L6	SCK4/U5TX/U2RTS/RF13
K2	PGED1/AN0/CN2/RB0	L7	AN13/ERXD1/AECOL/PMA10/RB13
K3	VREF+/CVREF+/AERXD3/PMA6/RA10	L8	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15
K4	AN8/C1OUT/RB8	L9	AETXD0/SS3/U4RX/U1CTS/CN20/RD14
K5	No Connect (NC)	L10	SDA5/SDI4/U2RX/PMA9/CN17/RF4
K6	SS4/U5RX/U2CTS/RF12	L11	SCL5/SDO4/U2TX/PMA8/CN18/RF5
K7	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14		

Note 1: Shaded pins are 5V tolerant.

FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX695F512H, PIC32MX695F512L, PIC32MX795F512H AND PIC32MX795F512L DEVICES



PIC32MX5XX/6XX/7XX

NOTES:

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	IRQ Number	Vector Number	Interrupt Bit Location			
			Flag	Enable	Priority	Sub-Priority
AD1 – ADC1 Convert Done	33	27	IFS1<1>	IEC1<1>	IPC6<28:26>	IPC6<25:24>
PMP – Parallel Master Port	34	28	IFS1<2>	IEC1<2>	IPC7<4:2>	IPC7<1:0>
CMP1 – Comparator Interrupt	35	29	IFS1<3>	IEC1<3>	IPC7<12:10>	IPC7<9:8>
CMP2 – Comparator Interrupt	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>
U2E – UART2 Error SPI2E – SPI2 Fault I2C4B – I2C4 Bus Collision Event	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>
U2RX – UART2 Receiver SPI2RX – SPI2 Receive Done I2C4S – I2C4 Slave Event	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>
U2TX – UART2 Transmitter SPI2TX – SPI2 Transfer Done IC4M – I2C4 Master Event	39	31	IFS1<7>	IEC1<7>	IPC7<28:26>	IPC7<25:24>
U3E – UART3 Error SPI4E – SPI4 Fault I2C5B – I2C5 Bus Collision Event	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>
U3RX – UART3 Receiver SPI4RX – SPI4 Receive Done I2C5S – I2C5 Slave Event	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>
U3TX – UART3 Transmitter SPI4TX – SPI4 Transfer Done IC5M – I2C5 Master Event	42	32	IFS1<10>	IEC1<10>	IPC8<4:2>	IPC8<1:0>
I2C2B – I2C2 Bus Collision Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>
I2C2S – I2C2 Slave Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>
I2C2M – I2C2 Master Event	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>
FSCM – Fail-Safe Clock Monitor	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>
RTCC – Real-Time Clock and Calendar	47	35	IFS1<15>	IEC1<15>	IPC8<28:26>	IPC8<25:24>
DMA0 – DMA Channel 0	48	36	IFS1<16>	IEC1<16>	IPC9<4:2>	IPC9<1:0>
DMA1 – DMA Channel 1	49	37	IFS1<17>	IEC1<17>	IPC9<12:10>	IPC9<9:8>
DMA2 – DMA Channel 2	50	38	IFS1<18>	IEC1<18>	IPC9<20:18>	IPC9<17:16>
DMA3 – DMA Channel 3	51	39	IFS1<19>	IEC1<19>	IPC9<28:26>	IPC9<25:24>
DMA4 – DMA Channel 4	52	40	IFS1<20>	IEC1<20>	IPC10<4:2>	IPC10<1:0>
DMA5 – DMA Channel 5	53	41	IFS1<21>	IEC1<21>	IPC10<12:10>	IPC10<9:8>
DMA6 – DMA Channel 6	54	42	IFS1<22>	IEC1<22>	IPC10<20:18>	IPC10<17:16>
DMA7 – DMA Channel 7	55	43	IFS1<23>	IEC1<23>	IPC10<28:26>	IPC10<25:24>
FCE – Flash Control Event	56	44	IFS1<24>	IEC1<24>	IPC11<4:2>	IPC11<1:0>
USB – USB Interrupt	57	45	IFS1<25>	IEC1<25>	IPC11<12:10>	IPC11<9:8>
CAN1 – Control Area Network 1	58	46	IFS1<26>	IEC1<26>	IPC11<20:18>	IPC11<17:16>
CAN2 – Control Area Network 2	59	47	IFS1<27>	IEC1<27>	IPC11<28:26>	IPC11<25:24>
ETH – Ethernet Interrupt	60	48	IFS1<28>	IEC1<28>	IPC12<4:2>	IPC12<1:0>
IC1E – Input Capture 1 Error	61	5	IFS1<29>	IEC1<29>	IPC1<12:10>	IPC1<9:8>
IC2E – Input Capture 2 Error	62	9	IFS1<30>	IEC1<30>	IPC2<12:10>	IPC2<9:8>

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX5XX USB and CAN Features”**, **TABLE 2: “PIC32MX6XX USB and Ethernet Features”** and **TABLE 3: “PIC32MX7XX USB, Ethernet, and CAN Features”** for the list of available peripherals.

PIC32MX5XX/6XX/7XX

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	IRQ Number	Vector Number	Interrupt Bit Location			
			Flag	Enable	Priority	Sub-Priority
IC3E – Input Capture 3 Error	63	13	IFS1<31>	IEC1<31>	IPC3<12:10>	IPC3<9:8>
IC4E – Input Capture 4 Error	64	17	IFS2<0>	IEC2<0>	IPC4<12:10>	IPC4<9:8>
IC5E – Input Capture 5 Error	65	21	IFS2<1>	IEC2<1>	IPC5<12:10>	IPC5<9:8>
PMPE – Parallel Master Port Error	66	28	IFS2<2>	IEC2<2>	IPC7<4:2>	IPC7<1:0>
U4E – UART4 Error	67	49	IFS2<3>	IEC2<3>	IPC12<12:10>	IPC12<9:8>
U4RX – UART4 Receiver	68	49	IFS2<4>	IEC2<4>	IPC12<12:10>	IPC12<9:8>
U4TX – UART4 Transmitter	69	49	IFS2<5>	IEC2<5>	IPC12<12:10>	IPC12<9:8>
U6E – UART6 Error	70	50	IFS2<6>	IEC2<6>	IPC12<20:18>	IPC12<17:16>
U6RX – UART6 Receiver	71	50	IFS2<7>	IEC2<7>	IPC12<20:18>	IPC12<17:16>
U6TX – UART6 Transmitter	72	50	IFS2<8>	IEC2<8>	IPC12<20:18>	IPC12<17:16>
U5E – UART5 Error	73	51	IFS2<9>	IEC2<9>	IPC12<28:26>	IPC12<25:24>
U5RX – UART5 Receiver	74	51	IFS2<10>	IEC2<10>	IPC12<28:26>	IPC12<25:24>
U5TX – UART5 Transmitter	75	51	IFS2<11>	IEC2<11>	IPC12<28:26>	IPC12<25:24>
(Reserved)	—	—	—	—	—	—
Lowest Natural Order Priority						

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX5XX USB and CAN Features”**, **TABLE 2: “PIC32MX6XX USB and Ethernet Features”** and **TABLE 3: “PIC32MX7XX USB, Ethernet, and CAN Features”** for the list of available peripherals.

17.0 OUTPUT COMPARE

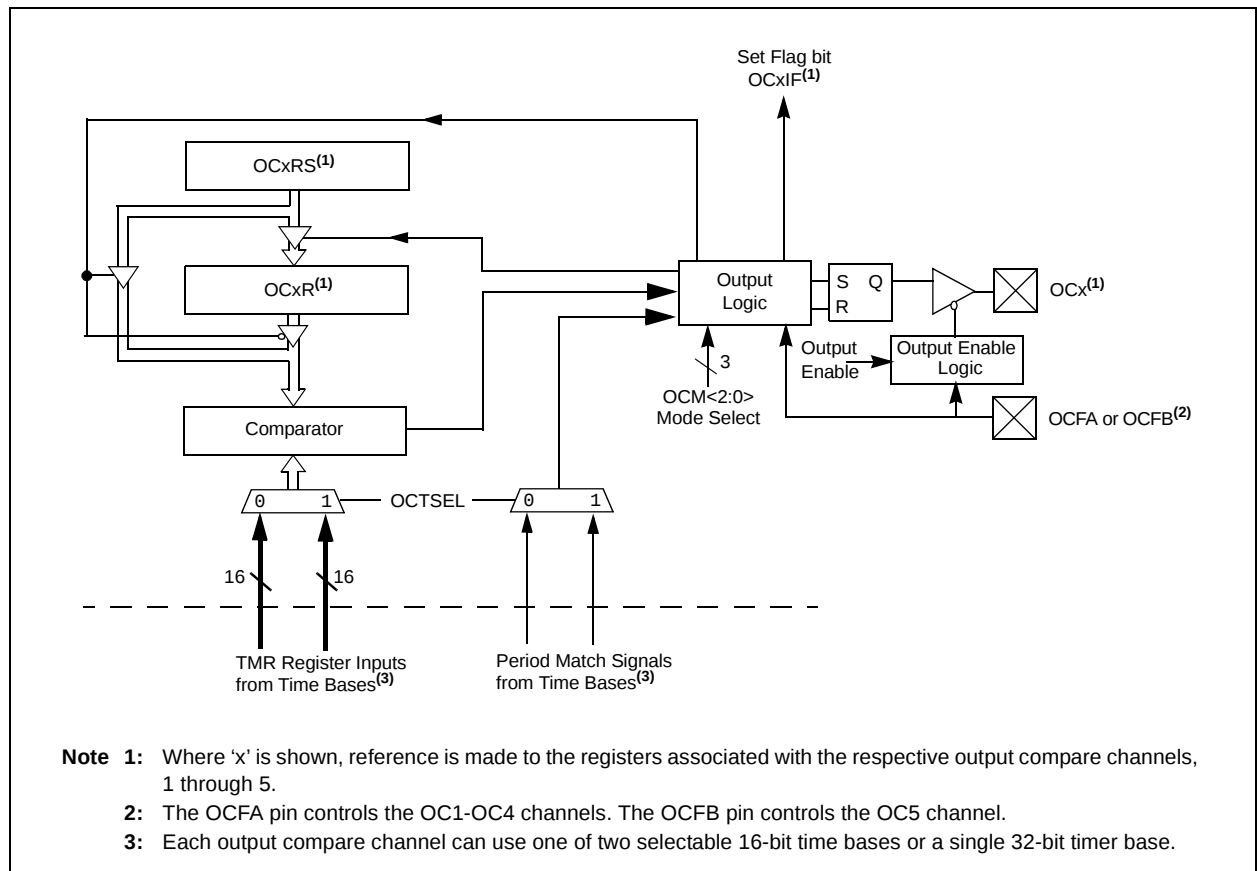
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. “Output Compare”** (DS60001111) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Output Compare module is used to generate a single pulse or a series of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

FIGURE 17-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



18.0 SERIAL PERIPHERAL INTERFACE (SPI)

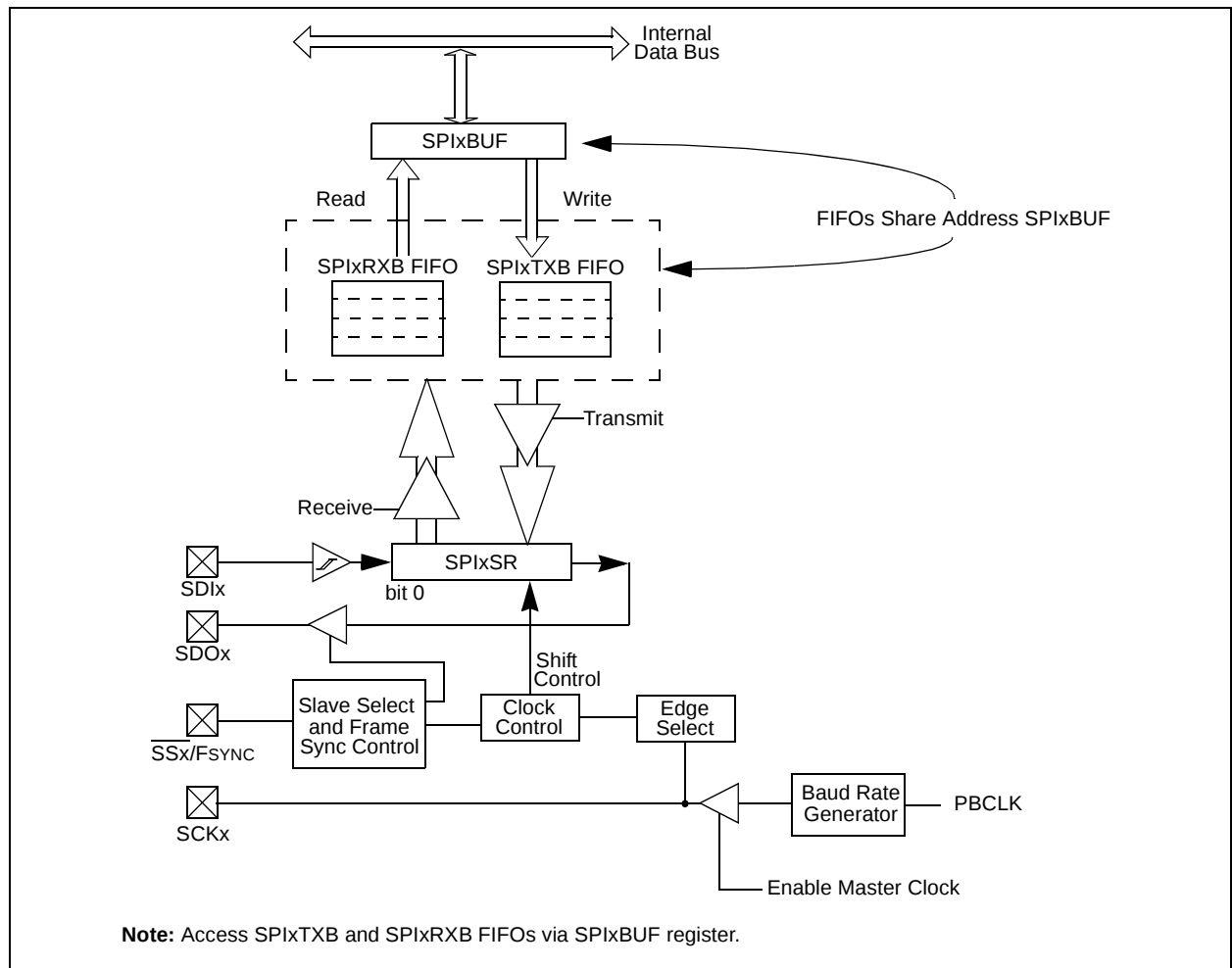
Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters, etc. The PIC32 SPI module is compatible with Motorola® SPI and SIOP interfaces.

The following are some of the key features of the SPI module:

- Master mode and Slave mode support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
 - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

FIGURE 18-1: SPI MODULE BLOCK DIAGRAM



REGISTER 22-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **HR10<3:0>**: Binary Coded Decimal value of hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>**: Binary Coded Decimal value of hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>**: Binary Coded Decimal value of minutes bits, 10 digits; contains a value from 0 to 5

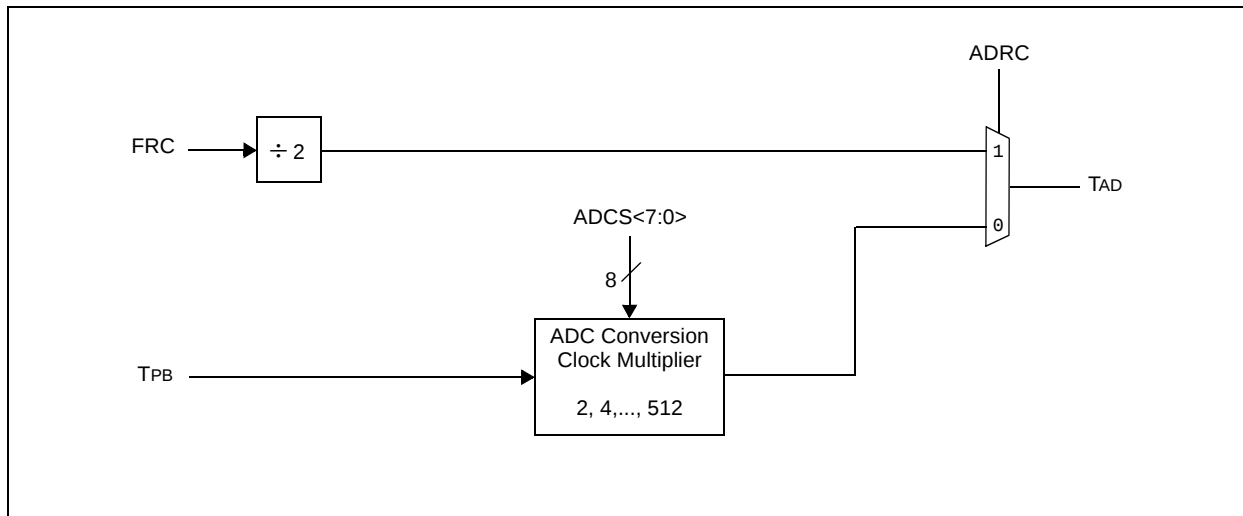
bit 19-16 **MIN01<3:0>**: Binary Coded Decimal value of minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>**: Binary Coded Decimal value of seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>**: Binary Coded Decimal value of seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented**: Read as '0'

FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



PIC32MX5XX/6XX/7XX

REGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ADRC	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
ADCS<7:0> ⁽²⁾								

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit

1 = Clock derived from FRC

0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits⁽¹⁾

11111 = 31 TAD

•
•
•

00001 = 1 TAD

00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits⁽²⁾

11111111 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 512 \cdot TPB = TAD$

•
•
•

00000001 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 4 \cdot TPB = TAD$

00000000 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 2 \cdot TPB = TAD$

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.

Note 2: This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

REGISTER 24-21: C*i*FIFOINT*n*: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)

- bit 9 **TXHALFIF**: FIFO Transmit FIFO Half Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 1 = FIFO is $\leq$ half full
 0 = FIFO is $>$ half full
 TXEN = 0: (FIFO configured as a receive buffer)
 Unused, reads '0'
- bit 8 **TXEMPTYIF**: Transmit FIFO Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 1 = FIFO is empty
 0 = FIFO is not empty, at least 1 message queued to be transmitted
 TXEN = 0: (FIFO configured as a receive buffer)
 Unused, reads '0'
- bit 7-4 **Unimplemented**: Read as '0'
- bit 3 **RXOVFLIF**: Receive FIFO Overflow Interrupt Flag bit
 TXEN = 1: (FIFO configured as a transmit buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a receive buffer)
 1 = Overflow event has occurred
 0 = No overflow event occurred
- bit 2 **RXFULLIF**: Receive FIFO Full Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a receive buffer)
 1 = FIFO is full
 0 = FIFO is not full
- bit 1 **RXHALFIF**: Receive FIFO Half Full Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a receive buffer)
 1 = FIFO is $\geq$ half full
 0 = FIFO is $<$ half full
- bit 0 **RXEMPTYIF**: Receive Buffer Not Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a transmit buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a receive buffer)
 1 = FIFO is not empty, has at least 1 message
 0 = FIFO is empty

Note 1: This bit is read-only and reflects the status of the FIFO.

PIC32MX5XX/6XX/7XX

REGISTER 25-17: ETHFRMTXOK: ETHERNET CONTROLLER FRAMES TRANSMITTED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMTXOKCNT<15:0>:** Frame Transmitted OK Count bits
Increment counter for frames successfully transmitted.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

PIC32MX5XX/6XX/7XX

REGISTER 25-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits

Increment count for frames that were successfully transmitted after there was more than one collision.

- Note 1:** This register is only used for TX operations.
- 2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.
- 3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

PIC32MX5XX/6XX/7XX

REGISTER 29-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 2-0 **FPLLIDIV<2:0>**: PLL Input Divider bits

111 = 12x divider

110 = 10x divider

101 = 6x divider

100 = 5x divider

011 = 4x divider

010 = 3x divider

001 = 2x divider

000 = 1x divider

31.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for
Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICKit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
Evaluation Kits and Starter Kits
- Third-party development tools

31.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

PIC32MX5XX/6XX/7XX

FIGURE 32-27: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

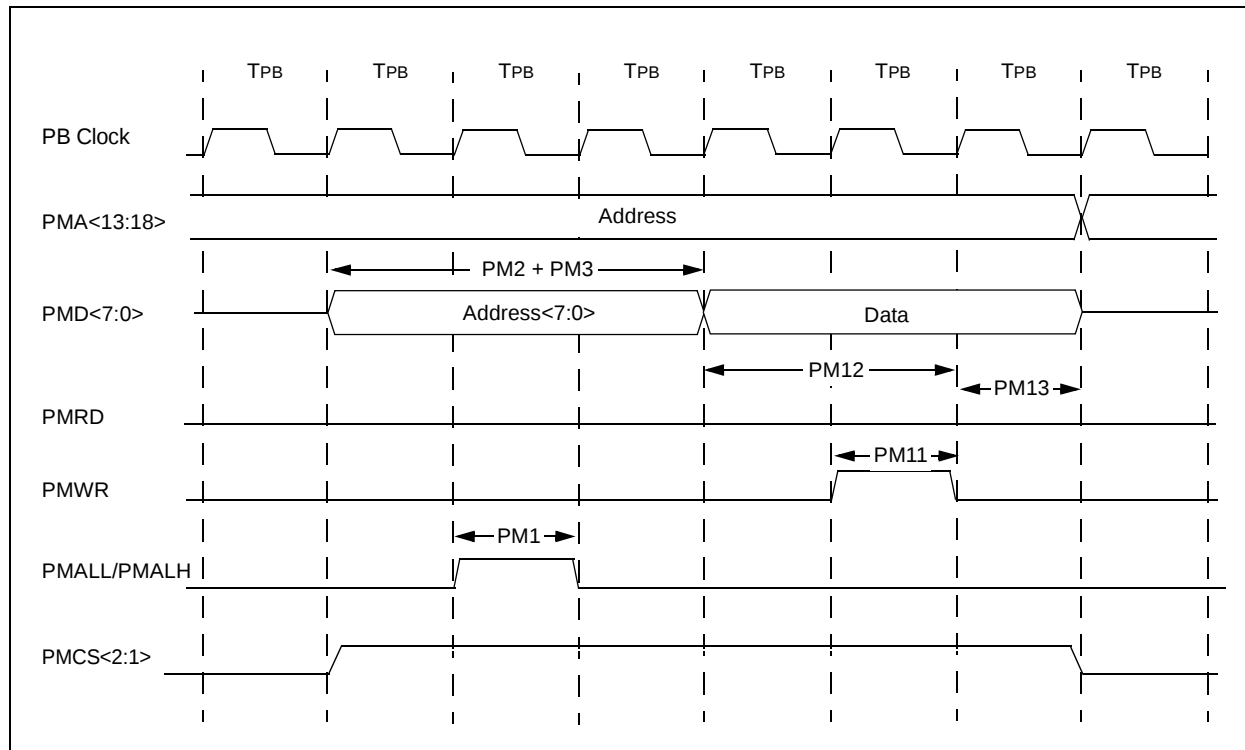


TABLE 32-41: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PM11	TWR	PMWR Pulse Width	—	1 TPB	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPB	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPB	—	—	—

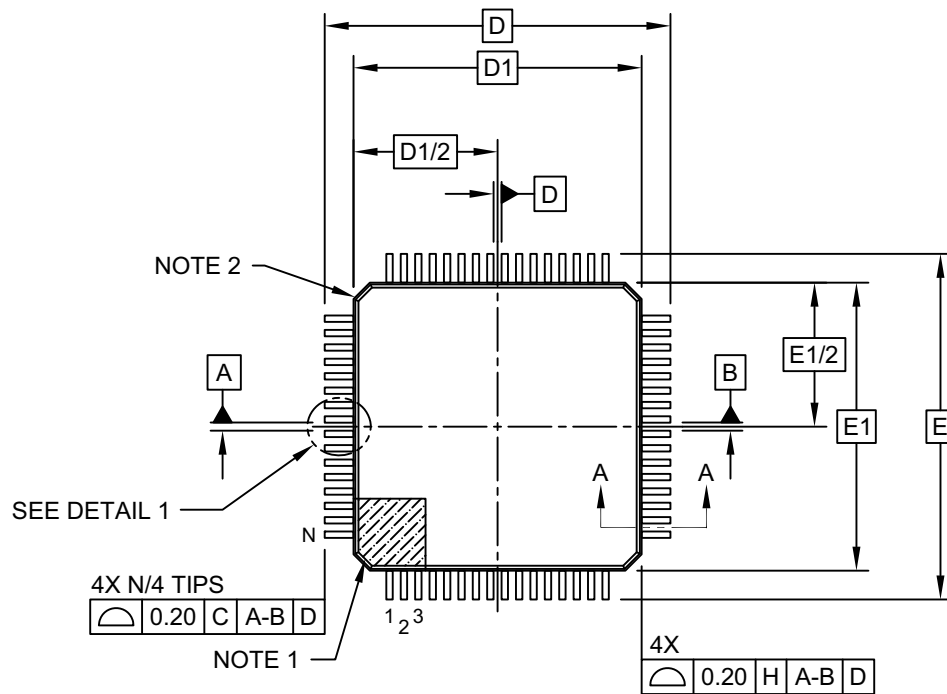
Note 1: These parameters are characterized, but not tested in manufacturing.

34.2 Package Details

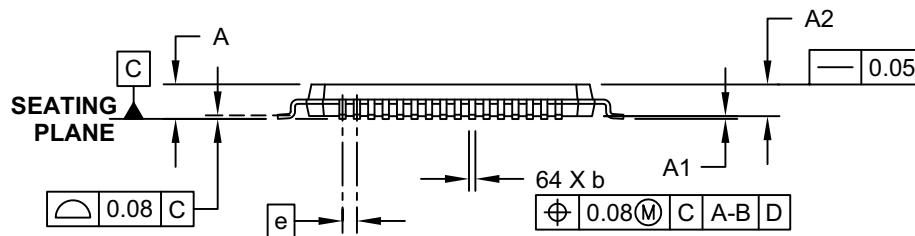
The following sections give the technical details of the packages.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



TOP VIEW



SIDE VIEW

TABLE B-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
1.0 “Electrical Characteristics”	Updated the Typical and Maximum DC Characteristics: Operating Current (IDD) in Table 1-5. Updated the Typical and Maximum DC Characteristics: Idle Current (I_{IDLE}) in Table 1-6. Updated the Typical and Maximum DC Characteristics: Power-Down Current (IPD) in Table 1-7. Added DC Characteristics: Program Memory parameters D130a and D132a in Table 1-11. Added the Internal Voltage Reference parameter (D305) to the Comparator Specifications in Table 1-13.

INDEX

A

AC Characteristics	366
10-bit Conversion Rate Parameters.....	390
ADC Specifications	388
Analog-to-Digital Conversion Requirements	391
EJTAG Timing Requirements	398
Ethernet	386
Internal FRC Accuracy	368
Internal RC Accuracy	369
OTG Electrical Specifications	397
Parallel Master Port Read Requirements	395
Parallel Master Port Write	396
Parallel Master Port Write Requirements.....	396
Parallel Slave Port Requirements	394
PLL Clock Timing	368
Analog-to-Digital Converter (ADC).....	231

B

Block Diagrams	
ADC1 Module.....	231
Comparator I/O Operating Modes.....	323
Comparator Voltage Reference	327
Connections for On-Chip Voltage Regulator.....	343
Core and Peripheral Modules	25
DMA	111
Ethernet Controller.....	279
I2C Circuit	196
Input Capture	181
Interrupt Controller	73
JTAG Programming, Debugging and Trace Ports	343
MCU	41
Output Compare Module.....	185
PIC32 CAN Module.....	241
PMP Pinout and Connections to External Devices ...	211
Prefetch Module	101
Reset System.....	69
RTCC	221
SPI Module	189
Timer1.....	167
Timer2/3/4/5 (16-Bit).....	171
Typical Multiplexed Port Structure	157
UART	203
WDT and Power-up Timer	177
Brown-out Reset (BOR)	
and On-Chip Voltage Regulator	343

C

C Compilers	
MPLAB XC.....	348
Clock Diagram	95
Comparator	
Specifications.....	364
Comparator Module	323
Comparator Voltage Reference (CVref).....	327
Configuration Bits.....	333
Controller Area Network (CAN).....	241
CPU Module.....	37
Customer Change Notification Service	437
Customer Notification Service.....	437
Customer Support.....	437

D

DC and AC Characteristics	
---------------------------------	--

Graphs and Tables	399
DC Characteristics.....	352
I/O Pin Input Specifications	360
I/O Pin Output Specifications.....	362
Idle Current (I _{IDLE})	356
Power-Down Current (I _{PD}).....	358
Program Memory	363
Temperature and Voltage Specifications.....	353
Development Support.....	347
Direct Memory Access (DMA) Controller	111

E

Electrical Characteristics	351
AC.....	366
Errata.....	23
Ethernet Controller.....	279
ETHPMM0 (Ethernet Controller Pattern Match Mask 0)...	289
ETHPMM1 (Ethernet Controller Pattern Match Mask 1)...	289
External Clock	
Timer1 Timing Requirements	372
Timer2, 3, 4, 5 Timing Requirements	373
Timing Requirements	367

F

Flash Program Memory	63
RTSP Operation	63

I

I/O Ports	157
Parallel I/O (PIO)	158
Input Capture	181
Instruction Set.....	345
Inter-Integrated Circuit (I2C)	195
Internal Voltage Reference Specifications.....	365
Internet Address	437
Interrupt Controller	73
IRG, Vector and Bit Location	74

M

MCU	
Architecture Overview	42
Coprocesor 0 Registers	43
Core Exception Types	44
EJTAG Debug Support.....	45
Power Management	45
MCU Module.....	41
Memory Map.....	52
Memory Maps.....	48, 49, 50, 51, 53
Memory Organization	47
Layout.....	47
Microchip Internet Web Site.....	437
Migration	
PIC32MX3XX/4XX to PIC32MX5XX/6XX/7XX.....	419
MPASM Assembler.....	348
MPLAB Assembler, Linker, and Librarian.....	348
MPLAB ICD 3 In-Circuit Debugger System	349
MPLAB PM3 Device Programmer	349
MPLAB REAL ICE In-Circuit Emulator System	349
MPLAB X Integrated Development Environment Software	347
MPLINK Object Linker/MPLIB Object Librarian	348

O

Open-Drain Configuration.....	158
-------------------------------	-----