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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256КВ (256К × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx675f256ht-80v-pt

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## TABLE 10: PIN NAMES FOR USB AND CAN DEVICES

121-	PIN TFBGA (BOTTOM VIEW)		L11
	PIC32MX534F064L PIC32MX564F064L PIC32MX564F128L PIC32MX575F256L PIC32MX575F512L	L1	A11
Note:	The TFBGA package skips from row "H" to row "	l" and has no "I" r	ow. A1
Pin #	Full Pin Name	Pin #	Full Pin Name
A1	PMD4/RE4	E2	T4CK/RC3
A2	PMD3/RE3	E3	SCK2/U6TXU6TX/U3RTS/PMA5/CN8/RG6
A3	TRD0/RG13	E4	T3CK/RC2
A4	PMD0/RE0	E5	VDD
A5	PMD8/RG0	E6	PMD9/RG1
A6	C1TX/PMD10/RF1	E7	Vss
A7	VDD	E8	SDA1/INT4/RA15
A8	Vss	E9	RTCC/IC1/RD8
A9	IC5/PMD12/RD12	E10	SS1/IC2/RD9
A10	OC3/RD2	E11	SCL1/INT3/RA14
A11	OC2/RD1	F1	MCLR
B1	No Connect (NC)	F2	SCL4/SDO2/U3TX/PMA3/CN10/RG8
B2	RG15	F3	SS2/U6RX/U3CTS/PMA2/CN11/RG9
B3	PMD2/RE2	F4	SDA4/SDI2/U3RX/PMA4/CN9/RG7
B4	PMD1/RE1	F5	Vss
B5	TRD3/RA7	F6	No Connect (NC)
B6	C1RX/PMD11/RF0	F7	No Connect (NC)
B7	VCAP	F8	Vdd
B8	PMRD/CN14/RD5	F9	OSC1/CLKI/RC12
B9	OC4/RD3	F10	Vss
B10	Vss	F11	OSC2/CLKO/RC15
B11	SOSCO/T1CK/CN0/RC14	G1	INT1/RE8
C1	PMD6/RE6	G2	INT2/RE9
C2	VDD	G3	TMS/RA0
C3	TRD1/RG12	G4	No Connect (NC)
C4	TRD2/RG14	G5	VDD
C5	TRCLK/RA6	G6	Vss
C6		G7	VSS
C7		G8	
C0	Voo	G9	IDU/RA3
C10		G10	
C10			
D1	T2CK/RC1	H2	
D2	PMD7/RF7	H3	Vee
D2 D3	PMD5/RE5	H4	Voo
D4	Vss	H5	No Connect (NC)
D5	Vss	H6	
D6	No Connect (NC)	H7	No Connect (NC)
D7	PMD14/CN15/RD6	H8	VBUS
D8	PMD13/CN19/RD13	H9	VUSB3V3
D9	SD01/0C1/INT0/RD0	H10	D+/RG2
D10	No Connect (NC)	H11	SCL2/RA2
D11	SCK1/IC3/PMCS2/PMA15/RD10		AN3/C2IN+/CN5/RB3
E1	T5CK/SDI1/RC4		AN2/C2IN-/CN4/RB2
Note 1:	Shaded pins are 5V tolerant.		1

# PIC32MX5XX/6XX/7XX

## TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

		Pin Nun	nber <sup>(1)</sup>				
Pin Name	64-Pin QFN/TQFP	100-Pin TQFP	121-Pin TFBGA	124-pin VTLA	Pin Type	Buffer Type	Description
TMS	23	17	G3	B9	I	ST	JTAG Test mode select pin
TCK	27	38	J6	A26	I	ST	JTAG test clock input pin
TDI	28	60	G11	A40	I	ST	JTAG test data input pin
TDO	24	61	G9	B33	0		JTAG test data output pin
RTCC	42	68	E9	B37	0		Real-Time Clock alarm output
CVREF-	15	28	L2	A21	I	Analog	Comparator Voltage Reference (low)
CVREF+	16	29	K3	B17	I	Analog	Comparator Voltage Reference (high)
CVREFOUT	23	34	L5	A24	0	Analog	Comparator Voltage Reference output
C1IN-	12	21	H2	B11	I	Analog	Comparator 1 negative input
C1IN+	11	20	H1	A12	I	Analog	Comparator 1 positive input
C1OUT	21	32	K4	A23	0		Comparator 1 output
C2IN-	14	23	J2	B13	I	Analog	Comparator 2 negative input
C2IN+	13	22	J1	A13	I	Analog	Comparator 2 positive input
C2OUT	22	33	L4	B19	0	—	Comparator 2 output
PMA0	30	44	L8	A29	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	29	43	K7	B24	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2	8	14	F3	A9	0	_	Parallel Master Port address
PMA3	6	12	F2	A8	0		(Demultiplexed Master modes)
PMA4	5	11	F4	B6	0		
PMA5	4	10	E3	A7	0		
PMA6	16	29	K3	B17	0		
PMA7	22	28	L2	A21	0		
PMA8	32	50	L11	A32	0		
PMA9	31	49	L10	B27	0		
PMA10	28	42	L7	A28	0		
PMA11	27	41	J7	B23	0		
PMA12	24	35	J5	B20	0		
PMA13	23	34	L5	A24	0		
PMA14	45	71	C11	A46	0		
PMA15	44	70	D11	B38	0		
PMCS1	45	71	C11	A46	0		Parallel Master Port Chip Select 1 strobe
PMCS2	44	70	D11	B38	0	—	Parallel Master Port Chip Select 2 strobe
Legend: C S T	MOS = CMC T = Schmitt T TL = TTL ing	S compatib Frigger input ut buffer	le input or c t with CMO	output S levels	A C	nalog = A = Outpu	Analog input P = Power t I = Input

Note 1: Pin numbers are only provided for reference. See the "Device Pin Tables" section for device pin availability.

2: See 25.0 "Ethernet Controller" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	R	R	R	R	R	R	R	R
31:24				BMXDRM	1SZ<31:24>			
22.16	R	R	R	R	R	R	R	R
23.10				BMXDRN	ISZ<23:16>			
45.0	R	R	R	R	R	R	R	R
15:8				BMXDRI	MSZ<15:8>			
7.0	R	R	R	R	R	R	R	R
7:0				BMXDR	MSZ<7:0>			

#### REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXDRMSZ<31:0>:** Data RAM Memory (DRM) Size bits Static value that indicates the size of the Data RAM in bytes: 0x00004000 = device has 16 KB RAM 0x00008000 = device has 32 KB RAM 0x00010000 = device has 64 KB RAM

# REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER<sup>(1,2)</sup>

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	—	—	—	—		BMXPUPE	3A<19:16>	
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
15:8				BMXPU	PBA<15:8>			
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				BMXPU	PBA<7:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 Unimplemented: Read as '0'

bit 19-11 BMXPUPBA<19:11>: Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>:** Program Flash (PFM) User Program Base Address Read-Only bits Value is always '0', which forces 2 KB increments

- **Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.
  - **2:** The value in this register must be less than or equal to BMXPFMSZ.

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	_	—	—		-	-
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—		—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
7:0	_	_	_	_	_	_	_	SWRST <sup>(1)</sup>

#### REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Legend:	HC = Cleared by hardware					
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-1 Unimplemented: Read as '0'

- bit 0 SWRST: Software Reset Trigger bit<sup>(1)</sup> 1 = Enable software Reset event 0 = No effect
- Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

#### **TABLE 7-4:** INTERRUPT REGISTER MAP FOR PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES (CONTINUED)

ess										В	its													
Virtual Addr (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset					
1000		31:16	_	_	_		INT4IP<2:0	>	INT4I	S<1:0>	_	_	_		OC4IP<2:0>	>	OC4IS	<1:0>	000					
1000	1604	15:0	_	_	-		IC4IP<2:0>		IC4IS	S<1:0>	_	_	_		T4IP<2:0>		T4IS-	<1:0>	000					
1050	IDCE	31:16	—		_	—	—	—	—	_		_	—		OC5IP<2:0>	>	OC5IS	<1:0>	000					
IUEU	IFC5	15:0	—	_	_		IC5IP<2:0>		IC5IS	S<1:0>	_	_	—		T5IP<2:0>		T5IS-	<1:0>	000					
		31:16	_	_	-		AD1IP<2:0>	•	AD1IS	S<1:0>	_	_	_		CNIP<2:0>		CNIS	<1:0>	000					
1050	IDCC														U1IP<2:0>		U1IS-	<1:0>						
TUFU	IPC6	15:0	_	—	_		I2C1IP<2:0>	>	I2C1IS<1:0>		—	—	_		SPI3IP<2:0:	>	SPI3IS	S<1:0>	000					
														I2C3IP<2:0>			12C315	6<1:0>						
							U3IP<2:0>		U3IS<1:0>															
1100		31:16	_	—	—		SPI2IP<2:0;	12IP<2:0>		S<1:0>	—	—	—		CMP2IP<2:0	>	CMP2I	S<1:0>	000					
1100	11 07						I2C4IP<2:0>		I2C4I	S<1:0>														
		15:0	_		—	(	CMP1IP<2:0>		CMP1	IS<1:0>		—	-		PMPIP<2:0>	>	PMPIS	S<1:0>	000					
		31:16	_		—		RTCCIP<2:0	>	RTCCI	S<1:0>		—	-		SCMIP<2:0	>	FSCMI	S<1:0>	000					
1110	IPC8														U2IP<2:0>		U2IS-	<1:0>						
1110	11 00	15:0	—	—	—	—	—	-	-	—	—	—	-		SPI4IP<2:0>	>	SPI4IS	S<1:0>	000					
															I2C5IP<2:0>	>	12C515	5<1:0>						
1120	IPC9	31:16	_		—		DMA3IP<2:0	>	DMA3	IS<1:0>		—	-		DMA2IP<2:0	>	DMA2I	S<1:0>	000					
1120	11 00	15:0	—		—		DMA1IP<2:0>		DMA1	IS<1:0>	—	—	—	1	DMA0IP<2:0	>	DMA0I	S<1:0>	000					
1130	IPC10	31:16	—		—	D	MA7IP<2:0>	.(2)	DMA7IS	6<1:0> <sup>(2)</sup>	—	—	—	D	MA6IP<2:0>	(2)	DMA6IS	<1:0> <sup>(2)</sup>	000					
1150	11 010	15:0	_		—	D	MA5IP<2:0>	.(2)	DMA5IS	S<1:0> <sup>(2)</sup>		—	-	D	MA4IP<2:0>	(2)	DMA4IS	<1:0> <sup>(2)</sup>	000					
1140	IPC11	31:16	—		—	CAN2IP<2:0> <sup>(2)</sup>		CAN2IP<2:0> <sup>(2)</sup>		CAN2IP<2:0> <sup>(2)</sup>		CAN2IP<2:0> <sup>(2)</sup>		CAN2IS	S<1:0> <sup>(2)</sup>	—	—	—		CAN1IP<2:0	>	CAN1	S<1:0>	000
1140		15:0	_	_	—		USBIP<2:0>	>	USBIS	S<1:0>	_	—	—		FCEIP<2:0>	>	FCEIS<1:0>		000					
1150	IPC12	31:16	_	—	—		U5IP<2:0>		U5IS	U5IS<1:0>		—	-		U6IP<2:0>		U6IS-	<1:0>	000					
1150	11 012	15:0		—			U4IP<2:0>		U4IS	<1:0>	—	-	-		ETHIP<2:0>	>	ETHIS	i<1:0>	000					

Legend: x = unknown value on Reset; ---- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Note 1: Registers" for more information. This bit is unimplemented on PIC32MX764F128H device. This register does not have associated CLR, SET, and INV registers.

2:

3:

# PIC32MX5XX/6XX/7XX

NOTES:

## REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

- bit 6 **CRCAPP:** CRC Append Mode bit<sup>(1)</sup>
  - 1 = The DMA transfers data from the source into the CRC but not to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
  - 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5 CRCTYP: CRC Type Selection bit
  - 1 = The CRC module will calculate an IP header checksum
  - 0 = The CRC module will calculate a LFSR CRC
- bit 4-3 Unimplemented: Read as '0'
- bit 2-0 CRCCH<2:0>: CRC Channel Select bits
  - 111 = CRC is assigned to Channel 7
  - 110 = CRC is assigned to Channel 6
  - 101 = CRC is assigned to Channel 5
  - 100 = CRC is assigned to Channel 4
  - 011 = CRC is assigned to Channel 3
  - 010 = CRC is assigned to Channel 2
  - 001 = CRC is assigned to Channel 1
  - 000 = CRC is assigned to Channel 0
- **Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

#### 11.1 **Control Registers**

#### TABLE 11-1: USB REGISTER MAP

SSS											Bits								
Virtual Addre (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5040		31:16	_	_	_		_	—	_	_	—	-	—	—	-	-	—	_	0000
0040	ororolic	15:0	_	_	_	_	_	—	_	_	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	_	VBUSVDIF	0000
5050	<b>U1OTGIE</b>	31:16	—	_	—	_	_	—		_	—	_	—	—	_	—		_	0000
		15:0	_	_	_	_	_	_	_	_	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	_	VBUSVDIE	0000
5060	U1OTGSTAT <sup>(3)</sup>	31:16	_	_	_		_	_		_	-		-	_	-	—	_	—	0000
		15:0	_	_	_		_	_		_	ID		LSTATE	_	SESVD	SESEND	_	VBUSVD	0000
5070	U1OTGCON	31:16	_	—	_	_	_		_	—	-	-					-	-	0000
		15:0	_	—	_	_	_		_	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	_	_	_	_	_	_	_	_		_	_			_			0000
		15.0	_					_			UACTPIND()		_	USLPGRD	0300031		USUSPEND	USDPWK	0000
5200	LI41D(2)	31.10	_					_				_	_		_	_			0000
5200	UTIK	15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	DETACHIF	0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
5210	U1IE	15:0	_	_	_	-	_	_	_		STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE		0000
		31.16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_		0000
5220	U1EIR <sup>(2)</sup>	00															CRC5EF		0000
0220	0.2.11	15:0	—	—	—	—	—	—	—	-	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	EOFEF	PIDEF	0000
		31:16	_		-			_			-		_	-			-		0000
5230	U1EIE	15.0	_	_	_	_	_	_	_	_	BTSEE	BMXEE		BTOFF		CRC16EE	CRC5EE	PIDEE	0000
		10.0									DIGEL	DIWIXEE	DMALL	DIGEL	DINOLL	ONOTOLL	EOFEE	TIDEE	0000
5240	U1STAT(3)	31:16	—	_	—	_	—	—	_	—	—	—	_	—	_	_	—	_	0000
02.0	010.0	15:0	—	_	—	_	_	—	_	_		ENDPT	<3:0> <sup>(4)</sup>		DIR	PPBI	—	_	0000
		31:16	—	_	—	_	_	—		_	—	_	—	—	_	—		_	0000
5250	U1CON	15:0	_	_	_	_	_	_	_	_	JSTATE <sup>(4)</sup>	SE0 <sup>(4)</sup>	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
5260	U1ADDR	31:16	-	_	_	_	_	-	_	_	-	_	—		—		—	—	0000
		15:0	—	—	_	_	_	—	—	_	LSPDEN			DE	VADDR<6:0	)>			0000
5270	U1BDTP1	31:16	—	—	_	_	_	—	—	_	_	—			—	—	—	_	0000
		15:0	-	_	-	-	-	-	-	-			BL	JIPIRL :1				—	0000

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 12.1.1 "CLR, SET and INV Registers" for Note 1: more information.

2:

This register does not have associated SET and INV registers. This register does not have associated CLR, SET and INV registers. 3:

4: Reset value for this bit is undefined.

### REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 3 Unimplemented: Read as '0'
  bit 2 TSYNC: Timer External Clock Input Synchronization Selection bit When TCS = 1: 1 = External clock input is synchronized 0 = External clock input is not synchronized When TCS = 0: This bit is ignored.
  bit 1 TCS: Timer Clock Source Select bit 1 = External clock from TxCKI pin 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

#### I2CxSTAT: I<sup>2</sup>C STATUS REGISTER (CONTINUED) REGISTER 19-2: **D\_A:** Data/Address bit (when operating as I<sup>2</sup>C slave) bit 5 This bit is cleared by hardware upon a device address match, and is set by hardware by reception of the slave byte. 1 = Indicates that the last byte received was data 0 = Indicates that the last byte received was device address bit 4 P: Stop bit This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected. 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last bit 3 S: Start bit This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected. 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last **R\_W:** Read/Write Information bit (when operating as I<sup>2</sup>C slave) bit 2 This bit is set or cleared by hardware after reception of an I<sup>2</sup>C device address byte. 1 = Read – indicates data transfer is output from slave 0 = Write - indicates data transfer is input to slave **RBF:** Receive Buffer Full Status bit bit 1 This bit is set by hardware when the I2CxRCV register is written with a received byte, and is cleared by hardware when software reads I2CxRCV. 1 = Receive complete, I2CxRCV is full 0 = Receive not complete, I2CxRCV is empty bit 0 TBF: Transmit Buffer Full Status bit This bit is set by hardware when software writes to the I2CxTRN register, and is cleared by hardware upon completion of data transmission.

1 = Transmit in progress, I2CxTRN is full

0 = Transmit complete, I2CxTRN is empty

## 22.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time. A simplified block diagram of the RTCC module is illustrated in Figure 22-1. Key features of the RTCC module include:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- · Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- · BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- · Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin



### FIGURE 22-1: RTCC BLOCK DIAGRAM

### REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

- bit 4 CLRASAM: Stop Conversion Sequence bit (when the first ADC interrupt is generated)
  - 1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
  - 0 = Normal operation, buffer contents will be overwritten by the next conversion sequence
- bit 3 Unimplemented: Read as '0'
- bit 2 ASAM: ADC Sample Auto-Start bit
  - 1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
  - 0 = Sampling begins when SAMP bit is set
- bit 1 SAMP: ADC Sample Enable bit<sup>(2)</sup>
  - 1 = The ADC S&H circuit is sampling
  - 0 = The ADC S&H circuit is holding
  - When ASAM = 0, writing '1' to this bit starts sampling.
  - When SSRC < 2:0 > = 000, writing '0' to this bit will end sampling and start conversion.

### bit 0 **DONE:** Analog-to-Digital Conversion Status bit<sup>(3)</sup>

- Clearing this bit will not affect any operation in progress.
  - 1 = Analog-to-digital conversion is done
  - 0 = Analog-to-digital conversion is not done or has not started
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write a '0' to end sampling and start conversion. If SSRC<2:0> ≠ '000', this bit is automatically cleared by hardware to end sampling and start conversion.
  - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22.10	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
23.10	—	—	ТХВО	TXBP	RXBP	TXWARN	RXWARN	EWARN
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
10.0				TERRC	NT<7:0>			
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7.0				RERRC	NT<7:0>			

#### REGISTER 24-5: CITREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-22 Unimplemented: Read as '0'

bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT  $\geq$  256)

- bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT  $\geq$  128)
- bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT  $\geq$  128)
- bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)
- bit 17 **RXWARN:** Receiver in Error State Warning  $(128 > \text{RERRCNT} \ge 96)$
- bit 16 EWARN: Transmitter or Receiver is in Error State Warning
- bit 15-8 TERRCNT<7:0>: Transmit Error Counter
- bit 7-0 RERRCNT<7:0>: Receive Error Counter

#### REGISTER 24-6: CIFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
31.24	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 FIFOIP<31:0>: FIFOn Interrupt Pending bits

1 = One or more enabled FIFO interrupts are pending

0 = No FIFO interrupts are pending

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31:24	SID<10:3>								
22.16	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	
23.10	SID<2:0>			—	MIDE	—	EID<	17:16>	
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
10.0	EID<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
				EID<7	7:0>				

#### REGISTER 24-9: CIRXMn: CAN ACCEPTANCE FILTER MASK 'n' REGISTER (n = 0, 1, 2 OR 3)

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 SID<10:0>: Standard Identifier bits

- 1 = Include the SIDx bit in filter comparison
- 0 = The SIDx bit is a 'don't care' in filter operation
- bit 20 Unimplemented: Read as '0'
- bit 19 MIDE: Identifier Receive Mode bit
  - 1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
  - 0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

#### bit 18 Unimplemented: Read as '0'

bit 17-0 EID<17:0>: Extended Identifier bits

- 1 = Include the EIDx bit in filter comparison
- 0 = The EIDx bit is a 'don't care' in filter operation

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

### REGISTER 24-12: CIFLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)

FLTEN9: Filter 9 Enable bit
<ul><li>1 = Filter is enabled</li><li>0 = Filter is disabled</li></ul>
MSEL9<1:0>: Filter 9 Mask Select bits
<ul> <li>11 = Acceptance Mask 3 selected</li> <li>10 = Acceptance Mask 2 selected</li> <li>01 = Acceptance Mask 1 selected</li> <li>00 = Acceptance Mask 0 selected</li> </ul>
FSEL9<4:0>: FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0
FLTEN8: Filter 8 Enable bit
<ul><li>1 = Filter is enabled</li><li>0 = Filter is disabled</li></ul>
MSEL8<1:0>: Filter 8 Mask Select bits
<ul> <li>11 = Acceptance Mask 3 selected</li> <li>10 = Acceptance Mask 2 selected</li> <li>01 = Acceptance Mask 1 selected</li> <li>00 = Acceptance Mask 0 selected</li> </ul>
FSEL8<4:0>: FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

## REGISTER 25-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	_	_	_		—	
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—		_	_		—	
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HTEN	MPEN	_	NOTPM	PMMODE<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CRCERREN	CRCOKEN	RUNTERREN	RUNTEN	UCEN	NOTMEEN	MCEN	BCEN

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 **HTEN:** Enable Hash Table Filtering bit
  - 1 = Enable Hash Table Filtering
    - 0 = Disable Hash Table Filtering
- bit 14 **MPEN:** Magic Packet<sup>™</sup> Enable bit 1 = Enable Magic Packet Filtering 0 = Disable Magic Packet Filtering
- bit 13 Unimplemented: Read as '0'
- bit 12 **NOTPM:** Pattern Match Inversion bit
  - 1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
  - 0 = The Pattern Match Checksum must match for a successful Pattern Match to occur

This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

- bit 11-8 PMMODE<3:0>: Pattern Match Mode bits
  - 1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)<sup>(1,3)</sup>
  - 1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)<sup>(1,2)</sup>
  - 0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)<sup>(1)</sup>
  - 0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)<sup>(1)</sup>
  - 0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)<sup>(1)</sup>
  - 0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)<sup>(1)</sup>
  - 0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)<sup>(1)</sup>
  - 0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)<sup>(1)</sup>
  - 0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)<sup>(1)</sup>
  - 0000 = Pattern Match is disabled; pattern match is always unsuccessful

#### **Note 1:** XOR = True when either one or the other conditions are true, but not both.

- 2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
- 3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

**Note 1:** This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

#### TABLE 32-36: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard O (unless oth Operating te	perating C erwise stat mperature	onditions ( ted) -40°C ≤ TA -40°C ≤ TA	see Not ≤ +85°0 ≤ +105°	e 5): 2.5V to 3.6V C for Industrial C for V-Temp
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
ADC Ac	curacy – N	leasurements with Inter	nal VREF+/VR	EF-			
AD20d	Nr	Resolution		10 data bits		bits	(Note 3)
AD21d	INL	Integral Nonlinearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD22d	DNL	Differential Nonlinearity	> -1		< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Notes 2,3)
AD23d	Gerr	Gain Error	> -4	_	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD24d	EOFF	Offset Error	> -2	_	< 2	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD25d	—	Monotonicity	—	—	_	_	Guaranteed
Dynami	c Performa	ince					
AD31b	SINAD	Signal to Noise and Distortion	55	58.5		dB	(Notes 3,4)
AD34b	ENOB	Effective Number of Bits	9.0	9.5	_	bits	(Notes 3,4)

**Note 1:** These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

**3:** These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

**5:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

## TABLE B-7: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
32.0 "Electrical Characteristics"	Note 4 in the Operating Current specification was updated (see Table 32-5).
	Note 3 in the Idle Current specification was updated (see Table 32-6).
	Note 6 references in the Power-Down Current specification were updated (see Table 32-7).
	The Program Memory parameters, D135, D136, and D137, and Note 4 were updated (see Table 32-11).
	The Voltage Reference Specifications were updated (see Table 32-14).
	Parameter DO50 (Cosco) was added to the Capacitive Loading Requirements on Output Pins (see Table 32-16).
	The EJTAG Timing Characteristics were updated (see Figure 32-28).
	The maximum value for parameters ET13 and ET14 were updated in the Ethernet Module Specifications (see Table 32-35).
	Parameter PM7 (TDHOLD) was updated (see Table 32-40).
34.0 "Packaging Information"	Packaging diagrams were updated.
Product Identification System	The Speed and Program Memory Size were updated and Note 1 was added.

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